TOSHIBA Field Effect Transistor Silicon N Channel MOS Type

SSM3K44FS

High Speed Switching Applications Analog Switching Applications

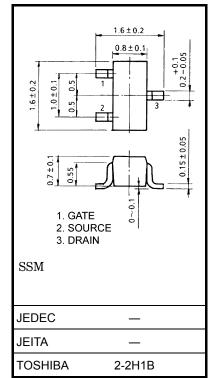
- Compact package suitable for high-density mounting
- Low ON-resistance : $R_{DS(ON)} = 4.0 \Omega (max) (@V_{GS} = 4 V)$

: $R_{DS(ON)} = 7.0 \Omega (max) (@V_{GS} = 2.5 V)$

Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit	
Drain-Source voltage		V _{DSS}	30	V	
Gate-Source voltage		V _{GSS}	±20	V	
Drain current	DC	۱ _D	100	mA	
	Pulse	I _{DP}	200		
Drain power dissipation (Ta = 25°C)		P _D (Note 1)	150	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	–55 to 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.



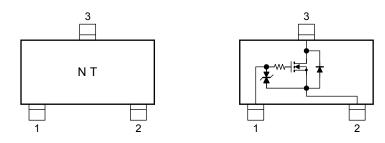
Weight: 2.4 mg (typ.)

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: mounted on an FR4 board (25.4 mm × 25.4 mm × 1.6 mm, Cu Pad : 0.36mm²×3)

Marking

Equivalent Circuit



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), be sure that the environment is protected against electrostatic electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Unit: mm

90%

tf

toff

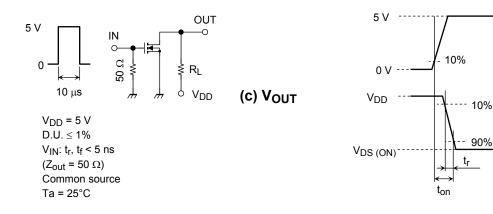
Electrical Characteristics (Ta = 25°C)

Characteristic		Symbol	Test Condition	Min	Тур.	Max	Unit	
Gate leakage current		I _{GSS}	V_{GS} = ±14 V, V_{DS} = 0 V	_	_	±1	μA	
Drain-Source breakdown voltage		V (BR) DSS	I _D = 0.1 mA, V _{GS} = 0 V	30	_		V	
Drain Cut-off current		IDSS	V _{DS} = 30 V, V _{GS} = 0 V	_	_	1	μA	
Gate threshold voltage		V _{th}	V _{DS} = 3 V, I _D = 0.1 mA	0.8	_	1.5	V	
Forward transfer admittance		Y _{fs}	V _{DS} = 3 V, I _D = 10 mA	25	_	_	mS	
Drain-Source ON resistance		R _{DS (ON)}	I _D = 10 mA, V _{GS} = 4 V	_	2.2	4.0	Ω	
			I _D = 10 mA, V _{GS} = 2.5 V	_	4.0	7.0	52	
Input capacitance		C _{iss}	V _{DS} = 3 V, V _{GS} = 0 V, f = 1 MHz	_	8.5	_	pF	
Reverse transfer capacitance		C _{rss}		_	5.3	_		
Output capacitance		C _{oss}		_	9.4	—		
Switching time	Turn-on time	t _{on}	V _{DD} = 5 V, I _D = 10 mA,	—	50	—	ns	
	Turn-off time	t _{off}	$V_{GS} = 0$ to 5 V	_	200			

Switching Time Test Circuit

(a) Test circuit

(b) V_{IN}

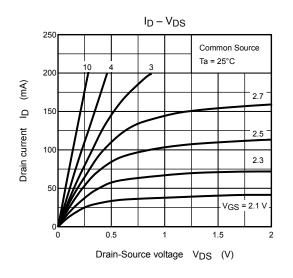


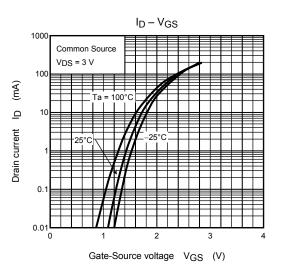
Precaution

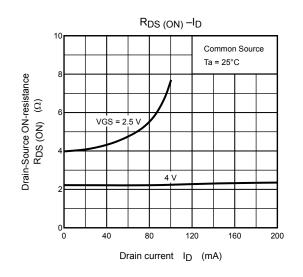
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (0.1mA for the SSM3K44FS). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

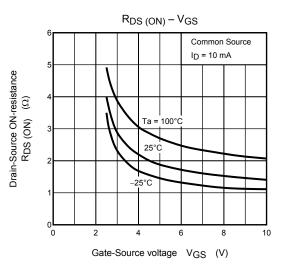
Take this into consideration when using the device

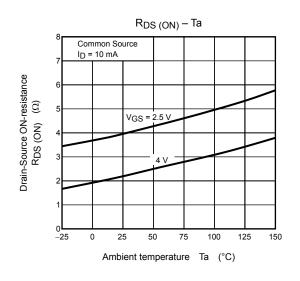
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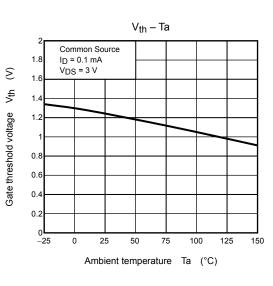




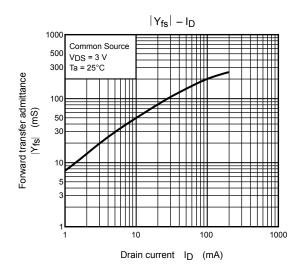


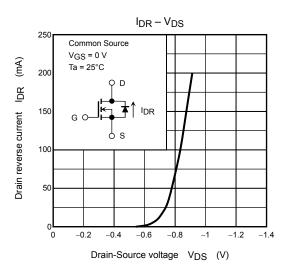


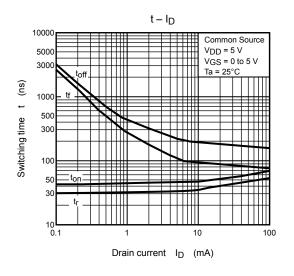


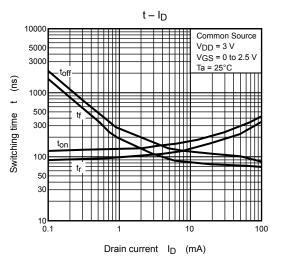


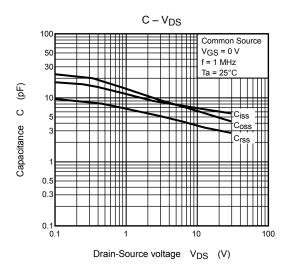
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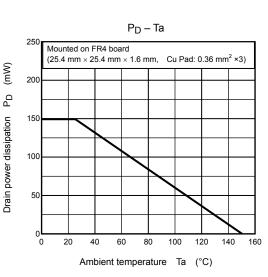












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