Unit: mm

TOSHIBA Field-Effect Transistor Silicon N Channel MOS Type (U-MOSIV)

SSM3K7002BFU

High-Speed Switching Applications Analog Switch Applications

Small package

: $R_{DS(ON)} = 3.3 \Omega \text{ (max) } (@V_{GS} = 4.5 \text{ V})$ Low ON-resistance

> : $R_{DS(ON)} = 2.6 \Omega \text{ (max) } (@V_{GS} = 5 \text{ V})$: $R_{DS(ON)} = 2.1 \Omega \text{ (max) } (@V_{GS} = 10 \text{ V})$

Absolute Maximum Ratings (Ta = 25°C)

Characteristics		Symbol	Rating	Unit	
Drain-source voltage		V_{DSS}	60	V	
Gate-source voltage		V _{GSS}	± 20	V	
Drain current	DC	ID	200	mA	
	Pulse	I _{DP}	800		
Drain power dissipation (Ta = 25°C)		P _D (Note 1)	150	mW	
Channel temperature		T _{ch}	150	°C	
Storage temperature range		T _{stg}	-55 to 150	°C	

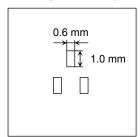
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the

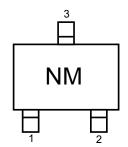
Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: mounted on FR4 board

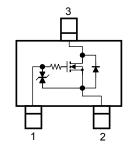
 $(25.4 \text{ mm} \times 25.4 \text{ mm} \times 1.6 \text{ mm}, \text{ Cu Pad: } 0.6 \text{mm}^2 \times 3)$

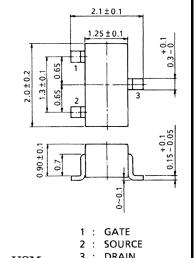


Marking



Equivalent Circuit (top view)





3 : DRAIN USM

JEDEC JEITA SC-70 **TOSHIBA** 2-2E1E

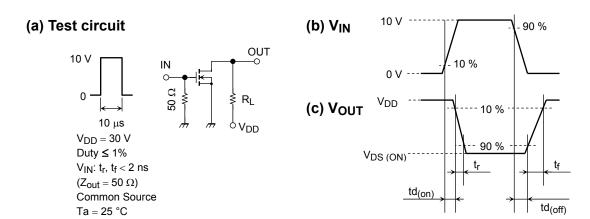
Weight: 6.0 mg (typ.)

Electrical Characteristics (Ta = 25°C)

Char	acteristics	Symbol	Test Condition		Min	Тур	Max	Unit	
Gate leakage curr	ent	I _{GSS}	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$		_	_	± 10	μА	
Drain-source breakdown voltage		V (BR) DSS	$I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V}$		60	_	_	V	
		V (BR) DSX	I _D = 10 mA, V _{GS} = -10 V		45	_	_	V	
Drain cutoff currer	nt	I _{DSS}	$V_{DS} = 60 \text{ V}, V_{GS} = 0 \text{ V}$		_		1	μΑ	
Gate threshold vo	Itage	V_{th}	$V_{DS} = 10 \text{ V}, I_{D} = 0.25 \text{ mA}$		1.5	_	3.1	V	
Forward transfer a	admittance	Y _{fs}	$V_{DS} = 10 \text{ V}, I_D = 200 \text{ mA}$	(Note 2)	225	_	_	mS	
Drain-source ON-resistance		R _{DS} (ON)	$I_D = 500 \text{ mA}, V_{GS} = 10 \text{ V}$	(Note 2)	_	1.62	2.1	Ω	
			$I_D = 100 \text{ mA}, V_{GS} = 5 \text{ V}$	(Note 2)	_	1.90	2.6		
			$I_D = 100 \text{ mA}, V_{GS} = 4.5 \text{ V}$	(Note 2)	_	2.10	3.3		
Input capacitance		C _{iss}	V _{DS} = 25 V, V _{GS} = 0 V, f = 1 MHz		_	17.0	_	pF	
Reverse transfer capacitance		C _{rss}			_	1.9	_		
Output capacitance		Coss			_	3.6	_		
Switching time	Turn-on delay time	td _(on)	V _{DD} = 30 V , I _D = 200 mA ,	_	3.3	6.6	ns		
	Turn-off delay time	td _(off)	V _{GS} = 0 to 10 V		_	14.5		40	
Drain-source forward voltage		V _{DSF}	I _D = -200 mA, V _{GS} = 0 V	(Note 2)	_	-0.84	-1.2	V	

Note2: Pulse test

Switching Time Test Circuit

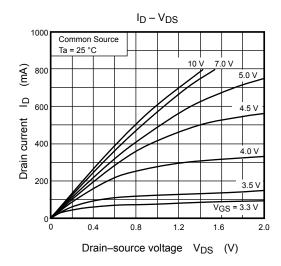


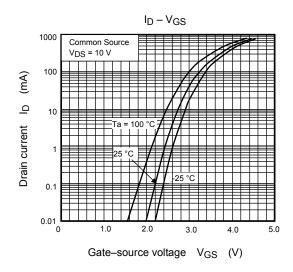
Precaution

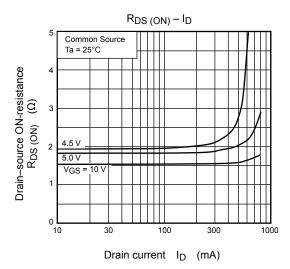
Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to be low (0.25 mA for the SSM3K7002BFU). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$. Take this into consideration when using the device

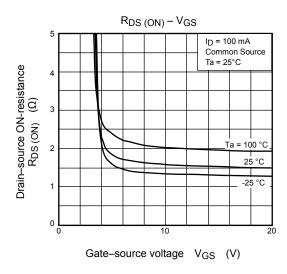
Handling Precaution

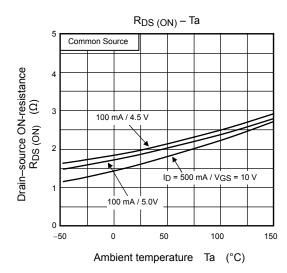
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

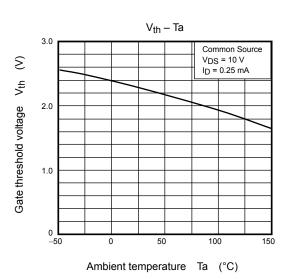


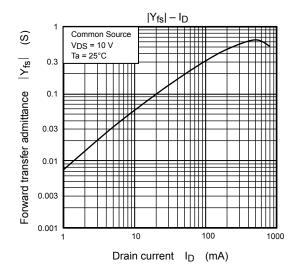


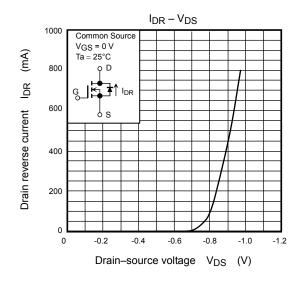


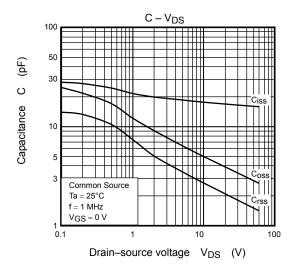


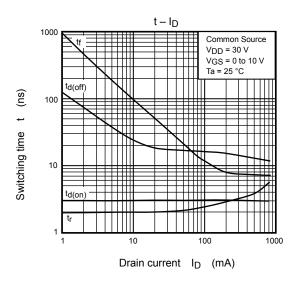


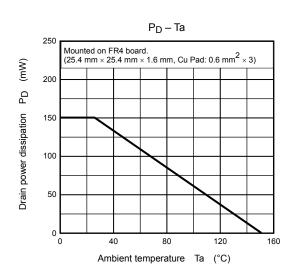












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