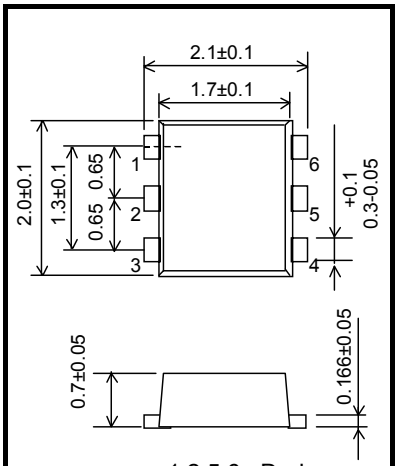
TOSHIBA Field-Effect Transistor Silicon N-Channel MOS Type

# SSM6K407TU

○ DC−DC Converter, Relay Drive and Motor Drive Applications

- 4V drive
- Low ON-resistance :$R_{on}$ = 440mΩ (max) (@$V_{GS}$ = 4 V)
  :$R_{on}$ = 300mΩ (max) (@$V_{GS}$ = 10 V)

Unit: mm




1,2,5,6 : Drain
3 : Gate
4 : Source

UF6

| | |
|---|---|
| JEDEC | ― |
| JEITA | ― |
| TOSHIBA | 2-2T1D |

Weight: 7mg (typ.)

## Absolute Maximum Ratings (Ta = 25°C) (Note)

| Characteristic | | Symbol | Rating | Unit |
|---|---|---|---|---|
| Drain–source voltage | | $V_{DSS}$ | 60 | V |
| Gate–source voltage | | $V_{GSS}$ | ±20 | V |
| Drain current | DC | $I_D$ | 2 | A |
| | Pulse | $I_{DP}$ | 6 | |
| Drain power dissipation | | $P_D$ (Note1) | 500 | mW |
| Channel temperature | | $T_{ch}$ | 150 | °C |
| Storage temperature | | $T_{stg}$ | −55~150 | °C |

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/“Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Mounted on an FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 $mm^2$)

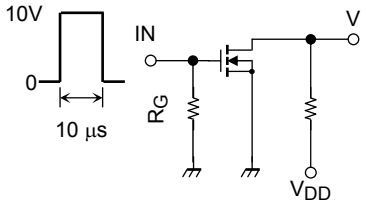
## Electrical Characteristics (Ta = 25°C)

| Characteristic | | Symbol | Test Condition | Min | Typ. | Max | Unit |
|---|---|---|---|---|---|---|---|
| Gate leakage current | | $I_{GSS}$ | $V_{GS}$ = ±16 V, $V_{DS}$ = 0 V | — | — | ±10 | μA |
| Drain cutoff current | | $I_{DSS}$ | $V_{DS}$ = 60 V, $V_{GS}$ = 0 V | — | — | 100 | μA |
| Drain–source breakdown voltage | | $V_{(BR)\ DSS}$ | $I_D$ = 10 mA, $V_{GS}$ = 0 V | 60 | — | — | V |
| Gate threshold voltage | | $V_{th}$ | $V_{DS}$ = 10 V, $I_D$ = 1 mA | 0.8 | — | 2.0 | V |
| Drain–source ON-resistance | | $R_{DS\ (ON)}$ | $V_{GS}$ = 4 V, $I_D$ = 1 A (Note2) | — | 0.33 | 0.44 | Ω |
| | | | $V_{GS}$ = 10 V, $I_D$ = 1 A (Note2) | — | 0.22 | 0.30 | |
| Forward transfer admittance | | $\|Y_{fs}\|$ | $V_{DS}$ = 10 V, $I_D$ = 1 A (Note2) | 1.0 | 2.0 | — | S |
| Input capacitance | | $C_{iss}$ | $V_{DS}$ = 10 V, $V_{GS}$ = 0 V<br>f = 1 MHz | — | 150 | — | pF |
| Reverse transfer capacitance | | $C_{rss}$ | | — | 25 | — | |
| Output capacitance | | $C_{oss}$ | | — | 70 | — | |
| Switching time | Turn-on time | $t_{on}$ | $V_{DD}$ = 30 V, $I_D$ = 1 A<br>$V_{GS}$ = 0 ~10 V, $R_G$ = 50 Ω | — | 30 | — | ns |
| | Turn-off time | $t_{off}$ | | — | 150 | — | |
| Total Gate Charge | | $Q_g$ | $V_{DD}$ = 48 V, $V_{GS}$ = 10 V<br>$I_D$ = 2 A | — | 6.0 | — | nC |
| Gate-Source Charge | | $Q_{gs}$ | | — | 4.6 | — | |
| Gate-Drain Charge | | $Q_{gd}$ | | — | 1.4 | — | |
| Drain–source forward voltage | | $V_{DSF}$ | $I_D$ = -2 A, $V_{GS}$ = 0 V (Note2) | — | -1.0 | −1.5 | V |

Note 2: Pulse test

## Switching Time Test Circuit

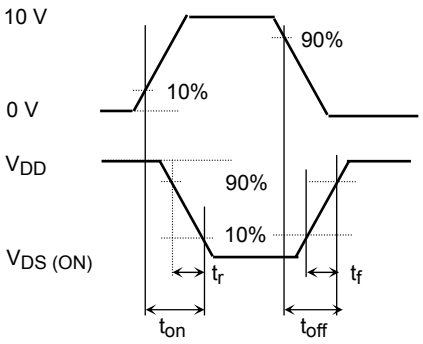
### (a) Test Circuit



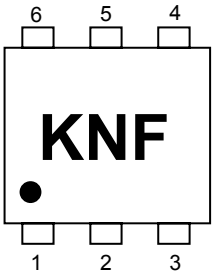

$V_{DD}$ = 30 V
$R_G$ = 50 Ω
D.U. ≦ 1%
$V_{IN}$: $t_r$, $t_f$ < 5 ns
Common Source
Ta = 25°C

### (b) $V_{IN}$

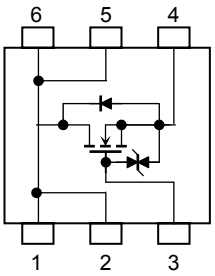
### (c) $V_{OUT}$




## Marking




## Equivalent Circuit (top view)



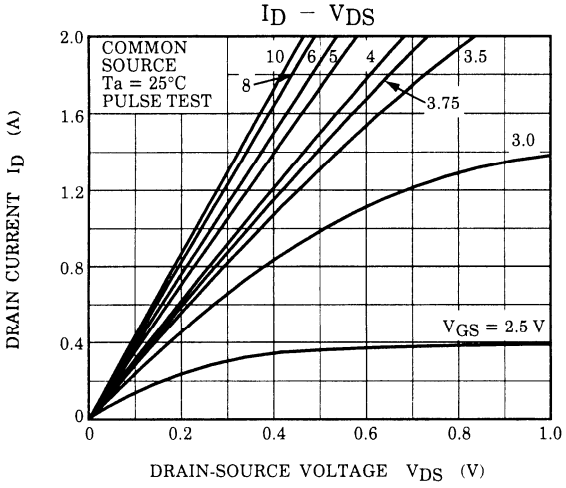

## Notice on Usage

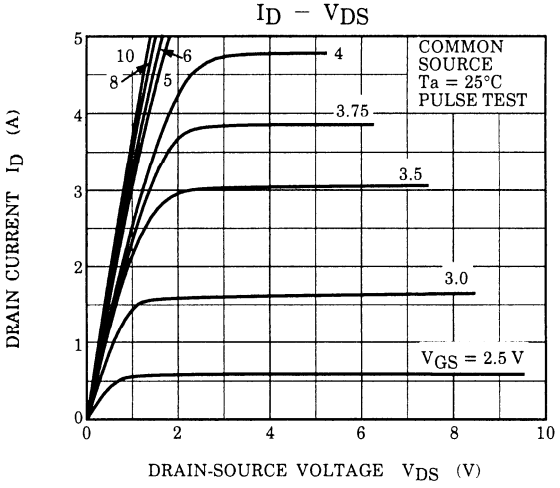
$V_{th}$ can be expressed as the voltage between gate and source when the low operating current value is $I_D$ = 1 mA for this product. For normal switching operation, $V_{GS\ (on)}$ requires a higher voltage than $V_{th}$ and $V_{GS\ (off)}$ requires a lower voltage than $V_{th}$. (The relationship can be established as follows: $V_{GS\ (off)} < V_{th} < V_{GS\ (on)}$.)

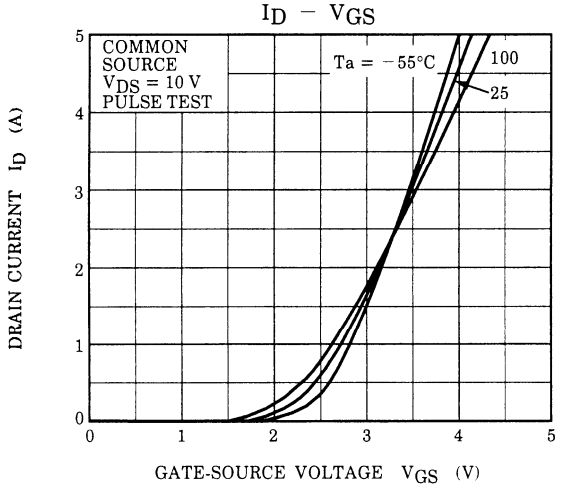
Take this into consideration when using the device.

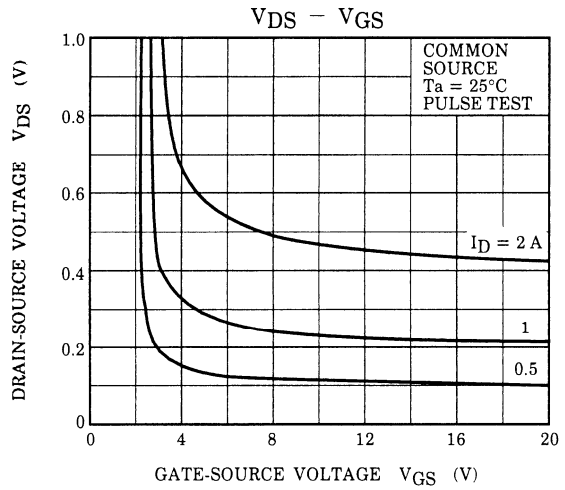
## Handling Precaution

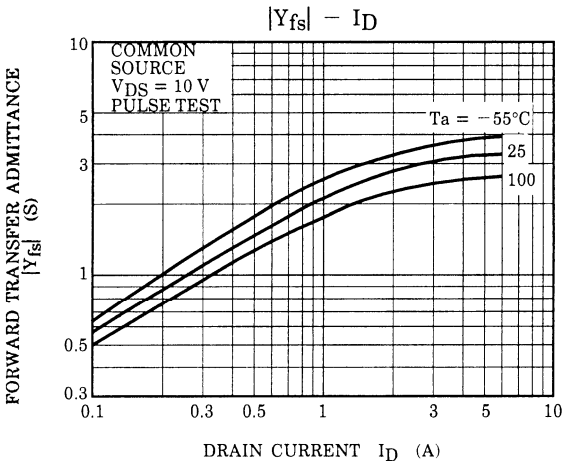
When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

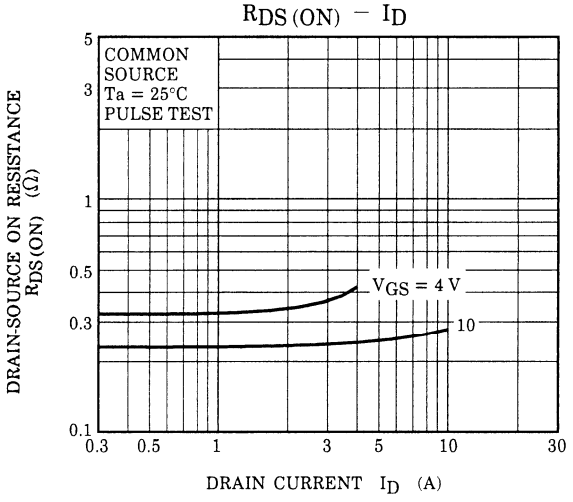

$I_D$ – $V_{DS}$
COMMON SOURCE
Ta = 25°C
PULSE TEST
10
8
6
5
4
3.5
3.75
3.0
$V_{GS}$ = 2.5 V
DRAIN CURRENT $I_D$ (A)
DRAIN-SOURCE VOLTAGE $V_{DS}$ (V)


$I_D$ – $V_{DS}$
COMMON SOURCE
Ta = 25°C
PULSE TEST
10
8
6
5
4
3.75
3.5
3.0
$V_{GS}$ = 2.5 V
DRAIN CURRENT $I_D$ (A)
DRAIN-SOURCE VOLTAGE $V_{DS}$ (V)

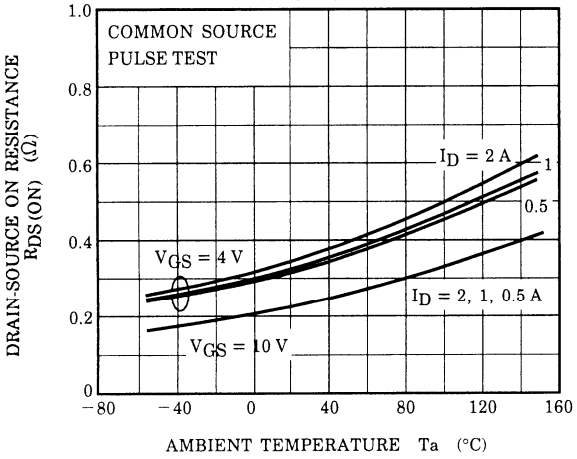

$I_D$ – $V_{GS}$
COMMON SOURCE
$V_{DS}$ = 10 V
PULSE TEST
Ta = −55°C
100
25
DRAIN CURRENT $I_D$ (A)
GATE-SOURCE VOLTAGE $V_{GS}$ (V)


$V_{DS}$ – $V_{GS}$
COMMON SOURCE
Ta = 25°C
PULSE TEST
$I_D$ = 2 A
1
0.5
DRAIN-SOURCE VOLTAGE $V_{DS}$ (V)
GATE-SOURCE VOLTAGE $V_{GS}$ (V)

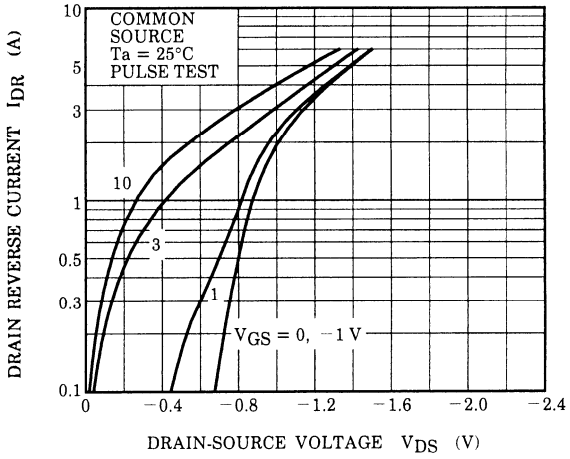

$|Y_{fs}|$ – $I_D$
COMMON SOURCE
$V_{DS}$ = 10 V
PULSE TEST
Ta = −55°C
25
100
FORWARD TRANSFER ADMITTANCE $|Y_{fs}|$ (S)
DRAIN CURRENT $I_D$ (A)


$R_{DS\,(ON)}$ – $I_D$
COMMON SOURCE
Ta = 25°C
PULSE TEST
$V_{GS}$ = 4 V
10
DRAIN-SOURCE ON RESISTANCE $R_{DS\,(ON)}$ (Ω)
DRAIN CURRENT $I_D$ (A)

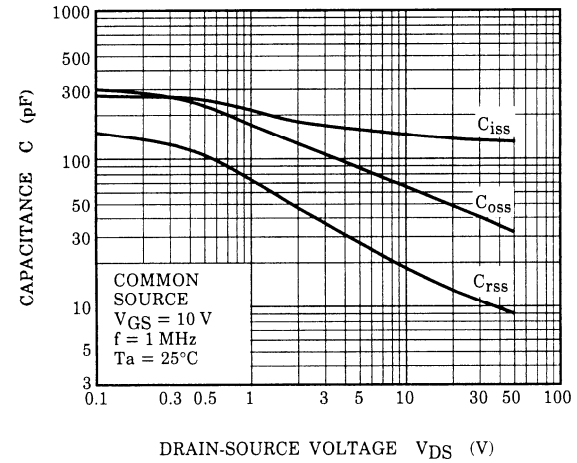
$R_{DS\,(ON)}$ – Ta



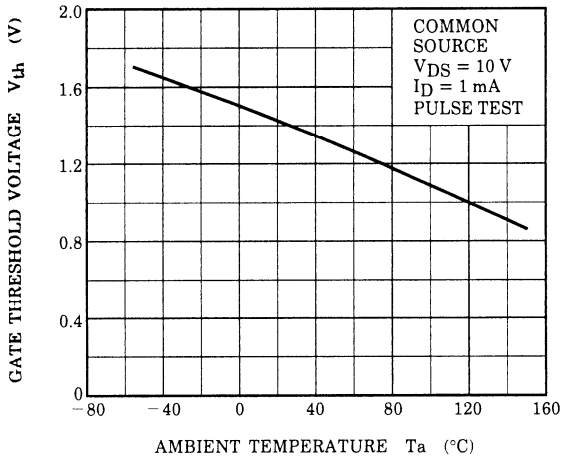

$I_{DR}$ – $V_{DS}$



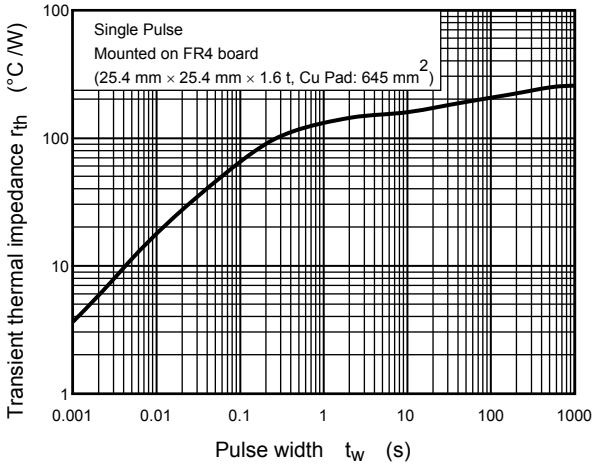

CAPACITANCE – $V_{DS}$



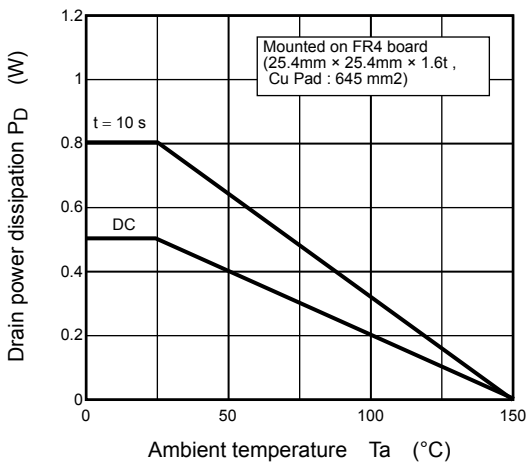

$V_{th}$ – Ta



$r_{th}$ – tW


Single Pulse
Mounted on FR4 board
(25.4 mm × 25.4 mm × 1.6 t, Cu Pad: 645 mm2)
Transient thermal impedance rth (°C /W)
100
100
10
1
0.001
0.01
0.1
1
10
100
1000
Pulse width tw (s)

$P_D$ – Ta


Mounted on FR4 board
(25.4mm × 25.4mm × 1.6t ,
Cu Pad : 645 mm2)
t = 10 s
DC
Drain power dissipation PD (W)
1.2
1
0.8
0.6
0.4
0.2
0
0
50
100
150
Ambient temperature Ta (°C)

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