

3A, Rad Hard, Positive, Ultra Low Dropout Regulator

ISL75051SEH

The ISL75051SEH is a radiation hardened low-voltage, high-current, single-output LDO specified for up to 3.0A of continuous output current. These devices operate over an input voltage range of 2.2V to 6.0V and are capable of providing output voltages of 0.8V to 5.0V adjustable based on resistor divider setting. Dropout voltages as low as 65mV can be realized using the device.

The OCP pin allows the short circuit output current limit threshold to be programmed by means of a resistor from the OCP pin to GND. The OCP setting range is from 0.5A minimum to 8.5A maximum. The resistor sets the constant current threshold for the output under fault conditions. The thermal shutdown disables the output if the device temperature exceeds the specified value. It subsequently enters an ON/OFF cycle until the fault is removed. The ENABLE feature allows the part to be placed into a low current shutdown mode that typically draws about 1µA. When enabled, the device operates with a typical low ground current of 11mA, which provides for operation with low quiescent power consumption.

The device is optimized for fast transient response and single event effects. This reduces the magnitude of SET seen on the output. Additional protection diodes and filters are not needed. The device is stable with tantalum capacitors as low as 47µF and provides excellent regulation all the way from no load to full load. Programmable soft-start allows the user to program the inrush current by means of the decoupling capacitor value used on the BYP pin.

Applications

- LDO Regulator for Space Application
- DSP, FPGA and µP Core Power Supplies
- Post-regulation of Switched Mode Power Supplies
- Down-hole Drilling

Features

- [DLA SMD#5962-11212](#)
 - Output Current Up to 3.0A at $T_j = +150^\circ\text{C}$
 - Output Accuracy $\pm 1.5\%$ over MIL Temp Range
 - Ultra Low Dropout:
 - 65mV Typ Dropout at 1.0A
 - 225mV Typ Dropout at 3.0A
 - Noise of $100\mu\text{V}_{\text{RMS}}$ from 300Hz to 300kHz
 - SET Mitigation with No Added Filtering/Diodes
 - Input Supply Range: 2.2V to 6.0V
 - Fast Load Transient Response
 - Shutdown Current of $1\mu\text{A}$ Typ
 - Output Adjustable Using External Resistors
 - PSRR 66dB Typ @ 1kHz
 - Enable and PGood Feature
 - Programmable Soft-start/Inrush Current Limiting
 - Adjustable Overcurrent Limit from 0.5A to 8.5A
 - Over-temperature Shutdown
 - Stable with 47µF Min Tantalum Capacitor
 - 18 Ld Ceramic Flatpack Package
 - Radiation Environment
 - High Dose Rate (50-300rad(Si)/s) 100krad(Si)
 - Low Dose Rate (0.01rad(Si)/s)..... 100krad(Si)*
- *Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer by wafer basis to 50 krad(Si) at low dose rate

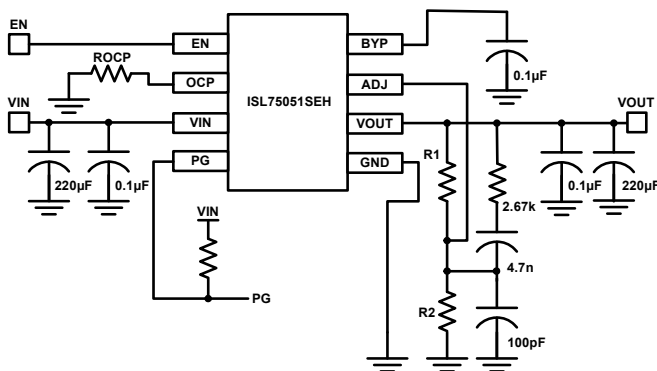


FIGURE 1. TYPICAL APPLICATION

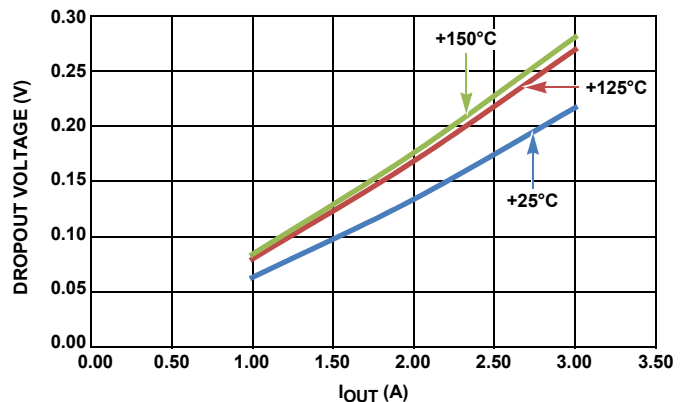
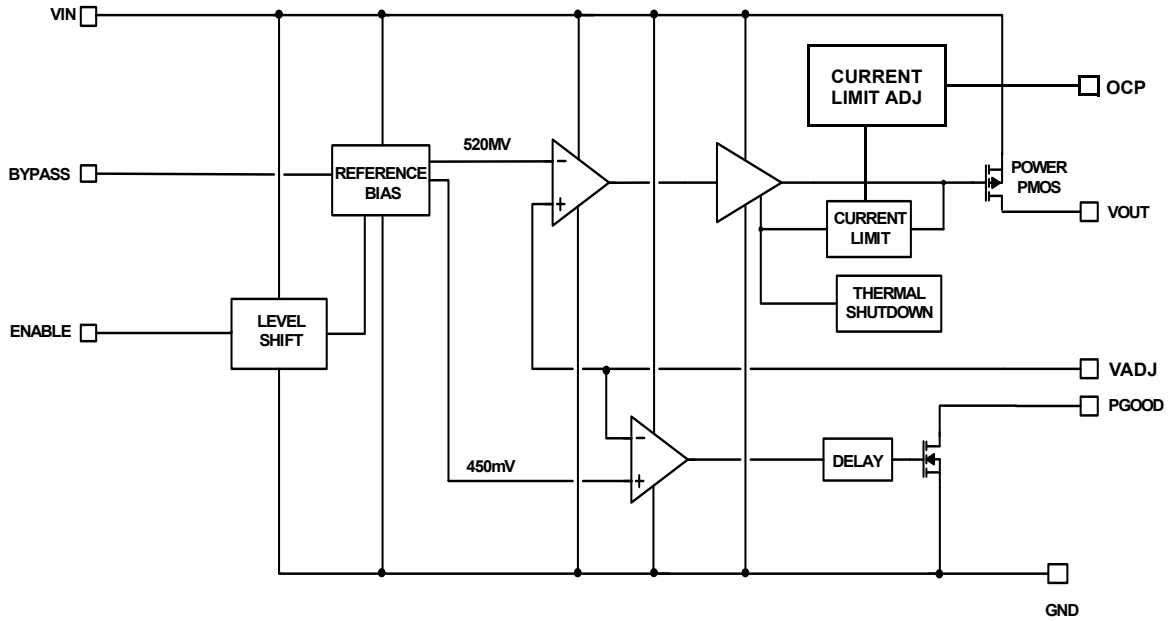


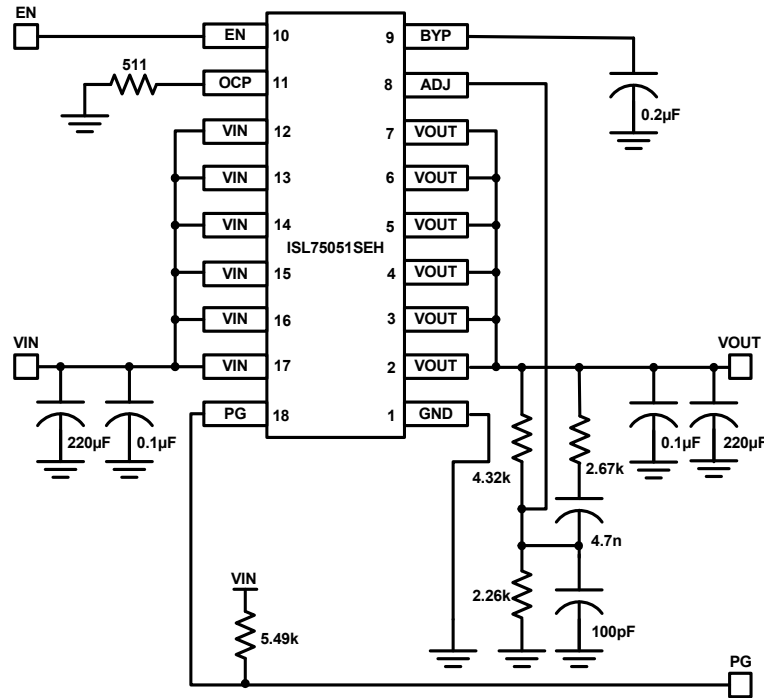
FIGURE 2. DROPOUT vs I_{OUT}

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Block Diagram

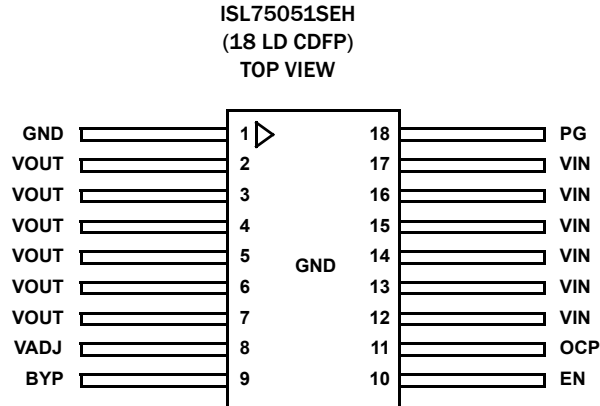


Typical Applications



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Pin Configuration



Pin Descriptions

| PIN NUMBER | PIN NAME | DESCRIPTION |
|--------------------------|-----------|--|
| 12, 13, 14 15, 16, 17 | V_{IN} | Input supply pins |
| 18 | PG | V_{OUT} in regulation signal. Logic low defines when V_{OUT} is not in regulation. Must be grounded if not used. |
| 1 | GND | GND pin |
| 2, 3, 4 5, 6, 7 | V_{OUT} | Output voltage pins |
| 8 | VADJ | VADJ pin allows V_{OUT} to be programmed with an external resistor divider. |
| 9 | BYP | To filter the internal reference, connect a 0.1 μ F capacitor from BYP pin to GND. |
| 10 | EN | V_{IN} independent chip enable. TTL and CMOS compatible. |
| 11 | OCP | Allows current limit to be programmed with an external resistor. |
| Top Lid | GND | The top lid is connected to GND pin of the package. |

Ordering Information

| ORDERING NUMBER | PART NUMBER (NOTES 1, 2) | TEMP RANGE (°C) | PACKAGE | PKG DWG. # |
|--------------------|--------------------------|-----------------|------------|------------|
| 5962R1121202VXC | ISL75051SEHVF | -55 to +125 | 18 Ld CDFP | K18.D |
| 5962R1121202V9A | ISL75051SEHVX | -55 to +125 | | |
| ISL75051SRHF/PROTO | ISL75051SRHF/PROTO | -55 to +125 | 18 Ld CDFP | K18.D |
| ISL75051SRHEVAL1Z | Evaluation Board | | | |

NOTES:

1. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. For Moisture Sensitivity Level (MSL), please see device information page for [ISL75051SEH](#). For more information on MSL please see Tech Brief [TB3363](#).

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Absolute Maximum Ratings

| | |
|--|-----------------|
| V_{IN} Relative to GND (Note 3) | -0.3 to +6.7V |
| V_{OUT} Relative to GND (Note 3) | -0.3 to +6.7V |
| PG, EN, OCP/ADJ Relative to GND (Note 3) | -0.3 to +6.7VDC |
| Junction Temperature (T_J) | +175°C |

Recommended Operating Conditions (Note 4)

| | |
|---|-----------------|
| Ambient Temperature Range (T_A) | -55°C to +125°C |
| Junction Temperature (T_J) (Note 3) | +150°C |
| V_{IN} Relative to GND | 2.2V to 6.0V |
| V_{OUT} Range | 0.8V to 5.0V |
| PG, EN, OCP/ADJ relative to GND | 0V to +6.0V |

Thermal Information

| | | |
|---------------------------------|----------------------|----------------------|
| Thermal Resistance (Typical) | θ_{JA} (°C/W) | θ_{JC} (°C/W) |
| 18 Ld CDFP Package (Notes 7, 8) | 28 | 4 |
| Storage Temperature Range | -65°C to +150°C | |

Radiation Information

| | |
|---|----------------------------|
| Maximum Total Dose | |
| Dose Rate = 50-300rad(Si)/s | 100krad (Si) |
| Dose Rate = 0.01rad(Si)/s (Note 5) | 100krad (Si) |
| SEE Performance | |
| SET ($V_{OUT} < \pm 5\%$ During Events) (Note 6) | .86MeV•cm ² /mg |
| SEL/SEB (No Latchup/Burnout) | .86MeV•cm ² /mg |

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- Extended operation at these conditions may compromise reliability. Exceeding these limits will result in damage. Recommended operating conditions define limits where specifications are guaranteed.
- Refer to "Thermal Guidelines" on page 15.
- Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer by wafer basis to 50 krad(Si) at low dose rate.
- Specify EVAL test conditions for SET/SEB/SEL here.
- θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief [TB379](#)
- For θ_{JC} , the "case temp" location is the center of the package underside.
- The device can work down to $V_{OUT} = 0.8V$; however, the SET performance of $< \pm 5\%$ at LET = 86MeV.cm²/mg is guaranteed at $V_{OUT} = >1.5V$ only. SET tests performed with 220µF 10V 25mΩ and 0.1µF CDR04 capacitor on the input and output.

Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the following specified conditions:

$V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 220\mu F$ 25mΩ and 0.1µF X7R, $T_J = +25^\circ C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature (see Note 13). **Boldface limits apply over the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines guaranteed limits.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 10) | TYP | MAX (Note 10) | UNITS |
|----------------------------|-----------|---|---------------|-------|---------------|-------|
| DC CHARACTERISTICS | | | | | | |
| DC Output Voltage Accuracy | V_{OUT} | V_{OUT} Resistor adjust to 0.52V, 1.5V and 1.8V | | | | |
| | | $2.2V < V_{IN} < 3.6V$; $0A < I_{LOAD} < 3.0A$ | -1.5 | 0.2 | 1.5 | % |
| | | V_{OUT} Resistor adjust to 5.0V | | | | |
| | | $V_{OUT} + 0.4V < V_{IN} < 6.0V$; $0A < I_{LOAD} < 3.0A$ | -1.5 | 0.2 | 1.5 | % |
| VADJ Pin Voltage | V_{ADJ} | $2.2V < V_{IN} < 6.0V$; $I_{LOAD} = 0A$ | 514.8 | 520 | 525.2 | mV |
| BYP Pin | V_{BYP} | $2.2V < V_{IN} < 6.0V$; $I_{LOAD} = 0A$ | | 520 | | mV |
| DC Input Line Regulation | | $2.2V < V_{IN} < 3.6V$, $V_{OUT} = 1.5V$, +25°C and -55°C (Note 11) | | 1.13 | 3.5 | mV |
| DC Input Line Regulation | | $2.2V < V_{IN} < 3.6V$, $V_{OUT} = 1.5V$, +125°C (Note 11) | | 1.13 | 8.0 | mV |
| DC Input Line Regulation | | $2.2V < V_{IN} < 3.6V$, $V_{OUT} = 1.8V$, +25°C and -55°C (Note 11) | | 1.62 | 3.5 | mV |
| DC Input Line Regulation | | $2.2V < V_{IN} < 3.6V$, $V_{OUT} = 1.8V$, +125°C (Note 11) | | 1.62 | 10.5 | mV |
| DC Input Line Regulation | | $V_{OUT} + 0.4V < V_{IN} < 6.0V$, $V_{OUT} = 5.0V$ (Note 11) | | 12.50 | 20.0 | mV |
| DC Output Load Regulation | | $V_{OUT} = 1.5V$; $0A < I_{LOAD} < 3.0A$, $V_{IN} = V_{OUT} + 0.4V$ (Note 11) | -4.0 | -0.8 | -0.1 | mV |
| DC Output Load Regulation | | $V_{OUT} = 1.8V$; $0A < I_{LOAD} < 3.0A$, $V_{IN} = V_{OUT} + 0.4V$ (Note 11) | -4.0 | -1.2 | -0.05 | mV |

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Electrical Specifications Unless otherwise noted, all parameters are guaranteed over the following specified conditions: $V_{IN} = V_{OUT} + 0.4V$, $V_{OUT} = 1.8V$, $C_{IN} = C_{OUT} = 220\mu F$ 25m Ω and 0.1 μF X7R, $T_J = +25^\circ C$, $I_L = 0A$. Applications must follow thermal guidelines of the package to determine worst-case junction temperature (see Note 13). **Boldface limits apply over the operating temperature range, -55°C to +125°C.** Pulse load techniques used by ATE to ensure $T_J = T_A$ defines guaranteed limits. (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 10) | TYP | MAX (Note 10) | UNITS |
|--|------------|--|------------------|------------|------------------|---------------|
| DC Output Load Regulation | | $V_{OUT} = 5.0V$; $0A < I_{LOAD} < 3.0A$, $V_{IN} = V_{OUT} + 0.4V$ (Note 11) | -15.0 | -6.0 | -0.05 | mV |
| VADJ Input Current | | $V_{ADJ} = 0.5V$ | | | 1 | μA |
| Ground Pin Current | I_Q | $V_{OUT} = 1.5V$; $I_{LOAD} = 0A$, $V_{IN} = 2.2V$ | | 11 | 12 | mA |
| Ground Pin Current | I_Q | $V_{OUT} = 5.0V$; $I_{LOAD} = 0A$, $V_{IN} = 6.0V$ | | 16 | 18 | mA |
| Ground Pin Current | I_Q | $V_{OUT} = 1.5V$; $I_{LOAD} = 3.0A$, $V_{IN} = 2.2V$ | | 11 | 13 | mA |
| Ground Pin Current | I_Q | $V_{OUT} = 5.0V$; $I_{LOAD} = 3.0A$, $V_{IN} = 6.0V$ | | 16 | 18 | mA |
| Ground Pin Current in Shutdown | I_{SHDN} | ENABLE Pin = 0V, $V_{IN} = 6.0V$ | | 1 | 10 | μA |
| Dropout Voltage | V_{DO} | $I_{LOAD} = 1.0A$, $V_{OUT} = 2.5V$ (Note 12) | | 65 | 100 | mV |
| Dropout Voltage | V_{DO} | $I_{LOAD} = 2.0A$, $V_{OUT} = 2.5V$ (Note 12) | | 140 | 200 | mV |
| Dropout Voltage | V_{DO} | $I_{LOAD} = 3.0A$, $V_{OUT} = 2.5V$ (Note 12) | | 225 | 300 | mV |
| Output Short Circuit Current | ISCL | $V_{OUT} = 0V$, $V_{IN} = 2.2V$, $R_{SET} = 5.11k$ | | 1.1 | | A |
| Output Short Circuit Current | ISCL | $V_{OUT} = 0V$, $V_{IN} = 6.0V$, $R_{SET} = 5.11k$ | | 1.2 | | A |
| Output Short Circuit Current | ISCH | $V_{OUT} = 0V$, $V_{IN} = 2.2V$, $R_{SET} = 511\Omega$ | | 5.7 | | A |
| Output Short Circuit Current | ISCH | $V_{OUT} = 0V$, $V_{IN} = 6.0V$, $R_{SET} = 511\Omega$ | | 6.2 | | A |
| Thermal Shutdown Temperature | TSD | $V_{OUT} + 0.4V < V_{IN} < 6.0V$ | | 175 | | $^\circ C$ |
| Thermal Shutdown Hysteresis (Rising Threshold) | TSDn | $V_{OUT} + 0.4V < V_{IN} < 6.0V$ | | 25 | | $^\circ C$ |
| AC CHARACTERISTICS | | | | | | |
| Input Supply Ripple Rejection | PSRR | $V_{P-P} = 300mV$, $f = 1kHz$, $I_{LOAD} = 3A$; $V_{IN} = 2.5V$, $V_{OUT} = 1.8V$ | 42 | 66 | | dB |
| Input Supply Ripple Rejection | PSRR | $V_{P-P} = 300mV$, $f = 100kHz$, $I_{LOAD} = 3A$; $V_{IN} = 2.5V$, $V_{OUT} = 1.8V$ | | 30 | | dB |
| Phase Margin | PM | $V_{OUT} = 1.8V$, $C_L = 220\mu F$ Tantalum | | 70 | | dB |
| Gain Margin | GM | $V_{OUT} = 1.8V$, $C_L = 220\mu F$ Tantalum | | 16 | | dB |
| Output Noise Voltage | | $I_{LOAD} = 10mA$, $BW = 300Hz < f < 300kHz$, BYPASS to GND capacitor = 0.2 μF | | 100 | | μV_{RMS} |
| DEVICE START-UP CHARACTERISTICS: ENABLE PIN | | | | | | |
| Rising Threshold | | $2.2V < V_{IN} < 6.0V$ | 0.6 | 0.9 | 1.2 | V |
| Falling Threshold | | $2.2V < V_{IN} < 6.0V$ | 0.47 | 0.7 | 0.9 | V |
| Enable Pin Leakage Current | | $V_{IN} = 6.0V$, EN = 6.0V | | | 1 | μA |
| Enable Pin Propagation Delay | | $V_{IN} = 2.2V$, EN rise to I_{OUT} rise | 225 | 300 | 450 | μs |
| Enable Pin Turn-on Delay | | $V_{IN} = 2.2V$, $V_{OUT} = 1.8V$, $I_{LOAD} = 1A$, $C_{OUT} =$ 220 μF , $C_{BYP} = 0.2\mu F$ | | 6 | | ms |
| Enable Pin Turn-on Delay | | $V_{IN} = 2.2V$, $V_{OUT} = 1.8V$, $I_{LOAD} = 1A$, $C_{OUT} = 47\mu F$, $C_{BYP} = 0.2\mu F$ | | 50 | | μs |
| Hysteresis | | Must be independent of V_{IN} ; $2.2V < V_{IN} < 6.0V$ | 90 | 200 | 318 | mV |

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| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 10) | TYP | MAX (Note 10) | UNITS |
|--|--------|-----------------------------------|------------------|------|------------------|-------------------|
| DEVICE START-UP CHARACTERISTICS: PG PIN | | | | | | |
| PG Rising Threshold | | 2.2V < V _{IN} < 6.0V | 85 | 90 | 96 | % |
| PG Falling Threshold | | 2.2V < V _{IN} < 6.0V | 82 | 88 | 93 | % |
| PG Hysteresis | | 2.2V < V _{IN} < 6.0V | 2.5 | 3.2 | 4.0 | %V _{OUT} |
| PG Low Voltage | | I _{SINK} = 1mA | | 35 | 100 | mV |
| PG Low Voltage | | I _{SINK} = 6mA | | 185 | 400 | mV |
| PG Leakage Current | | V _{IN} = 6.0V, PG = 6.0V | | 0.01 | 1 | μA |

NOTES:

- Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C and +125°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
- Line and Load Regulation done under pulsed condition for T < 10ms.
- Dropout is defined as the difference between the supply V_{IN} and V_{OUT}, when the supply produces a 2% drop in V_{OUT} from its nominal value. Data measured within a 3ms period.
- Please refer to "Applications Information" on page 14 of the datasheet and Tech Brief [TB379](#).

High Dose Rate Post Radiation Characteristics T_A = +25°C, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. (see Note 14). **These are not limits nor are they guaranteed.**

| ITEM # | DESCRIPTION | CONDITION | 0k RAD | 100k RAD | UNITS |
|--------|----------------------------|---|----------|----------|-------|
| 1 | DC Output Voltage Accuracy | V _{OUT} = 0.52V; V _{IN} = 2.2V; I _{OUT} = 0A | 0.520575 | 0.520975 | V |
| 2 | DC Output Voltage Accuracy | V _{OUT} = 0.52V; V _{IN} = 2.2V; I _{OUT} = 3A | 0.520000 | 0.520300 | V |
| 3 | DC Output Voltage Accuracy | V _{OUT} = 0.52V; V _{IN} = 3.6V; I _{OUT} = 0A | 0.520650 | 0.520813 | V |
| 4 | DC Output Voltage Accuracy | V _{OUT} = 0.52V; V _{IN} = 3.6V; I _{OUT} = 3A | 0.519963 | 0.520113 | V |
| 5 | DC Output Voltage Accuracy | V _{OUT} = 1.5V; V _{IN} = 2.2V; I _{OUT} = 0A | 1.500813 | 1.501325 | V |
| 6 | DC Output Voltage Accuracy | V _{OUT} = 1.5V; V _{IN} = 2.2V; I _{OUT} = 3A | 1.499250 | 1.499800 | V |
| 7 | DC Output Voltage Accuracy | V _{OUT} = 1.5V; V _{IN} = 3.6V; I _{OUT} = 0A | 1.500550 | 1.500938 | V |
| 8 | DC Output Voltage Accuracy | V _{OUT} = 1.5V; V _{IN} = 3.6V; I _{OUT} = 3A | 1.499075 | 1.499388 | V |
| 9 | DC Output Voltage Accuracy | V _{OUT} = 1.8V; V _{IN} = 2.2V; I _{OUT} = 0A | 1.802288 | 1.803613 | V |
| 10 | DC Output Voltage Accuracy | V _{OUT} = 1.8V; V _{IN} = 2.2V; I _{OUT} = 3A | 1.800900 | 1.801825 | V |
| 11 | DC Output Voltage Accuracy | V _{OUT} = 1.8V; V _{IN} = 3.6V; I _{OUT} = 0A | 1.802900 | 1.803338 | V |
| 12 | DC Output Voltage Accuracy | V _{OUT} = 1.8V; V _{IN} = 3.6V; I _{OUT} = 3A | 1.801175 | 1.801550 | V |
| 13 | DC Output Voltage Accuracy | V _{OUT} = 5.0V; V _{IN} = 5.4V; I _{OUT} = 0A | 5.018250 | 5.018850 | V |
| 14 | DC Output Voltage Accuracy | V _{OUT} = 5.0V; V _{IN} = 5.4V; I _{OUT} = 3A | 5.013050 | 5.013450 | V |
| 15 | DC Output Voltage Accuracy | V _{OUT} = 5.0V; V _{IN} = 6.0V; I _{OUT} = 0A | 5.023838 | 5.024188 | V |
| 16 | DC Output Voltage Accuracy | V _{OUT} = 5.0V; V _{IN} = 6.0V; I _{OUT} = 3A | 5.016550 | 5.016763 | V |
| 17 | VADJ Pin Voltage | V _{OUT} = 0.52V; V _{IN} = 2.2V | 0.520625 | 0.521000 | V |
| 18 | VADJ Pin Voltage | V _{OUT} = 0.52V; V _{IN} = 3.6V | 0.520700 | 0.520863 | V |
| 19 | VADJ Pin Voltage | V _{OUT} = 0.52V; V _{IN} = 5.5V | 0.521125 | 0.521200 | V |
| 20 | VADJ Pin Voltage | V _{OUT} = 1.5V; V _{IN} = 2.2V | 0.520800 | 0.521013 | V |
| 21 | VADJ Pin Voltage | V _{OUT} = 1.5V; V _{IN} = 3.6V | 0.520688 | 0.520838 | V |

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High Dose Rate Post Radiation Characteristics $T_A = +25^\circ\text{C}$, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 50 to 300rad(SI)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. (see Note 14). These are not limits nor are they guaranteed. (Continued)

| ITEM # | DESCRIPTION | CONDITION | 0k RAD | 100k RAD | UNITS |
|--------|--------------------------------|--|------------|------------|---------------|
| 22 | VADJ Pin Voltage | $V_{OUT} = 1.5\text{V}; V_{IN} = 5.5\text{V}$ | 0.521025 | 0.521113 | V |
| 23 | VADJ Pin Voltage | $V_{OUT} = 1.8\text{V}; V_{IN} = 2.2\text{V}$ | 0.520563 | 0.520925 | V |
| 24 | VADJ Pin Voltage | $V_{OUT} = 1.8\text{V}; V_{IN} = 3.6\text{V}$ | 0.520688 | 0.520838 | V |
| 25 | VADJ Pin Voltage | $V_{OUT} = 1.8\text{V}; V_{IN} = 5.5\text{V}$ | 0.521038 | 0.521100 | V |
| 26 | VADJ Pin Voltage | $V_{OUT} = 5.0\text{V}; V_{IN} = 5.4\text{V}$ | 0.521000 | 0.521088 | V |
| 27 | VADJ Pin Voltage | $V_{OUT} = 5.0\text{V}; V_{IN} = 6.0\text{V}$ | 0.521575 | 0.521625 | V |
| 28 | DC Input Line Regulation | $2.2\text{V} < V_{IN} < 3.6\text{V}, V_{OUT} = 1.5\text{V}$ | -0.257100 | -0.408960 | mV |
| 29 | DC Input Line Regulation | $2.2\text{V} < V_{IN} < 3.6\text{V}, V_{OUT} = 1.8\text{V}$ | 0.611613 | -0.281990 | mV |
| 30 | DC Input Line Regulation | $V_{OUT} + 0.4\text{V} < V_{IN} < 6.0\text{V}, V_{OUT} = 5.0\text{V}$ | 5.600700 | 5.313688 | mV |
| 31 | DC Output Load Regulation | $V_{OUT} = 1.5\text{V}; 0\text{A} < I_{LOAD} < 3.0\text{A}, V_{IN} = V_{OUT} + 0.4\text{V}$ | -1.559875 | -1.549760 | mV |
| 32 | DC Output Load Regulation | $V_{OUT} = 1.8\text{V}; 0\text{A} < I_{LOAD} < 3.0\text{A}, V_{IN} = V_{OUT} + 0.4\text{V}$ | -1.390263 | -1.784640 | mV |
| 33 | DC Output Load Regulation | $V_{OUT} = 5.0\text{V}; 0\text{A} < I_{LOAD} < 3.0\text{A}, V_{IN} = V_{OUT} + 0.4\text{V}$ | -5.201513 | -5.418710 | mV |
| 34 | Feedback Input Current | $V_{ADJ} = 0.5\text{V}$ | -0.036650 | -0.040980 | μA |
| 35 | Ground Pin Current | $V_{OUT} = 1.5\text{V}; I_{LOAD} = 0\text{A}, V_{IN} = 2.2\text{V}$ | 10.715763 | 10.758810 | mA |
| 36 | Ground Pin Current | $V_{OUT} = 1.5\text{V}; I_{LOAD} = 3.0\text{A}, V_{IN} = 2.2\text{V}$ | 12.016163 | 12.067510 | mA |
| 37 | Ground Pin Current | $V_{OUT} = 5.0\text{V}; I_{LOAD} = 0\text{A}, V_{IN} = 6.0\text{V}$ | 15.796488 | 15.781190 | mA |
| 38 | Ground Pin Current | $V_{OUT} = 5.0\text{V}; I_{LOAD} = 3.0\text{A}, V_{IN} = 6.0\text{V}$ | 17.178913 | 17.166440 | mA |
| 39 | Ground Pin Current in Shutdown | ENABLE Pin = 0V, $V_{IN} = 6.0\text{V}$ | 0.811625 | 0.752100 | μA |
| 40 | Dropout Voltage | $I_{LOAD} = 1.0\text{A}, V_{OUT} = 2.5\text{V}$ | 62.588600 | 63.660340 | mV |
| 41 | Dropout Voltage | $I_{LOAD} = 2.0\text{A}, V_{OUT} = 2.5\text{V}$ | 134.520040 | 135.703500 | mV |
| 42 | Dropout Voltage | $I_{LOAD} = 3.0\text{A}, V_{OUT} = 2.5\text{V}$ | 215.603360 | 216.651900 | mV |
| 43 | Output Short Circuit Current | $V_{OUT} = 0\text{V}, V_{IN} = 2.2\text{V}, R_{SET} = 5.11\text{k}$ | 1.204063 | 1.323238 | A |
| 44 | Output Short Circuit Current | $V_{OUT} = 0\text{V}, V_{IN} = 2.2\text{V}, R_{SET} = 511\Omega$ | 5.903613 | 6.058613 | A |
| 45 | Output Short Circuit Current | $V_{OUT} = 0\text{V}, V_{IN} = 6.0\text{V}, R_{SET} = 5.11\text{k}$ | 1.333325 | 1.439638 | A |
| 46 | Output Short Circuit Current | $V_{OUT} = 0\text{V}, V_{IN} = 6.0\text{V}, R_{SET} = 511\Omega$ | 6.389913 | 6.635563 | A |
| 47 | PSRR | $V_{P-P} = 300\text{mV}, f = 1\text{kHz}, I_{LOAD} = 3\text{A}; V_{IN} = 2.5\text{V}, V_{OUT} = 1.8\text{V}$ | 65.428638 | 66.410750 | db |
| 48 | Enable Rising Threshold | $V_{IN} = 2.2\text{V}$ | 0.863700 | 0.824150 | V |
| 49 | Enable Rising Threshold | $V_{IN} = 6.0\text{V}$ | 0.911300 | 0.875263 | V |
| 50 | Enable Falling Threshold | $V_{IN} = 2.2\text{V}$ | 0.678400 | 0.636800 | V |
| 51 | Enable Falling Threshold | $V_{IN} = 6.0\text{V}$ | 0.724475 | 0.684400 | V |
| 52 | Enable Pin Leakage Current | $V_{IN} = 6.0\text{V}, \text{EN} = 0\text{V}$ | -0.028513 | -0.029950 | μA |
| 53 | Enable Pin Leakage Current | $V_{IN} = 6.0\text{V}, \text{EN} = 6.0\text{V}$ | -0.030638 | -0.038110 | μA |
| 54 | Enable Hysteresis | $V_{IN} = 2.2\text{V}$ | 185.370000 | 187.374000 | mV |
| 55 | Enable Hysteresis | $V_{IN} = 6.0\text{V}$ | 186.874000 | 190.881600 | mV |
| 56 | Enable Pin Propagation Delay | $V_{IN} = 2.2\text{V}, \text{EN rise to } I_{OUT} \text{ rise}$ | 305.015280 | 290.839200 | μs |
| 57 | PG Rising Threshold | $V_{IN} = 2.2\text{V}$ | 89.542938 | 88.811230 | % |
| 58 | PG Rising Threshold | $V_{IN} = 6.0\text{V}$ | 91.083838 | 90.396230 | % |
| 59 | PG Falling Threshold | $V_{IN} = 2.2\text{V}$ | 86.793125 | 86.074360 | % |

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High Dose Rate Post Radiation Characteristics $T_A = +25^\circ\text{C}$, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 50 to 300rad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. (see Note 14). These are not limits nor are they guaranteed. (Continued)

| ITEM # | DESCRIPTION | CONDITION | 0k RAD | 100k RAD | UNITS |
|--------|----------------------|---|------------|------------|---------------|
| 60 | PG Falling Threshold | $V_{IN} = 6.0\text{V}$ | 87.840925 | 87.165790 | % |
| 61 | PG Hysteresis | $V_{IN} = 2.2\text{V}$ | 2.749825 | 2.736875 | % |
| 62 | PG Hysteresis | $V_{IN} = 6.0\text{V}$ | 3.242925 | 3.230450 | % |
| 63 | PG Low Voltage | $I_{SINK} = 1\text{mA}$ | 31.426938 | 31.570940 | mV |
| 64 | PG Low Voltage | $I_{SINK} = 6\text{mA}$ | 177.107950 | 178.578800 | mV |
| 65 | PG Leakage Current | $V_{IN} = 6.0\text{V}$, $PG = 6.0\text{V}$ | -0.001550 | -0.001560 | μA |

Low Dose Rate Post Radiation Characteristics $T_A = +25^\circ\text{C}$, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. (see Note 14). These are not limits nor are they guaranteed.

| ITEM # | DESCRIPTION | CONDITION | 0k RAD | 50k RAD | 100k RAD | UNITS |
|--------|----------------------------|---|-----------|-----------|----------|-------|
| 1 | DC Output Voltage Accuracy | $V_{OUT} = 0.52\text{V}$; $V_{IN} = 2.2\text{V}$; $I_{OUT} = 0\text{A}$ | 0.521050 | 0.521150 | 0.521600 | V |
| 2 | DC Output Voltage Accuracy | $V_{OUT} = 0.52\text{V}$; $V_{IN} = 2.2\text{V}$; $I_{OUT} = 3\text{A}$ | 0.520500 | 0.520600 | 0.520950 | V |
| 3 | DC Output Voltage Accuracy | $V_{OUT} = 0.52\text{V}$; $V_{IN} = 3.6\text{V}$; $I_{OUT} = 0\text{A}$ | 0.521050 | 0.521350 | 0.521750 | V |
| 4 | DC Output Voltage Accuracy | $V_{OUT} = 0.52\text{V}$; $V_{IN} = 3.6\text{V}$; $I_{OUT} = 3\text{A}$ | 0.520450 | 0.520600 | 0.521000 | V |
| 5 | DC Output Voltage Accuracy | $V_{OUT} = 1.5\text{V}$; $V_{IN} = 2.2\text{V}$; $I_{OUT} = 0\text{A}$ | 1.502450 | 1.503050 | 1.503200 | V |
| 6 | DC Output Voltage Accuracy | $V_{OUT} = 1.5\text{V}$; $V_{IN} = 2.2\text{V}$; $I_{OUT} = 3\text{A}$ | 1.500950 | 1.501400 | 1.502100 | V |
| 7 | DC Output Voltage Accuracy | $V_{OUT} = 1.5\text{V}$; $V_{IN} = 3.6\text{V}$; $I_{OUT} = 0\text{A}$ | 1.501950 | 1.502900 | 1.503650 | V |
| 8 | DC Output Voltage Accuracy | $V_{OUT} = 1.5\text{V}$; $V_{IN} = 3.6\text{V}$; $I_{OUT} = 3\text{A}$ | 1.500500 | 1.501400 | 1.502150 | V |
| 9 | DC Output Voltage Accuracy | $V_{OUT} = 1.8\text{V}$; $V_{IN} = 2.2\text{V}$; $I_{OUT} = 0\text{A}$ | 1.804150 | 1.805050 | 1.806100 | V |
| 10 | DC Output Voltage Accuracy | $V_{OUT} = 1.8\text{V}$; $V_{IN} = 2.2\text{V}$; $I_{OUT} = 3\text{A}$ | 1.802850 | 1.803650 | 1.804800 | V |
| 11 | DC Output Voltage Accuracy | $V_{OUT} = 1.8\text{V}$; $V_{IN} = 3.6\text{V}$; $I_{OUT} = 0\text{A}$ | 1.804450 | 1.805850 | 1.806600 | V |
| 12 | DC Output Voltage Accuracy | $V_{OUT} = 1.8\text{V}$; $V_{IN} = 3.6\text{V}$; $I_{OUT} = 3\text{A}$ | 1.802850 | 1.804100 | 1.804900 | V |
| 13 | DC Output Voltage Accuracy | $V_{OUT} = 5.0\text{V}$; $V_{IN} = 5.4\text{V}$; $I_{OUT} = 0\text{A}$ | 5.022600 | 5.027250 | 5.028500 | V |
| 14 | DC Output Voltage Accuracy | $V_{OUT} = 5.0\text{V}$; $V_{IN} = 5.4\text{V}$; $I_{OUT} = 3\text{A}$ | 5.017200 | 5.022200 | 5.023350 | V |
| 15 | DC Output Voltage Accuracy | $V_{OUT} = 5.0\text{V}$; $V_{IN} = 6.0\text{V}$; $I_{OUT} = 0\text{A}$ | 5.028050 | 5.032500 | 5.034350 | V |
| 16 | DC Output Voltage Accuracy | $V_{OUT} = 5.0\text{V}$; $V_{IN} = 6.0\text{V}$; $I_{OUT} = 3\text{A}$ | 5.020950 | 5.025500 | 5.027050 | V |
| 17 | VADJ Pin Voltage | $V_{OUT} = 0.52\text{V}$; $V_{IN} = 2.2\text{V}$ | 0.521150 | 0.521300 | 0.521600 | V |
| 18 | VADJ Pin Voltage | $V_{OUT} = 0.52\text{V}$; $V_{IN} = 3.6\text{V}$ | 0.521150 | 0.521400 | 0.521700 | V |
| 19 | VADJ Pin Voltage | $V_{OUT} = 0.52\text{V}$; $V_{IN} = 5.5\text{V}$ | 0.521550 | 0.521800 | 0.522150 | V |
| 20 | VADJ Pin Voltage | $V_{OUT} = 1.5\text{V}$; $V_{IN} = 2.2\text{V}$ | 0.521400 | 0.521500 | 0.521550 | V |
| 21 | VADJ Pin Voltage | $V_{OUT} = 1.5\text{V}$; $V_{IN} = 3.6\text{V}$ | 0.521150 | 0.521400 | 0.521700 | V |
| 22 | VADJ Pin Voltage | $V_{OUT} = 1.5\text{V}$; $V_{IN} = 5.5\text{V}$ | 0.521450 | 0.521800 | 0.522050 | V |
| 23 | VADJ Pin Voltage | $V_{OUT} = 1.8\text{V}$; $V_{IN} = 2.2\text{V}$ | 0.521050 | 0.521200 | 0.521550 | V |
| 24 | VADJ Pin Voltage | $V_{OUT} = 1.8\text{V}$; $V_{IN} = 3.6\text{V}$ | 0.521150 | 0.521400 | 0.521750 | V |
| 25 | VADJ Pin Voltage | $V_{OUT} = 1.8\text{V}$; $V_{IN} = 5.5\text{V}$ | 0.521450 | 0.521800 | 0.522000 | V |
| 26 | VADJ Pin Voltage | $V_{OUT} = 5.0\text{V}$; $V_{IN} = 5.4\text{V}$ | 0.521400 | 0.521800 | 0.521950 | V |
| 27 | VADJ Pin Voltage | $V_{OUT} = 5.0\text{V}$; $V_{IN} = 6.0\text{V}$ | 0.522000 | 0.522250 | 0.522600 | V |
| 28 | DC Input Line Regulation | $2.2\text{V} < V_{IN} < 3.6\text{V}$, $V_{OUT} = 1.5\text{V}$ | -0.284500 | -0.176150 | 0.158400 | mV |
| 29 | DC Input Line Regulation | $2.2\text{V} < V_{IN} < 3.6\text{V}$, $V_{OUT} = 1.8\text{V}$ | 0.520000 | 0.551100 | 0.356200 | mV |

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Low Dose Rate Post Radiation Characteristics $T_A = +25^\circ\text{C}$, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. (see Note 14). These are not limits nor are they guaranteed. (Continued)

| ITEM # | DESCRIPTION | CONDITION | 0k RAD | 50k RAD | 100k RAD | UNITS |
|--------|--------------------------------|---|------------|------------|------------|---------------|
| 30 | DC Input Line Regulation | $V_{OUT} + 0.4V < V_{IN} < 6.0V, V_{OUT} = 5.0V$ | 5.792850 | 5.296750 | 5.315300 | mV |
| 31 | DC Output Load Regulation | $V_{OUT} = 1.5V; 0A < I_{LOAD} < 3.0A, V_{IN} = V_{OUT} + 0.4V$ | -1.525700 | -1.571300 | -1.219950 | mV |
| 32 | DC Output Load Regulation | $V_{OUT} = 1.8V; 0A < I_{LOAD} < 3.0A, V_{IN} = V_{OUT} + 0.4V$ | -1.314200 | -1.447200 | -1.372050 | mV |
| 33 | DC Output Load Regulation | $V_{OUT} = 5.0V; 0A < I_{LOAD} < 3.0A, V_{IN} = V_{OUT} + 0.4V$ | -5.026850 | -5.007050 | -4.816750 | mV |
| 34 | Feedback Input Current | $V_{ADJ} = 0.5V$ | -0.011650 | -0.030300 | -0.036550 | μA |
| 35 | Ground Pin Current | $V_{OUT} = 1.5V; I_{LOAD} = 0A, V_{IN} = 2.2V$ | 10.665000 | 10.658900 | 10.621750 | mA |
| 36 | Ground Pin Current | $V_{OUT} = 1.5V; I_{LOAD} = 3.0A, V_{IN} = 2.2V$ | 11.977100 | 12.015600 | 11.948450 | mA |
| 37 | Ground Pin Current | $V_{OUT} = 5.0V; I_{LOAD} = 0A, V_{IN} = 6.0V$ | 15.814550 | 15.840150 | 15.771750 | mA |
| 38 | Ground Pin Current | $V_{OUT} = 5.0V; I_{LOAD} = 3.0A, V_{IN} = 6.0V$ | 17.223200 | 17.224650 | 17.189200 | mA |
| 39 | Ground Pin Current in Shutdown | ENABLE Pin = 0V, $V_{IN} = 6.0V$ | 0.430300 | 0.601500 | 0.707900 | μA |
| 40 | Dropout Voltage | $I_{LOAD} = 1.0A, V_{OUT} = 2.5V$ | 62.801250 | 62.431600 | 65.466000 | mV |
| 41 | Dropout Voltage | $I_{LOAD} = 2.0A, V_{OUT} = 2.5V$ | 132.799650 | 133.294300 | 138.742500 | mV |
| 42 | Dropout Voltage | $I_{LOAD} = 3.0A, V_{OUT} = 2.5V$ | 214.477050 | 213.033000 | 221.517950 | mV |
| 43 | Output Short Circuit Current | $V_{OUT} = 0V, V_{IN} = 2.2V, R_{SET} = 5.11k$ | 1.178050 | 1.199850 | 1.224300 | A |
| 44 | Output Short Circuit Current | $V_{OUT} = 0V, V_{IN} = 2.2V, R_{SET} = 511\Omega$ | 5.838350 | 5.898050 | 5.750950 | A |
| 45 | Output Short Circuit Current | $V_{OUT} = 0V, V_{IN} = 6.0V, R_{SET} = 5.11k$ | 1.317450 | 1.338450 | 1.361150 | A |
| 46 | Output Short Circuit Current | $V_{OUT} = 0V, V_{IN} = 6.0V, R_{SET} = 511\Omega$ | 6.375650 | 6.464150 | 6.539300 | A |
| 47 | PSRR | $V_{P-P} = 300mV, f = 1kHz, I_{LOAD} = 3A; V_{IN} = 2.5V, V_{OUT} = 1.8V$ | 64.103100 | 67.373400 | 65.407000 | db |
| 48 | Enable Rising Threshold | $V_{IN} = 2.2V$ | 0.867700 | 0.835700 | 0.827700 | V |
| 49 | Enable Rising Threshold | $V_{IN} = 6.0V$ | 0.915800 | 0.905800 | 0.893800 | V |
| 50 | Enable Falling Threshold | $V_{IN} = 2.2V$ | 0.681400 | 0.671300 | 0.661300 | V |
| 51 | Enable Falling Threshold | $V_{IN} = 6.0V$ | 0.727500 | 0.715400 | 0.707400 | V |
| 52 | Enable Pin Leakage Current | $V_{IN} = 6.0V, EN = 0V$ | -0.004900 | -0.025200 | -0.030100 | μA |
| 53 | Enable Pin Leakage Current | $V_{IN} = 6.0V, EN = 6.0V$ | -0.009750 | -0.024850 | -0.029650 | μA |
| 54 | Enable Hysteresis | $V_{IN} = 2.2V$ | 184.368000 | 166.332000 | 168.336000 | mV |
| 55 | Enable Hysteresis | $V_{IN} = 6.0V$ | 188.377000 | 190.381000 | 188.377000 | mV |
| 56 | Enable Pin Propagation Delay | $V_{IN} = 2.2V, EN$ rise to I_{OUT} rise | 304.015700 | 299.771700 | 296.604250 | μs |
| 57 | PG Rising Threshold | $V_{IN} = 2.2V$ | 88.455750 | 88.057850 | 88.741300 | % |
| 58 | PG Rising Threshold | $V_{IN} = 6.0V$ | 89.994350 | 89.499600 | 90.142250 | % |
| 59 | PG Falling Threshold | $V_{IN} = 2.2V$ | 85.755650 | 85.356800 | 85.996150 | % |
| 60 | PG Falling Threshold | $V_{IN} = 6.0V$ | 86.812350 | 86.316300 | 86.870500 | % |
| 61 | PG Hysteresis | $V_{IN} = 2.2V$ | 2.701500 | 2.699650 | 2.745150 | % |
| 62 | PG Hysteresis | $V_{IN} = 6.0V$ | 3.182050 | 3.183350 | 3.271700 | % |
| 63 | PG Low Voltage | $I_{SINK} = 1mA$ | 31.560800 | 31.295600 | 31.212750 | mV |
| 64 | PG Low Voltage | $I_{SINK} = 6mA$ | 177.500500 | 177.572900 | 175.997050 | mV |
| 65 | PG Leakage Current | $V_{IN} = 6.0V, PG = 6.0V$ | 0.017550 | -0.000750 | -0.002400 | μA |

NOTE:

14. See the [Radiation report](#).

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Post Radiation Characteristics for High Dose and Low Dose $T_A = +25^\circ\text{C}$, unless otherwise noted. This data is typical test data post radiation exposure at a rate of 10mrad(Si)/s for low dose rate and 50-300rad(Si)/s for high dose rate. This data is intended to show typical parameter shifts due to HDR (High Dose Rate) or LDR (Low Dose Rate) radiation. These are not limits nor are they guaranteed.

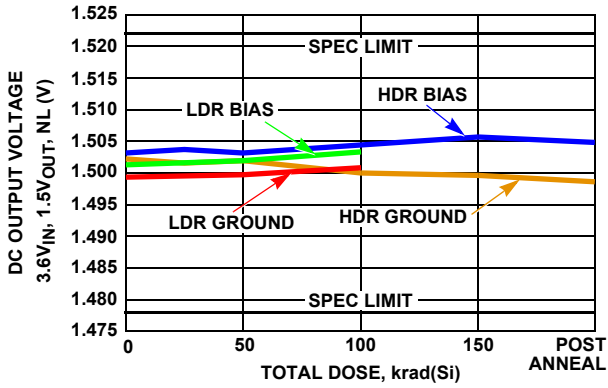


FIGURE 3. DC OUTPUT VOLTAGE, 1.5V_{OUT}, 3.6V_{IN} NO LOAD

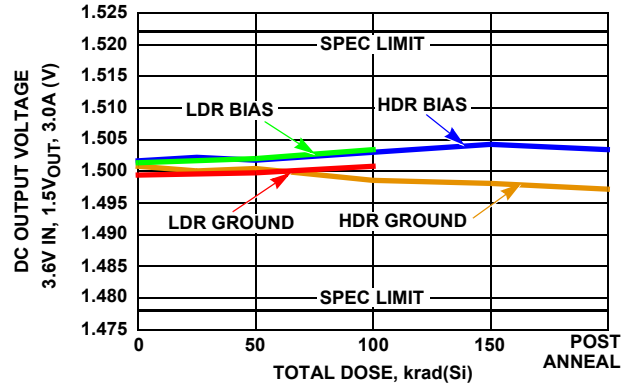


FIGURE 4. DC OUTPUT VOLTAGE, 1.5V_{OUT}, 3.6V_{IN}, 3A LOAD

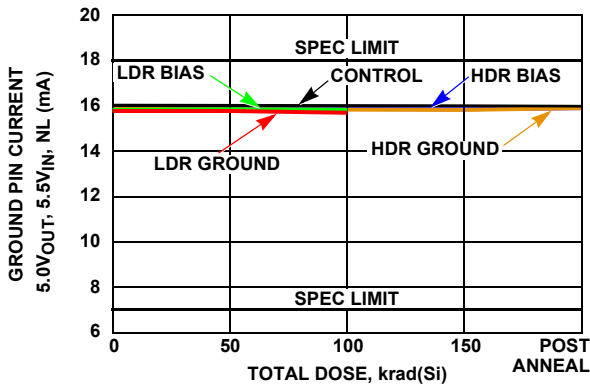


FIGURE 5. GROUND PIN CURRENT, 1.5V_{OUT}, 6.0V_{IN}, NO LOAD

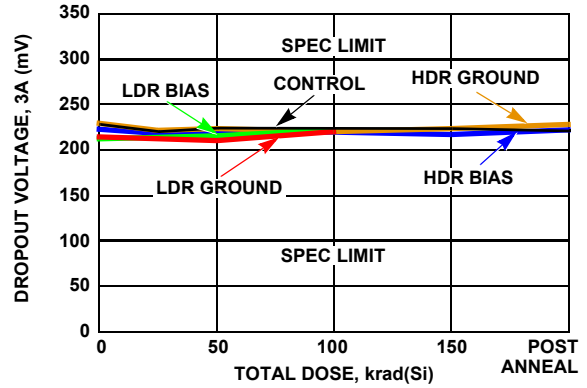


FIGURE 6. DROPOUT VOLTAGE, 2.5V_{OUT}, 3A LOAD CURRENT

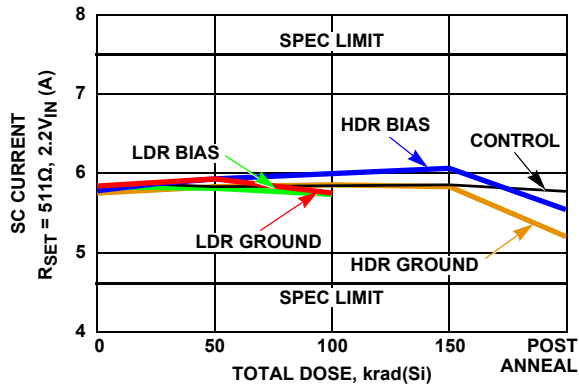


FIGURE 7. OUTPUT SHORT CIRCUIT CURRENT, $R_{SET} = 511\Omega$, 2.2V_{IN}

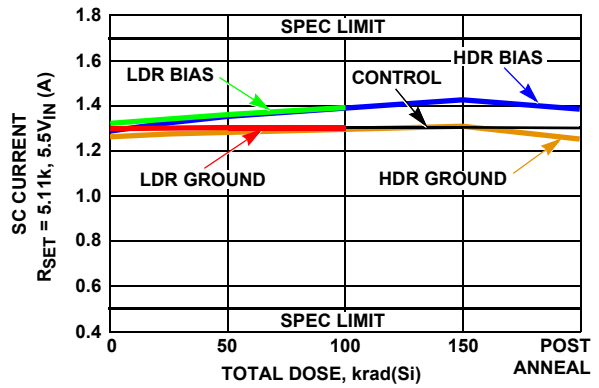


FIGURE 8. OUTPUT SHORT CIRCUIT CURRENT, $R_{SET} = 5.11k$, 6.0V_{IN}

Typical Operating Performance

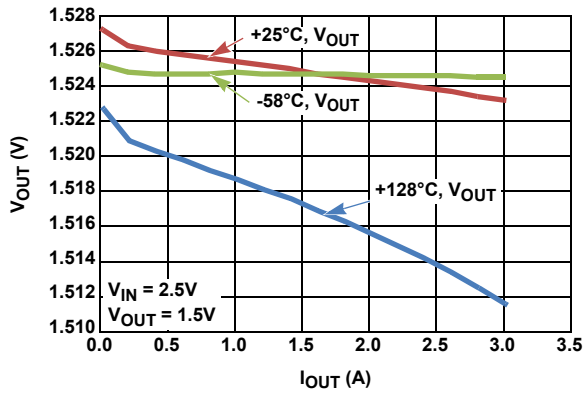


FIGURE 9. LOAD REGULATION, V_{OUT} vs I_{OUT}

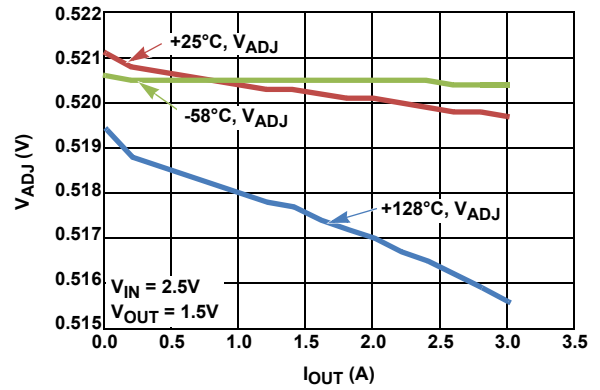


FIGURE 10. LOAD REGULATION, V_{ADJ} vs I_{OUT}

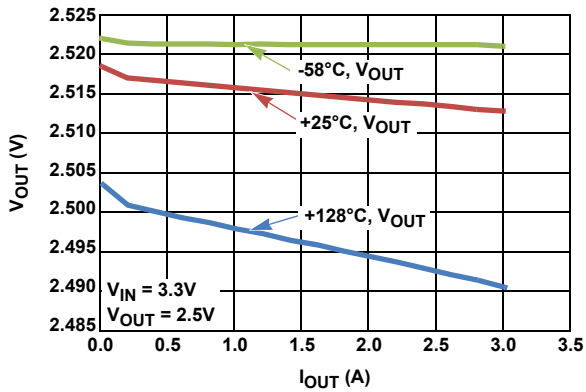


FIGURE 11. LOAD REGULATION, V_{OUT} vs I_{OUT}

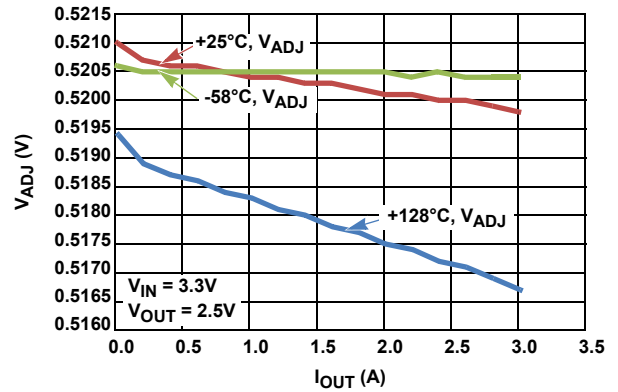


FIGURE 12. LOAD REGULATION, V_{ADJ} vs I_{OUT}

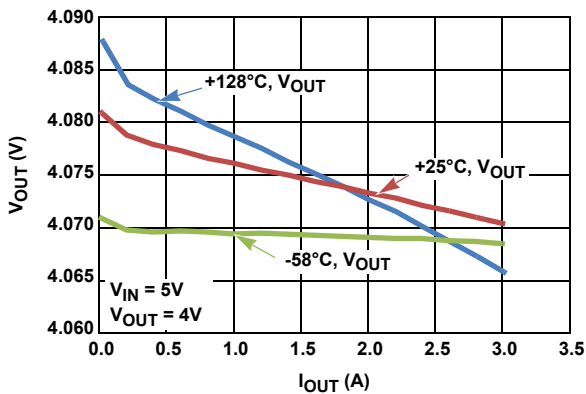


FIGURE 13. LOAD REGULATION, V_{OUT} vs I_{OUT}

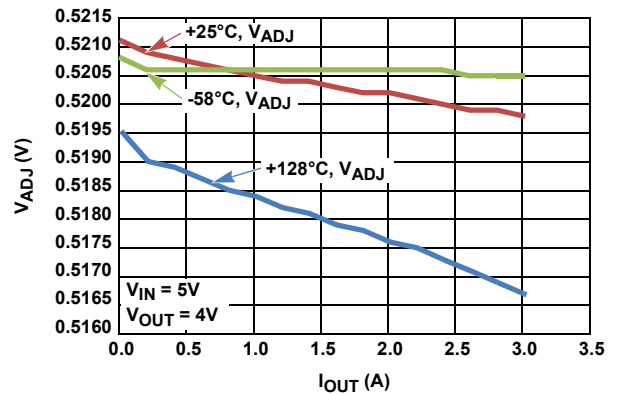


FIGURE 14. LOAD REGULATION, V_{ADJ} vs I_{OUT}

Typical Operating Performance (Continued)

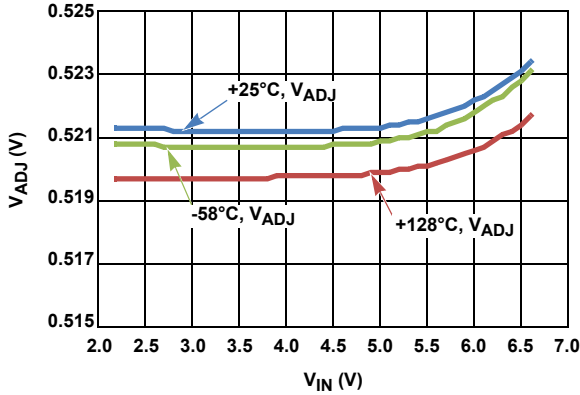


FIGURE 15. V_{IN} vs V_{ADJ} OVER TEMPERATURE

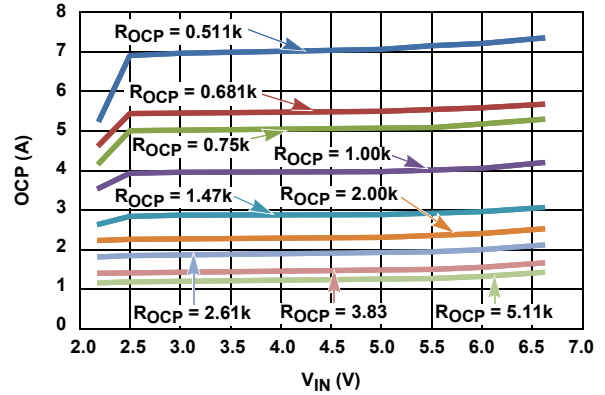


FIGURE 16. R_{OCP} vs OCP AT +25°C, V_{OUT} = 1.5V

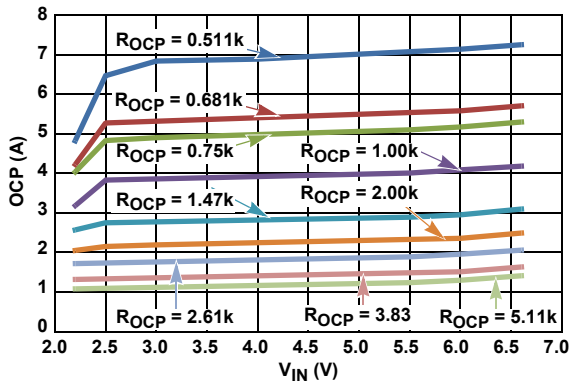


FIGURE 17. R_{OCP} vs OCP AT +128°C, V_{OUT} = 1.5V

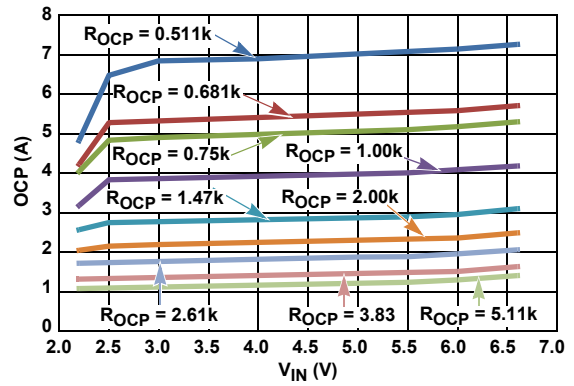


FIGURE 18. R_{OCP} vs OCP AT -58°C, V_{OUT} = 1.5V

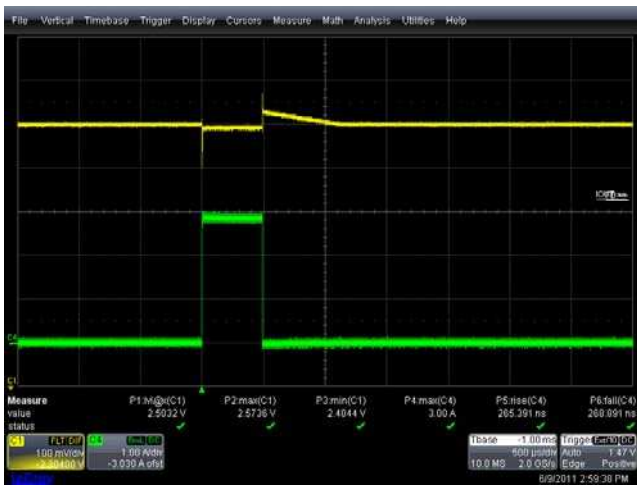


FIGURE 19. TRANSIENT LOAD RESPONSE, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 47µF, 35mΩ



FIGURE 20. TRANSIENT LOAD RESPONSE, V_{IN} = 3.3V, V_{OUT} = 2.5V, C_{OUT} = 220µF, 25mΩ

Typical Operating Performance (Continued)



FIGURE 21. POWER-ON AND POWER-OFF, EN = 0 TO 1, +25°C, $V_{IN} = 6V$, $V_{OUT} = 0.8V$, $I_{OUT} = 0.5A$, PGOOD TURN-ON



FIGURE 22. POWER-ON AND POWER-OFF, EN = 0 TO 1, +25°C, $V_{IN} = 2.2V$, $V_{OUT} = 0.8V$, $I_{OUT} = 0.5A$, PGOOD TURN-ON



FIGURE 23. POWER-ON AND POWER-OFF, EN = 1 TO 0, +25°C, $V_{IN} = 6V$, $V_{OUT} = 0.8V$, $I_{OUT} = 0.5A$, PGOOD TURN-OFF



FIGURE 24. POWER-ON AND POWER-OFF, EN = 1 TO 0, +25°C, $V_{IN} = 2.2V$, $V_{OUT} = 0.8V$, $I_{OUT} = 0.5A$, PGOOD TURN-OFF

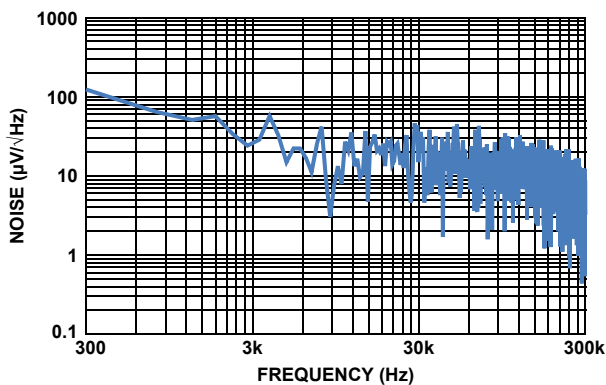


FIGURE 25. NOISE ($\mu V/\sqrt{Hz}$)

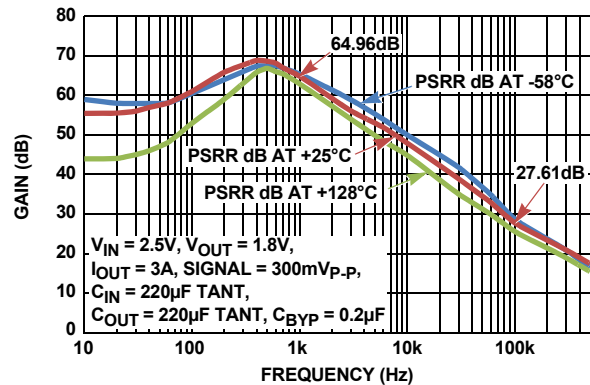


FIGURE 26. PSRR

Applications Information

Input Voltage Requirements

This RH LDO will work from a V_{IN} in the range of 2.2V to 6.0V. The input supply can have a tolerance of as much as $\pm 10\%$ for conditions noted in the “Electrical Specifications” table starting on page 4. Minimum guaranteed input voltage is 2.2V. However, due to the nature of an LDO, V_{IN} must be some margin higher than the output voltage, plus dropout at the maximum rated current of the application, if active filtering (PSRR) is expected from V_{IN} to V_{OUT} . The dropout spec of this family of LDOs has been generously specified to allow applications to design for efficient operation.

Adjustable Output Voltage

The output voltage of the RH LDO can be set to any user programmable level between 0.8V to 5.0V. This is achieved with a resistor divider connected between the OUT, ADJ and GND pins. With the internal reference at 0.52V, the divider ratio should be fixed such that when the desired V_{OUT} level is reached, the voltage presented to the ADJ pin is 0.52V. Resistor values for typical voltages are shown in Table 1.

TABLE 1. RESISTOR VALUES FOR TYPICAL VOLTAGES

| V_{OUT} | R_{BOTTOM} | R_{TOP} |
|-----------|--------------|-----------|
| 0.8V | 7.87k | 4.32k |
| 1.5V | 2.26k | 4.32k |
| 1.8V | 1.74k | 4.32k |
| 2.5V | 1.13k | 4.32k |
| 4.0V | 634 | 4.32k |
| 5.0V | 499 | 4.32k |

Input and Output Capacitor Selection

RH operation requires the use of a combination of tantalum and ceramic capacitors to achieve a good volume-to-capacitance ratio. The recommended combination is a 220 μ F, 25m Ω 10V DSSC 04051-032 rated tantalum capacitor in parallel with a 0.1 μ F MIL-PRF-49470 CDR04 ceramic capacitor, to be connected between V_{IN} to GND pins and V_{OUT} to GND pins of the LDO, with PCB traces no longer than 0.5cm.

The stability of the device depends on the capacitance and ESR of the output capacitor. The usable ESR range for the device is 6m Ω to 100m Ω . At the lower limit of ESR = 6m Ω , the phase margin is about 51°. On the high side, an ESR of 100m Ω is found to limit the gain margin at around 10dB. The typical GM/PM seen with capacitors are shown in Table 2.

TABLE 2. TYPICAL GM/PM WITH VARIOUS CAPACITORS

| CAPACITANCE (μ F) | ESR (m Ω) | GAIN MARGIN (dB) | PHASE MARGIN (°) |
|------------------------|-------------------|------------------|------------------|
| 47 | 35 | 14 | 55 |
| 100 | 25 | 16 | 57 |
| 220 | 6 | 19 | 51 |
| 220 | 25 | 16 | 69 |
| 100 | 100 | 10 | 62 |

Type numbers of KEMET capacitors used in the device are shown in Table 3.

TABLE 3. KEMET CAPACITORS USED IN DEVICE

| KEMET TYPE NUMBER | CAPACITOR DETAILS |
|--------------------|---------------------------------|
| T525D476M016ATE035 | 47 μ F, 10V, 35m Ω |
| T525D107M010ATE025 | 100 μ F, 10V, 25m Ω |
| T530D227M010ATE006 | 220 μ F, 10V, 6m Ω |
| T525D227M010ATE025 | 220 μ F, 10V, 25m Ω |
| T495X107K016ATE100 | 100 μ F, 16V, 100m Ω |

A typical gain phase plot measured on the ISL75051SRHEVAL1Z evaluation board for $V_{IN} = 3.3V$, $V_{OUT} = 1.8V$ and $I_{OUT} = 3A$ with a 220 μ F, 10V, 25m Ω capacitor is shown in Figure 27 and is measured at GM = 16.3dB and PM = 69.16°.

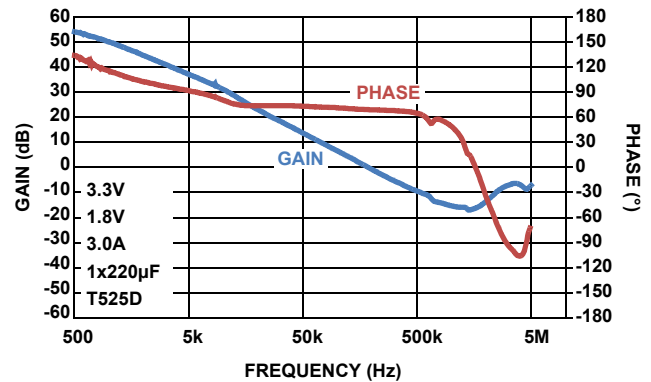


FIGURE 27. TYPICAL GAIN PHASE PLOT

Enable

The device can be enabled by applying a logic high on the EN pin. The enable threshold is typically 0.9V. A soft-start cycle is initiated when the device is enabled using this pin. Taking this pin to logic low disables the device.

EN can be driven from either an open drain or a totem pole logic drive between EN pin and GND. Assuming an open drain configuration, M1 will actively pull down the EN line, as shown in Figure 28, and thereby discharge the input capacitance, shutting off the device immediately.

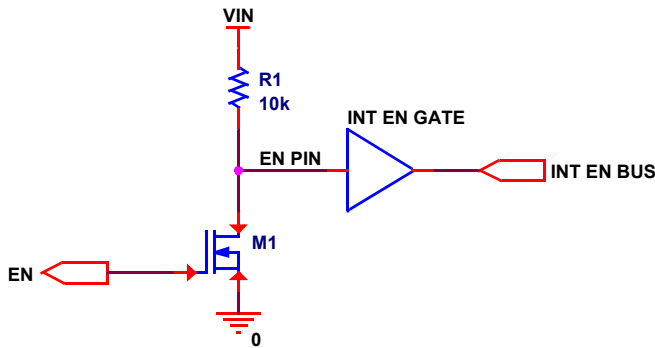


FIGURE 28. ENABLE

Power-Good

The Power-Good pin is asserted high when the voltage on the ADJ pin crosses the rising threshold of $0.9 \times V_{ADJ}$ typ. On the falling threshold, Power-Good is asserted low when the voltage on the ADJ pin crosses the falling threshold of $0.88 \times V_{ADJ}$. The power-good output is an open-drain output rated for a continuous sink current of 1mA.

Soft-start

Soft-start is achieved by means of the charging time constant of the BYP pin. The capacitor value on the pin determines the time constant and can be calculated using Equation 1:

$$T_S = 0.00577 \times C_S \quad (\text{EQ. 1})$$

where T_S = soft-start time in ms, and C_S = BYPASS capacitor in nF.

The BYPASS capacitor, C1, charges with a $90\mu\text{A}$ source current and provides an EA reference, -IN, with an SS ramp. V_{OUT} , in turn, follows this ramp. The ramp rate can be calculated based on the C1 value. For conditions in which C1 is opened, or for small values of C1, the ramp is provided by C2 = 50pF, with a source of $0.5\mu\text{A}$. Connecting C1 min = $0.1\mu\text{F}$ to the BYPASS pin is recommended for normal operation.

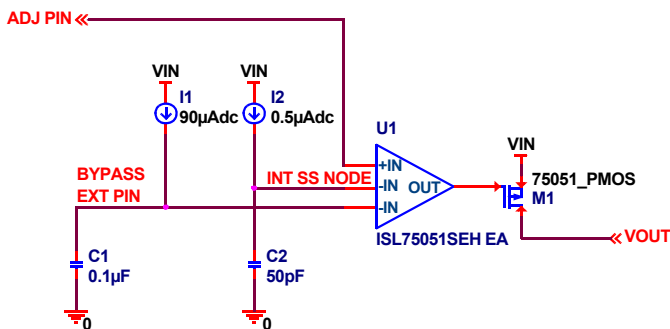


FIGURE 29. SOFT-START

Current Limit Protection

The RH LDO incorporates protection against overcurrent due to any short or overload condition applied to the output pin. The current limit circuit becomes a constant current source when the output current exceeds the current limit threshold, which can be adjusted by means of a resistor connected between the OCP pin and GND. If the short or overload condition is removed from V_{OUT} , then the output returns to normal voltage mode regulation. OCP can be calculated with Equation 2:

$$OCP = 9.5 \cdot \text{EXP}(-0.6 \cdot (\text{ROCP} / (1 + 0.1\text{ROCP}))) \quad (\text{EQ. 2})$$

where OCP = Overcurrent Threshold in amps, and ROCP = OCP resistor in kΩ.

In the event of an overload condition based on the set OCP limit, the die temperature may exceed the internal over-temperature limit, and the LDO begins to cycle on and off due to the fault condition (Figure 30). However, thermal cycling may never occur if the heatsink used for the package can keep the die temperature below the limits specified for thermal shutdown.

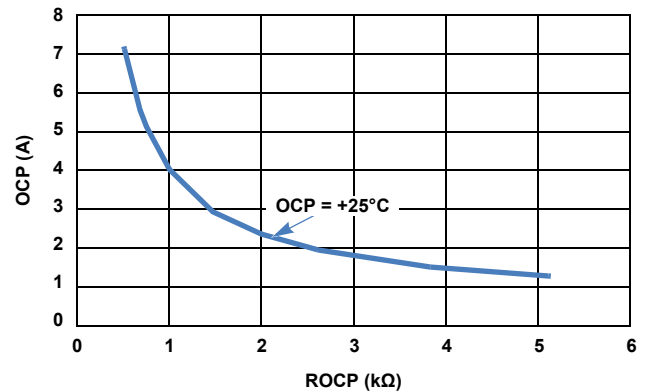


FIGURE 30. OCP vs ROCP OVER TEMP

Thermal Guidelines

If the die temperature exceeds typically $+175^\circ\text{C}$, then the LDO output shuts down to zero until the die temperature cools to typically $+155^\circ\text{C}$. The level of power combined with the thermal impedance of the package (θ_{JC} of 4°C/W for the 18 Ld CDFP package) determines whether the junction temperature exceeds the thermal shutdown temperature specified in the “Electrical Specifications” table.

The device should be mounted on a high effective thermal conductivity PCB with thermal vias, per JESD51-7 and JESD51-5. Place a silpad between package base and PCB copper plane. The VIN and VOUT ratios should be selected to ensure that dissipation for the selected VIN range keeps T_J within the recommended operating level of 150°C for normal operation.

Weight Characteristics

Weight of Packaged Device

K18.D: 1.07 Grams typical with leads clipped

ISL75051SEH

Die Characteristics

Die Dimensions

4555 μ m x 4555 μ m (179.3 mils x 179.3 mils)
Thickness: 304.8 μ m \pm 25.4 μ m (12.0 mils \pm 1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
Thickness: 0.3 μ m \pm 0.03 μ m to 1.2 μ m \pm 0.12 μ m

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 2.7 μ m \pm 0.4 μ m

BACKSIDE METALLIZATION

None

SUBSTRATE

Type: Silicon

BACKSIDE FINISH

Silicon

PROCESS

0.6 μ m BiCMOS Junction Isolated

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased

ADDITIONAL INFORMATION

Worst Case Current Density

$< 2 \times 10^5$ A/cm²

Transistor Count

2932

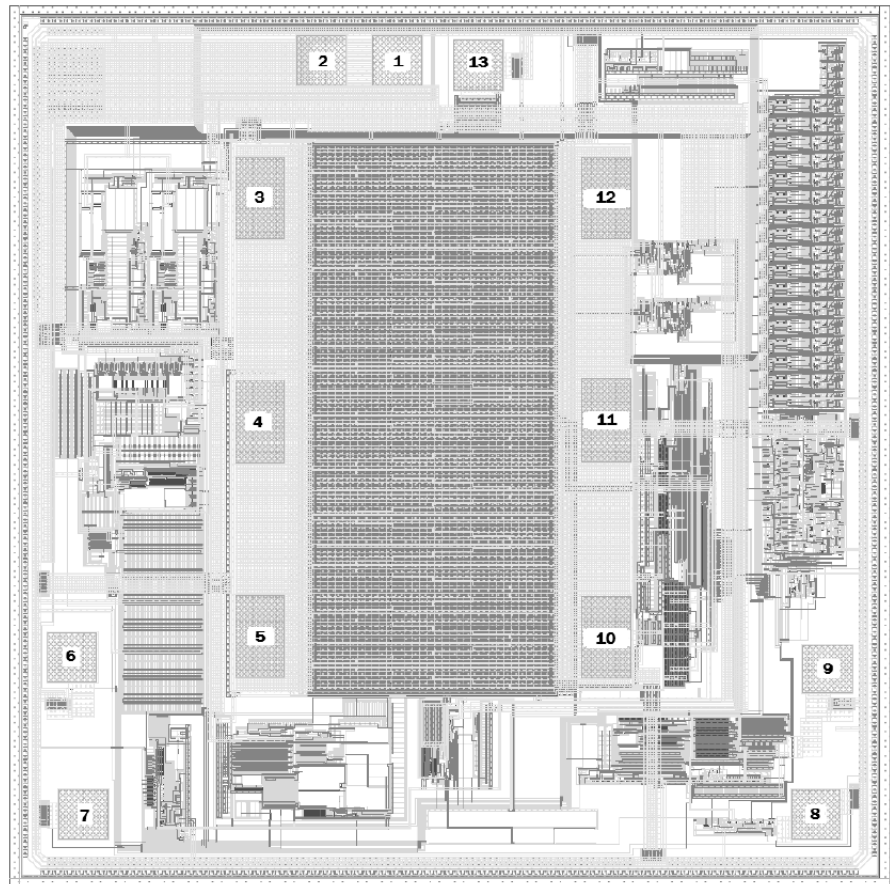
Layout Characteristics

Step and Repeat

4555 μ m x 4555 μ m

Metallization Mask Layout

| PAD X Y COORDINATES | | | |
|---------------------|------|-----------|-----------|
| PAD | NAME | X μ m | Y μ m |
| 1 | GND | 0 | 0 |
| 2 | GND | -393 | 0 |
| 3 | VOUT | -711 | -710 |
| 4 | VOUT | -711 | -1858 |
| 5 | VOUT | -711 | -2964 |
| 6 | ADJ | -1680 | -3070 |
| 7 | BYP | -1621 | -3879 |
| 8 | EN | 2164 | -3879 |
| 9 | OCP | 2222 | -3131 |
| 10 | VIN | 1078 | -2965 |
| 11 | VIN | 1078 | -1853 |
| 12 | VIN | 1078 | -711 |
| 13 | PG | 420 | -25 |



Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|-----------------|----------|------------------|
| August 28, 2012 | FN8294.0 | Initial Release. |

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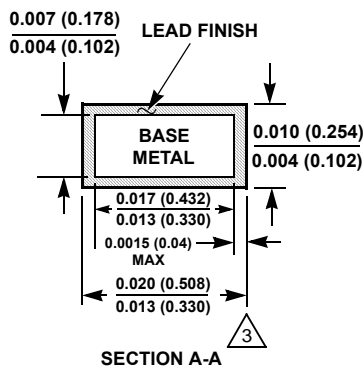
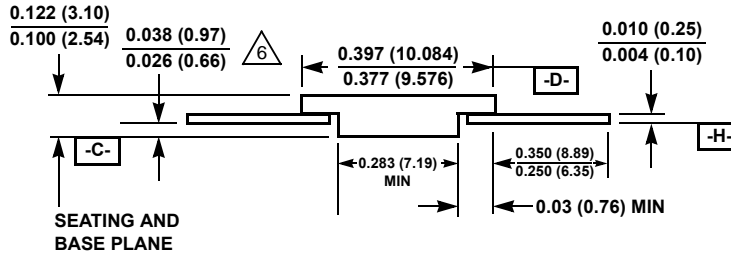
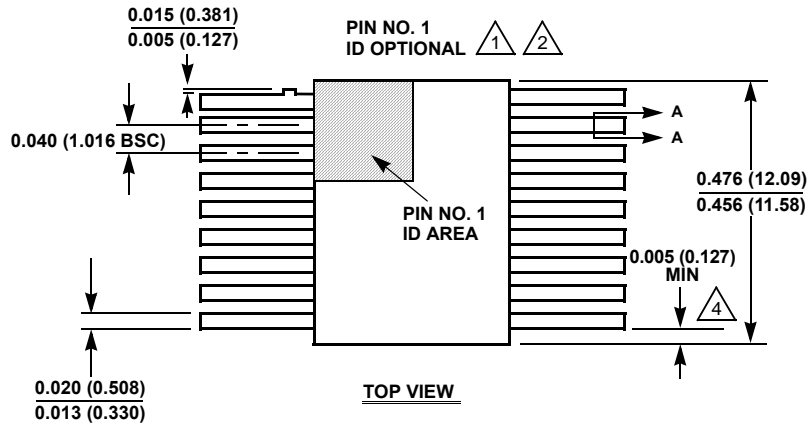
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Package Outline Drawing

K18.D

18 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

Rev 3, 1/12



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions = INCH (mm). Controlling dimension: INCH.