Data Sheet | April 3, 2008 | FN6541.1

Dual Input Lithium Ion Battery Charger with OVP USB Bypass and 10mA LDO

The ISL9221 Lithium Ion charging IC is designed to meet the charging requirements of most of today's handheld devices. The IC provides two inputs for either USB connection where the current is limited by the USB standard or for powering/charging from a power adapter.

If the voltage at either VUSB or VDC pin is within the safe allowable range, the $\overline{PPR}$ pin is pulled low indicating to the system processor that external power is available.

Charging can be enabled/disabled by controlling the state of the $\overline{EN}$ pin. While charging, the $\overline{CHG}$ pin is pulled low indicating the battery is being charged.

The battery is charged to 4.2V with only a 1% error across the temperature range. USB charge current, Adapter charge current and charge termination currents can be programmed via external resistors.

The ISL9221 adds an additional feature in providing a limited amount of current to system architecture while protecting the system from destructively high voltage.

The device contains Thermal regulation and protection to provide additional safety features of this device. When the temperature exceeds +125°C, the current will fold back to reduce and control the die temperature.

Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL9221IRZ	9221	-40°C to +85°C	12 Ld 4x3 DFN	L12.4x3
ISL9221IRZ-T*	9221	-40°C to +85°C	12 Ld 4x3 DFN	L12.4x3

*Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

- Lithium Ion/Polymer battery charging
- Dual input - USB host or car/wall adapter
- Input voltage withstanding up to 28V
- 5.4V overvoltage protection on VUSB inputs
- Charging current up to 1.2A
- 4.9V/10mA linear regulator with input OVP
- Current limit on bypass path
- Programmable end-of-charge current
- Programmable charging current
- Programmable USB current limit
- Charging and power present indicator pins
- Charge enable pin
- Reverse current protection
- Pb-free (RoHS compliant)

Applications

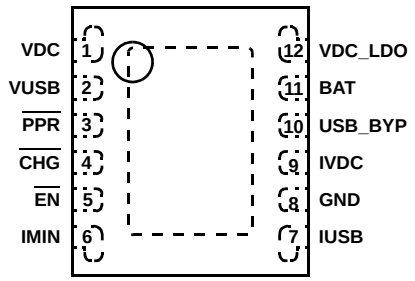
- Smart Handheld Devices
- Cell Phones, PDAs, MP3 Players
- Digital Still Cameras
- Handheld Test Equipment

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"
- Technical Brief TB389 "PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages"

Pinout

ISL9221
(12 LD DFN)
TOP VIEW



Absolute Maximum Ratings

Supply Voltage (V_{DC}, V_{USB}) . . . . . -0.3V to 28V
Other Input Voltage ($\overline{EN}$, IMIN, IUSB, IVDC) . . . . . -0.3V to 7V
Open Drain Pull Voltage ($\overline{PPR}$, $\overline{CHG}$) . . . . . -0.3V to 7V
Other Pin Voltage(VDC_LDO, USB_BYP, VBAT) . . . . . -0.3V to 7V

Recommended Operating Conditions

Ambient Temperature Range . . . . . -40℃ to +85℃
Supply Voltage (V_{USB}) . . . . . 4.5V to 5.3V
Supply Voltage (V_{DC}) . . . . . 4.5V to 6.7V
Typical Adapter Charge Current . . . . . 100mA to 1.2A
Typical USB Charge Current . . . . . 46.5mA to 465mA
Typical USB Bypass Current . . . . . 0mA to 200mA
Typical LDO Current . . . . . 0mA to 10mA

Thermal Information

Thermal Resistance (Typical, Notes 1, 2)	θ_{JA} (℃/W)	θ_{JC} (℃/W)
4x3 DFN Package	41	3.5

Maximum Junction Temperature (Plastic Package)+ . . . . . +150℃
Maximum Storage Temperature Range . . . . . -65℃ to +150℃
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
3. Parts are 100% tested at +25℃. Temperature limits established by characterization and are not production tested.

Electrical Specifications

Typical Values are tested at USB = VDC = 5V and ambient temperature at +25℃, unless otherwise noted. All maximum and minimum values are guaranteed under the recommended operating conditions.

PARAMETERS	SYMBOL	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
CHARGER POWER-ON THRESHOLDS						
Rising VUSB/VDC Threshold			3.4	3.9	4.2	V
Falling VUSB/VDC Threshold			3.2	3.7	4.0	V
INPUT VOLTAGE OFFSET						
Rising Edge of VDC or VUSB Relative to V_{BAT}	VOS_{HC}	V_{BAT} = 4.0V, use CHG pin to indicate the comparator output	-	150	250	mV
Falling Edge of VDC or VUSB Relative to V_{BAT}	VOS_{LC}		20	80	-	mV
STANDBY CURRENT						
BAT Pin Sink Current	$I_{STANDBY}$	$\overline{EN}$ = HIGH or both inputs are floating	-	0.05	0.5	µA
VDC Pin Supply Current	I_{VDC}	$\overline{EN}$ = HIGH, I_{LDO} = 0	-	365	420	µA
VUSB Pin Supply Current	I_{VUSB}	$\overline{EN}$ = HIGH, USB_BYP disconnected	-	300	360	µA
VDC/USB Pin Supply Current		$\overline{EN}$ = LOW, I_{LDO} = 0, USB_BYP disconnected	-	0.63	0.85	mA
VOLTAGE REGULATION						
Output Voltage	V_{BAT}	Load = 10mA	4.158	4.2	4.242	V
		Load = 10mA (T_J = +25℃)	4.174	4.2	4.226	V
VDC Linear ON-resistance		V_{BAT} =3.8V, I_{VDC} = 0.3A, (T_J = +25℃)	-	600	-	mΩ
USB Linear ON-resistance		V_{BAT} =3.8V, I_{USB} = 0.3A, (T_J = +25℃)	-	600	-	mΩ
CHARGE CURRENT						
IVDC Pin Output Voltage	V_{IVDC}	V_{BAT} = 3.8V	1.19	1.22	1.25	V
VDC Constant Current Accuracy	I_{VDC_CHRG}	R_{IVDC} = 12.4kΩ, V_{BAT} = 2.7V to 3.8V	500	550	580	mA
VDC Trickle Charge Current	I_{VDC_TRKL}	R_{IVDC} = 12.4kΩ, V_{BAT} = 2.2V, given as a % of the I_{VDC_CHARGE}	16	18	20	%

Electrical Specifications Typical Values are tested at USB = VDC = 5V and ambient temperature at +25℃, unless otherwise noted. All maximum and minimum values are guaranteed under the recommended operating conditions. **(Continued)**

PARAMETERS	SYMBOL	CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNITS
IUSB Pin Output Voltage	V_{IUSB}	V_{BAT} = 3.8V	1.19	1.22	1.25	V
VUSB Constant Current Accuracy	I_{USB_CHRG}	R_{IUSB} = 29.4kΩ,V_{BAT} = 2.7V to 3.8V	211	232	246	mA
VUSB Trickle Charge Current	I_{USB_TRKL}	R_{IUSB} = 29.4kΩ, V_{BAT} = 2.2V and if $I_{USB\_CHRG} \le I_{VDC\_TRKL}$, then given as a % of the I_{USB_CHRG}	16	18	20	%
		If $I_{USB\_CHRG} \le I_{VDC\_TRKL}$	-	I_{USB_CHRG}	-	%
DC and USB End-of-Charge Threshold	I_{MIN}	R_{MIN} = 10kΩ	46.5	55	63.5	mA
PRECONDITIONING CHARGE THRESHOLD						
Preconditioning Charge Threshold Voltage	V_{MIN}		2.5	2.6	2.7	V
RECHARGE THRESHOLD						
Recharge Threshold Voltage	V_{RCH}		3.8	3.9	4.0	V
PROTECTIONS						
VDC Overvoltage Level	OVP		6.7	6.8	6.9	V
VDC Overvoltage Hysteresis	H_{OVP}		-	90	130	mV
VDC Overvoltage Protection Delay			-	1	-	µs
VUSB Overvoltage Level			5.3	5.4	5.5	V
VUSB Overvoltage Hysteresis			-	60	90	mV
VUSB Overvoltage Protection Delay			-	1	-	µs
Short Circuit (USB_BYP)	I_{OCP}		-	400	600	mA
BYPASS FETS						
Resistance VUSB to USB_BYP	USB_ $r_{DS(ON)}$	Measured at 200mA, 4.3V < V_{DC} < 5.3V	-	1.3	2.0	Ω
Drop Out VUSB to USB_BYP	$VUSB_{DO}$	I_{OUT} = 150mA, V_{USB} > 4.3V	-	200	-	mV
INTERNAL TEMPERATURE MONITORING						
Current Fold Back Threshold	T_{FOLD}		-	125	-	℃
LOGIC INPUT AND OUTPUT						
$\overline{EN}$ Pin Logic Input HIGH	V_{IH}		1.3	-	-	V
$\overline{EN}$ Pin Logic Input LOW	V_{IL}		-	-	0.4	V
$\overline{EN}$ Pin Internal Pull-down Resistance			350	600	850	kΩ
$\overline{CHG}$ and $\overline{PRR}$ Sink Current		Pin Voltage = 0.8V	10	-	-	mA
LINEAR REGULATOR						
Output Voltage	V_{LDO}		-	4.94	-	V
Voltage Regulation Accuracy	V_{REG}	Initial accuracy, I_{LDO} = 10mA; T_J = +25℃	-2.0	-	+2.0	%
		Line/Load, I_{LDO} = 10µA to 10mA, VDC = V_{LDO} + 0.5V to 6.5V; T_J = -40℃ to +125℃	-2.8	-	+2.8	%
Dropout (VDC to V_{LDO})	V_{DO}	I_{LDO} = 10mA, V_{LDO}= 4.9V, $V_{DC} \ge V_{LDO}$+0.5V	-	30	50	mV
Current Limit	I_{LIMIT}	For I_{LDO} = 10mA option, V_{DC} = 5.5V	12	-	-	mA

Pin Assignments

NAME	PIN	TYPE	DESCRIPTION
VDC	1	AI	Input pin from car adapter or AC/DC adapter
VUSB	2	AI	Input pin from USB host device
VDC_LDO	12	AO	Output pin of Linear Regulator
USB_BYP	10	AO	Output pin from USB bypass circuitry
IVDC	9	AI	Battery current setting pin for adapter power
IUSB	7	AI	Current setting pin for USB power
IMIN	6	AI	End-of-charge current setting pin
BAT	11	AO	Output pin to battery
$\overline{EN}$	5	DI	Active low charge enable pin
$\overline{PPR}$	3	OD	Active low power present indicator pin
$\overline{CHG}$	4	OD	Active low charging indication pin
GND	8	G	Ground pad

TABLE 1. TYPE CHART

SYMBOL	DESCRIPTION
A	Analog Pin
D	Digital Pin
I	Input Pin
O	Output Pin
OD	Open-Drain
G	Ground

Functional Pin Descriptions

VDC

Adapter input pin. This pin is usually connected to adapter power. The maximum input voltage is 28V. The charge current from this pin is programmable up to 1.2A by selection of the resistor on the IVDC pin. When this pin is connected to a power source, no charge current is drawn from the USB pin. A 1µF or larger value ceramic capacitor is recommended for decoupling.

VDC_LDO

Linear regulator output. A 0.1µF to 1µF ceramic capacitor from this pin to ground is required.

USB_BYP

USB input bypass pin. This is an output from the low current bypass FET connected to the USB input pin. The USB_BYP can be connected to the system to provide safe, voltage-limited power from the USB input pin.

VUSB

VUSB Input pin. This pin is usually connected to a USB port power connector. The maximum input voltage is 28V. However, the internal OVP circuitry will trip at 5.4V.

The maximum current drawn from the VUSB pin is the combination of the load at USB_BYP and the programmed USB charging current.

A 1µF bypass capacitor is recommended on the VUSB pin. Higher values of bypass capacitance can be utilized but the designer should refer to the maximum allowed bus capacitance per USB application standard. When using ceramic capacitors, a small resistance value, such as 1Ω in series with the capacitor, is recommended to reduce voltage overshoot.

IVDC

Adapter charging current setting pin. A resistor on this pin sets the maximum charging current to be delivered to the BAT pin. The maximum current, however, may be reduced by the adapter's current limit or by the power dissipation within the charging IC.

IUSB

USB charge current pin. This pin is connected internally to a current source for setting the programmed charging current delivered to the BAT pin.

BAT

Charger IC output pin. This pin is to be connected to the positive (+) terminal of the battery. The charging IC monitors this pin to determine the charge state of the battery.

A 1µF bypass capacitor from the BAT pin to ground is recommended. The charging IC relies on the battery to help stabilize the circuitry and it is not recommended to operate the charger IC without a battery connected to this pin.

$\overline{EN}$

Enable charging pin. This pin is a logic level input to control charging by the system processor. An external pull-up resistor should be connected to processor's I/O power supply.

The USB_BYP and VDC_LDO stay on regardless of the state of this pin. This ensures that the processor can be powered up when an external source is connected to the VDC or VUSB input pin.

$\overline{PPR}$

Power presence indication pin. This pin is used to notify the system processor or enable the power circuitry when a source is connected. The pin is an open drain output pin, which pulls low when a valid voltage (above POR) is present at either the VDC or VUSB pin. The $\overline{PPR}$ pin is held low regardless of the state of the $\overline{EN}$ pin. If connected to the processor, a pull-up resistor should be connected to the processors I/O supply. If connected to power circuitry, a pull-up should be tied to the appropriate bypass supply.

$\overline{CHG}$

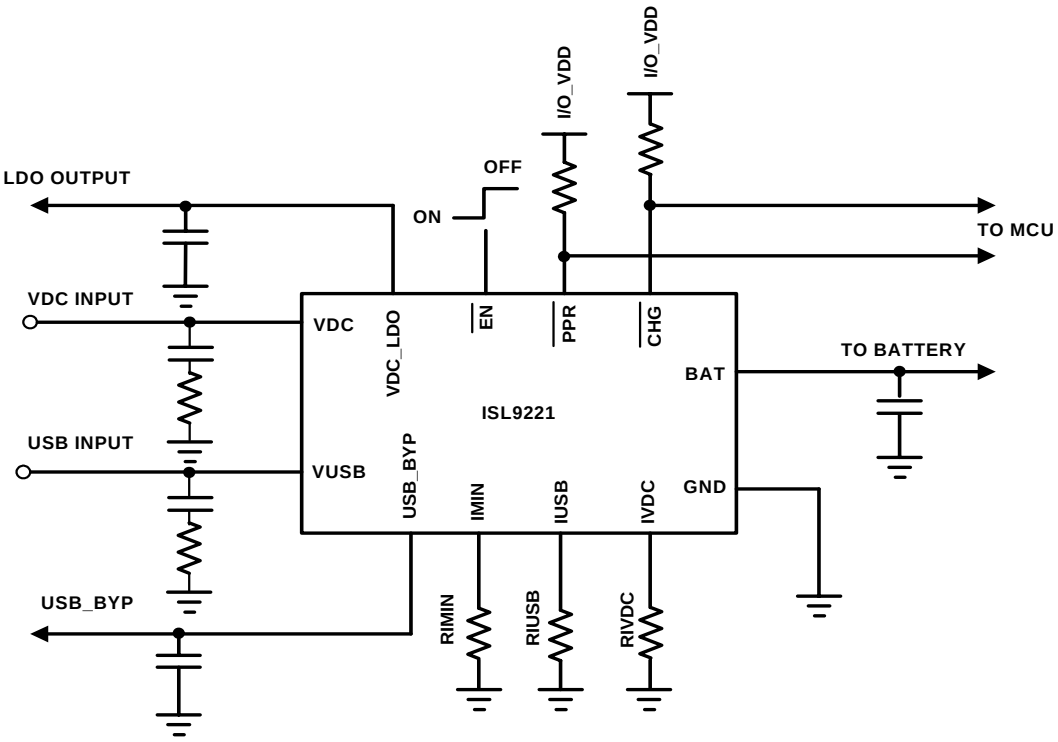
Charge indication pin. This open-drain pin is pulled low to indicate when the battery is being charged. If connected to the processor, a pull-up resistor should be connected to the processors I/O supply.

The $\overline{CHG}$ pin can also be used to drive an LED to indicate to the user the battery is being charged.

GND

Ground pin. This provides the ground path for all internal circuits.

Typical Application



Block Diagram

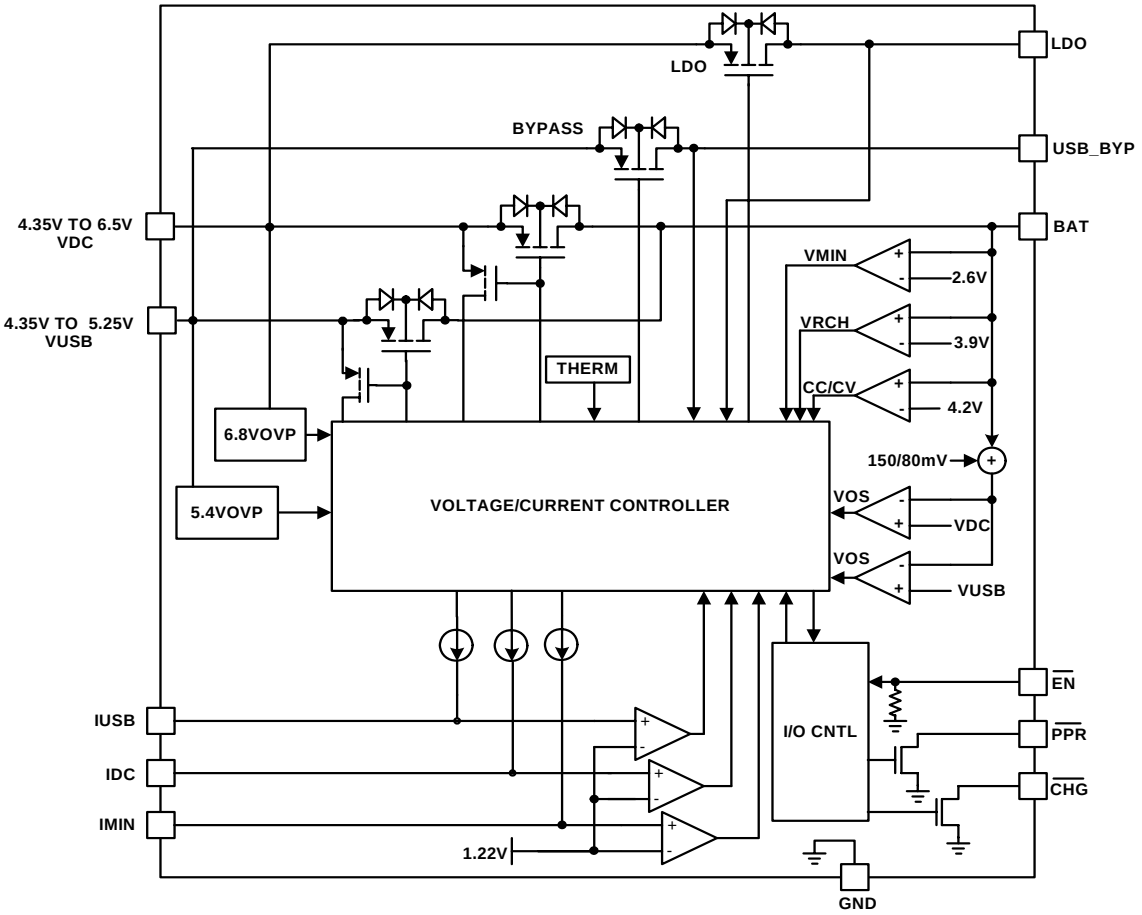


FIGURE 1. SIMPLIFIED BLOCK DIAGRAM

USB Charge Current

When the $\overline{EN}$ pin is pulled low and a valid USB voltage is present at the USB pin, the IC will charge the battery at a rate dependent on the IUSB setting. The charge current maybe reduced by the USB source if it is set to a value higher than the current limit of the USB source.

Equation 1 for setting the IUSB current is as follows:

$$IUSB = \frac{6820}{R_{IUSB}}(mA) \quad \text{(EQ. 1)}$$

Where R_{IUSB} is in kΩ.

The current set by the IUSB pin for charging the battery is in addition to current drawn by the load on the USB_BYP. The system designer should consider the maximum expected USB_BYP load current when selecting the USB charging current so as not to exceed the current limits set by the USB standards.

Typically at room temperature, the $r_{DS(ON)}$ across the charge path, VUSB to BAT is 600mΩ. If the entire USB current limit of 465mA is being supplied to the battery, the drop across the charging FET could be more than 300mV. Thus, the voltage at the USB pin needs to be maintained above ~4.5V. Otherwise, the period to charge the battery may be prolonged.

Adapter Charge Current

When the $\overline{EN}$ pin is pulled low and a valid adapter voltage is present at the VDC pin, the IC will charge the battery at a rate dependent on the IVDC setting; the charge on the battery and the source connected to the VDC pin. An example of this is while the IVDC is set for 1000mA, the adapter supply may only provide 800mA and the battery is limited to the 800mA.

Typically the $r_{DS(ON)}$ across the charge path, VDC to BAT is 600mΩ. At a 1.0A charging rate, 600mV is dropped across the charge path. Thus, the voltage at the VDC pin needs to be maintained above ~4.80V. Otherwise the period to charge the battery may be prolonged.

$$IVDC = \frac{6820}{R_{IVDC}}(mA) \quad \text{(EQ. 2)}$$

Where R_{IVDC} is in kΩ.

It is recommended that the maximum charging current be programmed to between 100mA and 1200mA.

Floating Charge Voltage

The floating voltage during the constant voltage phase is 4.2V. The floating voltage has 1% accuracy over the ambient temperature range of -40℃ to +85℃.

Trickle Charge Current

When the battery voltage is below 2.7V (V_{BATmin}), the charger operates in trickle/preconditioning mode, where the charge current is typically 18% of the programmed current set by R_{IVDC}.

End-of-Charge Indication

When an EOC condition (charge current falls below IMIN during constant-voltage charging) is encountered, the internal open-drain MOSFET at the $\overline{CHG}$ pin turn-off.

IMIN threshold is programmable by the resistor R_{IMIN} at the IMIN pin for both adapter and USB inputs. If the programmed fast charge current is less than IMIN, then after the de-bounce period for $V_{BAT} = V_{BATmax}$ expires, EOC occurs. Once EOC is reached, the status is latched and can be reset by one of the following conditions:

- The part is disabled and re-enabled
- The selected input source is removed and reapplied
- The BAT pin voltage falls below the recharge threshold (~3.9V)

IMIN

IMIN sets the charge termination current for EOC (End-of-Charge). IMIN can be calculated by Equation 3:

$$IMIN = \frac{550}{R_{IMIN}}(mA) \quad \text{(EQ. 3)}$$

Where R_{IMIN} is in kΩ. IMIN is applicable for both adapter and USB charging.

Power Presence Indication

When either the Adapter power or USB is above the POR threshold, the PPR internal Open-Drain MOSFET pulls the pin low indicating that there is a valid source on one of the power input pins.

If only one source is connected and it is above V_{OVP} or both sources are connected and both exceed V_{OVP}, the PPR will be released (HIGH) indicating that the voltage at the pin(s) is invalid. If one input is valid while the other isn't, the PPR pin will be pulled low.

Thermal Fold Back (Thermaguard™)

The thermal fold back function reduces the charge current when the internal temperature reaches the thermal foldback threshold, which is typically +125℃. This protects the charger from excessive thermal stress at high input voltages.

Power-Good Condition

Even if there is a power present at one of the power input pins, the charger will not deliver power to the battery for charging if three of the conditions below are not met:

- VDC or VUSB> V_{POR}
- VDC or VUSB - $V_{BAT} > V_{OS}$
- VDC or VUSB < V_{OVP}

Where V_{POR} is the power on reset voltage and V_{OS} is the offset voltage of the input-to-output comparator. All of these voltages have hysteresis, as given in the "Electrical Specifications" table on page 2.

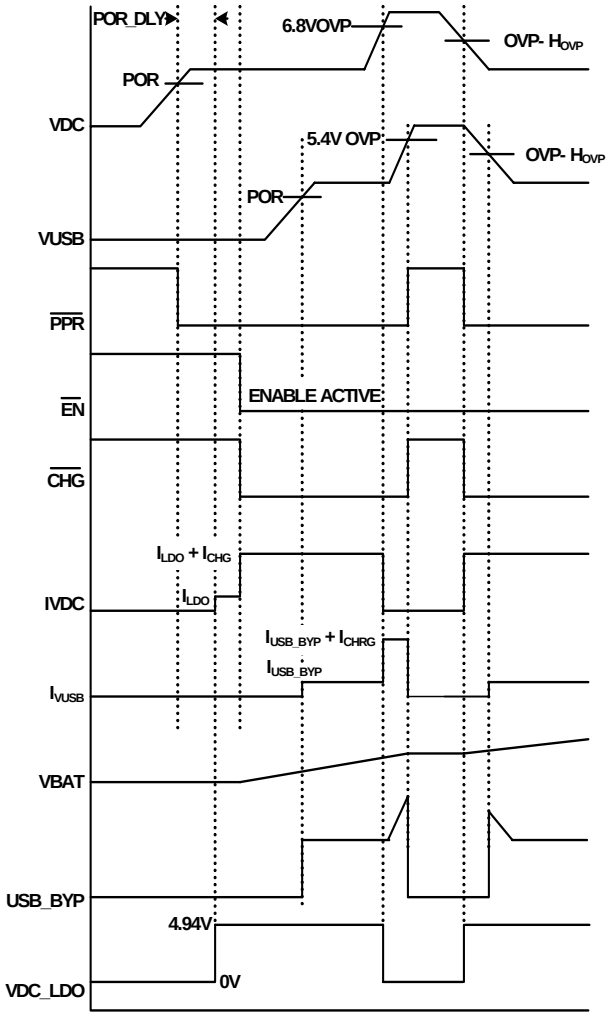


FIGURE 2. . CHARGING PROFILE

Input Bypass Capacitors

Due to the wall or car power adapter power lead inductance, the VDC input capacitor type must be properly selected to prevent high voltage transient during a hot-plug event. This is also true for the USB input capacitor. A tantalum capacitor is a good choice for its high ESR, providing damping to the voltage transient. Multi-layer ceramic capacitors, however

have a very low ESR and hence when chosen as input capacitors, a 1Ω series resistor must be placed between the capacitor and ground, as shown in the Typical Applications Section, to provide adequate damping.

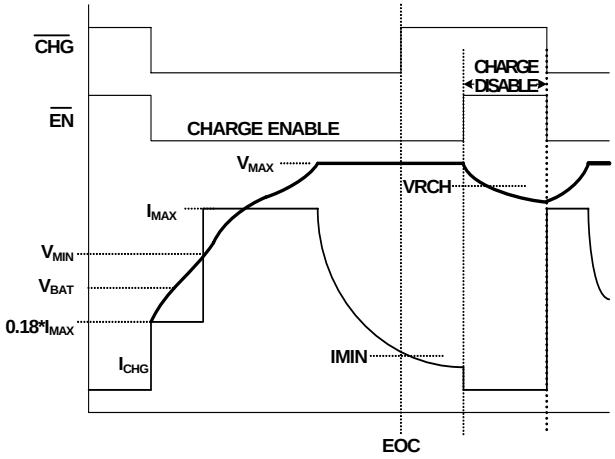


FIGURE 3. TIMING DIAGRAM

Fault Summary

If VDC is greater than 6.8V, then the VDC_LDO and charging FETs are turned off until VDC < V_{OVP} - H_{OVP} (Where H_{OVP} is the OVP hysteresis). PPR will be asserted high (off), unless VUSB is valid.

If VUSB is greater than 5.4V, then the VUSB bypass and charging FETs are turned off until VUSB < V_{OVP} - H_{OVP}. $\overline{PPR}$ will be asserted high (off), unless VDC is valid.

If the load on VUSB_BYP exceeds 400mA, the FET will be current limited to protect the load and the IC.

If V_{USB_BYP} > VUSB, USB Bypass FET is turned off.

State Diagram

The state diagram for the charger functions is shown in Figure 4. The diagram starts with the Power-off state. When at least one input voltage rises above the POR threshold, the charger resets itself. If both input voltages are above the POR threshold, the charger selects the VDC input as the power source. Then if the $\overline{EN}$ pin is at a logic HIGH voltage, the charger will stay in the disabled state. If the $\overline{EN}$ pin is LOW or is brought LOW charging begins. Any time the $\overline{EN}$ pin is asserted high, the charger returns to the disabled state. When the EOC condition is reached, the $\overline{CHG}$ will turn to a logic HIGH to indicate a charge complete status but charging will continue.

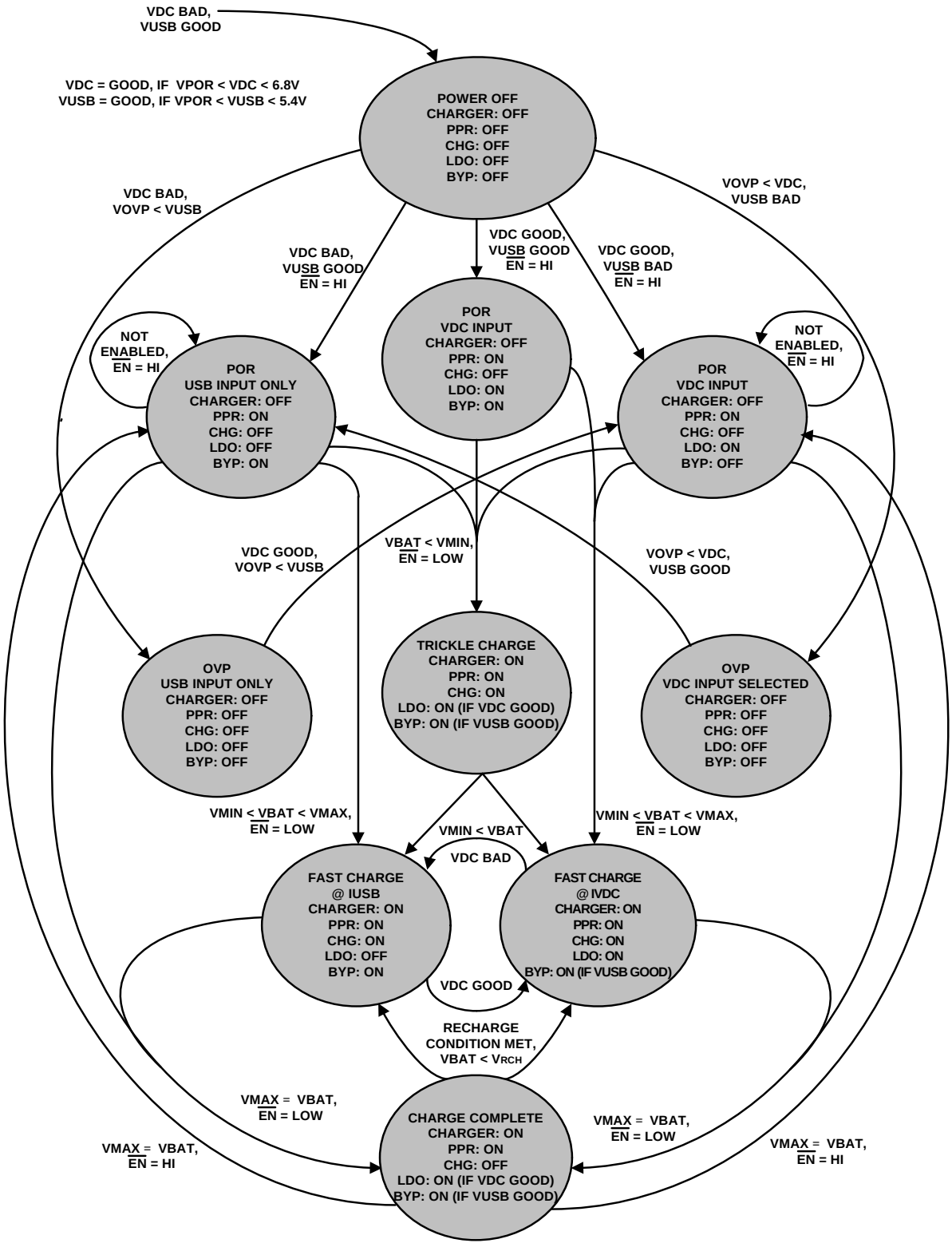


FIGURE 4. STATE DIAGRAM FOR CHARGER FUNCTIONS

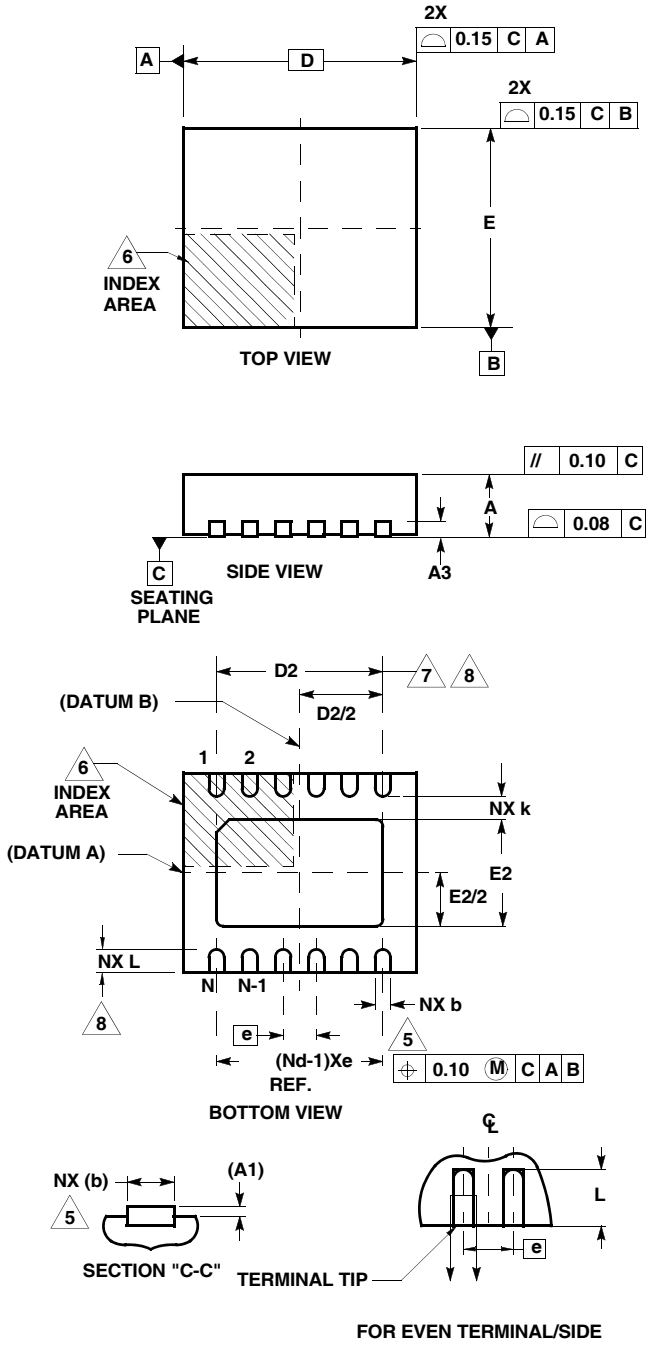
Logic Function State Table

VDC INPUT			USB INPUT								
$V_{IN} < V_{POR}$	PGOOD, $V_{POR} < VDC < V_{OVP}$	$V_{IN} > V_{OVP}$	$V_{IN} < V_{POR}$	PGOOD, $V_{POR} < VUSB < V_{OVP}$	$V_{IN} > V_{OVP}$	$\overline{EN}$	$\overline{PPR}$	$\overline{CHG}$	BAT CHARGING	VDC_LDO OUTPUT	USB_BYP
X		X	X		X	Don't Care	Hi Z	Hi Z	No, Reverse Blocked	No, Reverse Blocked	No, Reverse Blocked
X		X		Yes		Low	Low	Low	Yes, USB Charging	No, reverse blocked	Yes
	Yes		X		X	Low	Low	Low	Yes, VDC Charging	Yes	No, Reverse Blocked
	Yes			Yes		Low	Low	Low	Yes, VDC Charging	Yes	Yes
	Yes		X		X	High (Disables Charging)	Low	Hi Z	No, Reverse Blocked	Yes	No, Reverse Blocked
X		X		Yes		High (Disables Charging)	Low	Hi Z	No, Reverse Blocked	No, reverse blocked	Yes
	Yes			Yes		High (Disables Charging)	Low	Hi Z	No, Reverse Blocked	Yes	Yes

NOTES:

4. "X" denotes that the input is either less than V_{POR} or greater than V_{OVP}
5. VDC_V_{OVP} is a nominal 6.8V
6. VUSB_V_{OVP} is a nominal 5.4V

Dual Flat No-Lead Plastic Package (DFN)



L12.4x3

12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-229-VGED-4 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.30	5,8
D		4.00 BSC		-
D2	3.15	3.30	3.40	7,8
E		3.00 BSC		-
E2	1.55	1.70	1.80	7,8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		12		2
Nd		6		3

Rev. 1 2/05

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.