SMBus/ I^{2}C 8-Channel LED Driver

ISL97677

The ISL97677 is an SMBus/I^{2}C controlled multi-channel LED driver for notebook and monitor LCD backlight applications with PWM dimming and fault reporting functions. The ISL97677 is capable of driving typically 96 pieces of 3.4V/50mA LEDs. The ISL97677 has multiple channels of voltage controlled current sources with typical currents matching to ±0.7%, which compensate for the non-uniformity effect of forward voltages variance in the LED strings. To minimize the voltage headroom and power loss in the typical multi-string operation, the ISL97677 features dynamic headroom control that monitors the highest LED forward voltage string and uses its feedback signal for output regulation.

The ISL97677 can operate in multiple modes of operations. It can be controlled by SMBus/I^{2}C communications and an external PWM dimming signal with currents matching of ±1% across all ranges.

The ISL97677 features extensive protection functions that include string open and short circuit detections, OVP, and OTP. The fault conditions will be recorded in the Fault/Status register. There are selectable short-circuit thresholds and the switching frequency can be programmed between 500kHz and 1.5MHz.

ISL97677 is available in the 32 Leads QFN 5mmx5mm and operate from -40°C to +85°C with input voltage ranges from 4.75V to 26V.

Features

- 8 Channels
- 4.75V ~ 26V Input
- 45V Maximum Output
- Drive Typically 96 LEDs (3.4V/50mA each)
- Dimming Controls
  - SMBus/I^{2}C 8-Bit PWM Dimming
  - SMBus and External PWM DPST Dimming Control
  - External PWM Dimming with or without SMBus/I^{2}C
  - PWM Dimming range from 0.4% to 100%
- Current Matching ±0.7%
- Protections
  - String Open Circuit and Short Circuit Detections, OVP, and OTP
- Adjustable Dimming Frequency
- Adjustable Switching Frequency
- 32 Ld (5mmx5mm) QFN Package

Applications

- Notebook Displays WLED or RGB LED Backlighting
- LCD Monitor LED Backlighting

Typical Application Circuit

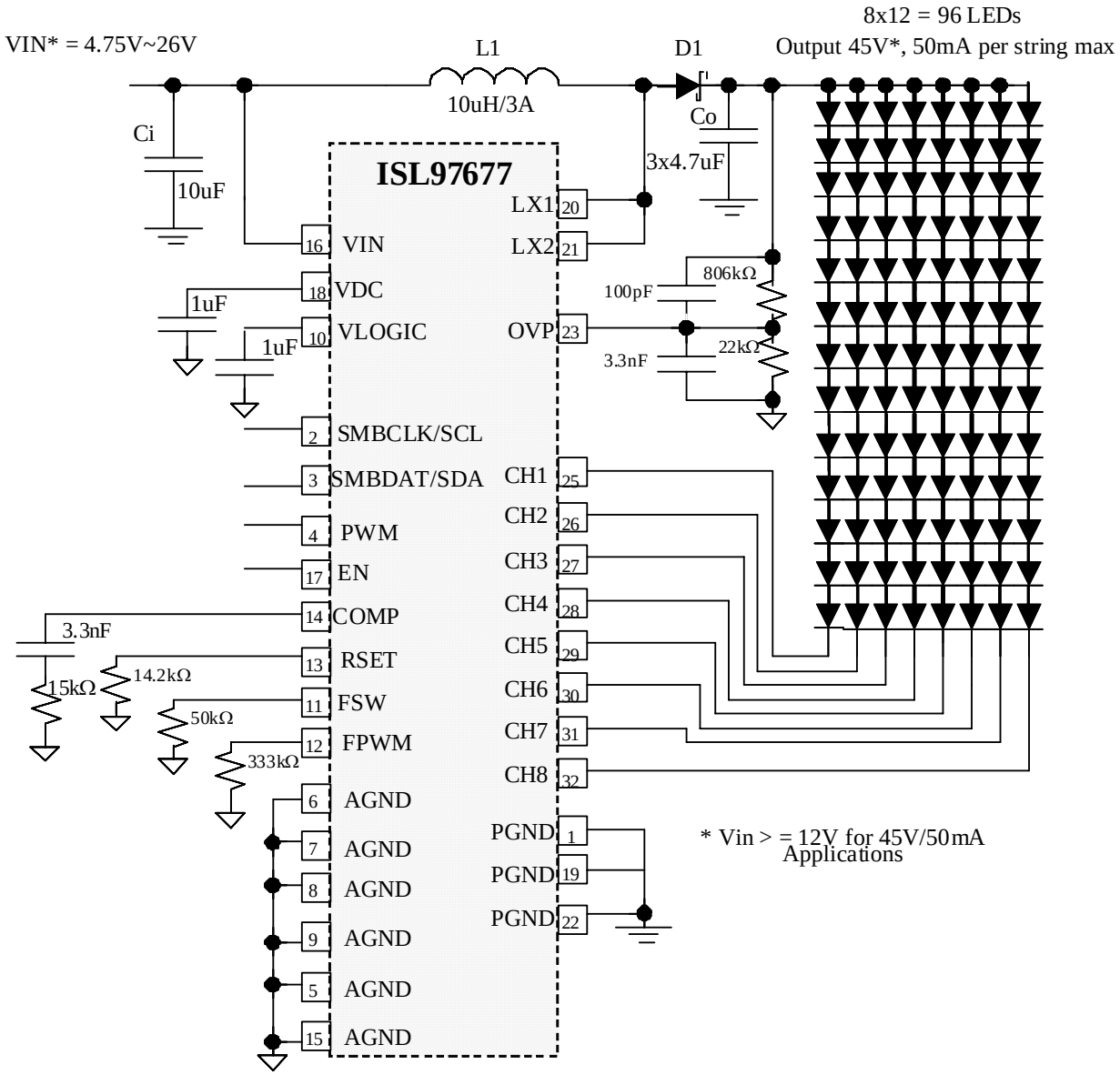


FIGURE 1. ISL97677 TYPICAL APPLICATION DIAGRAM

Block Diagram

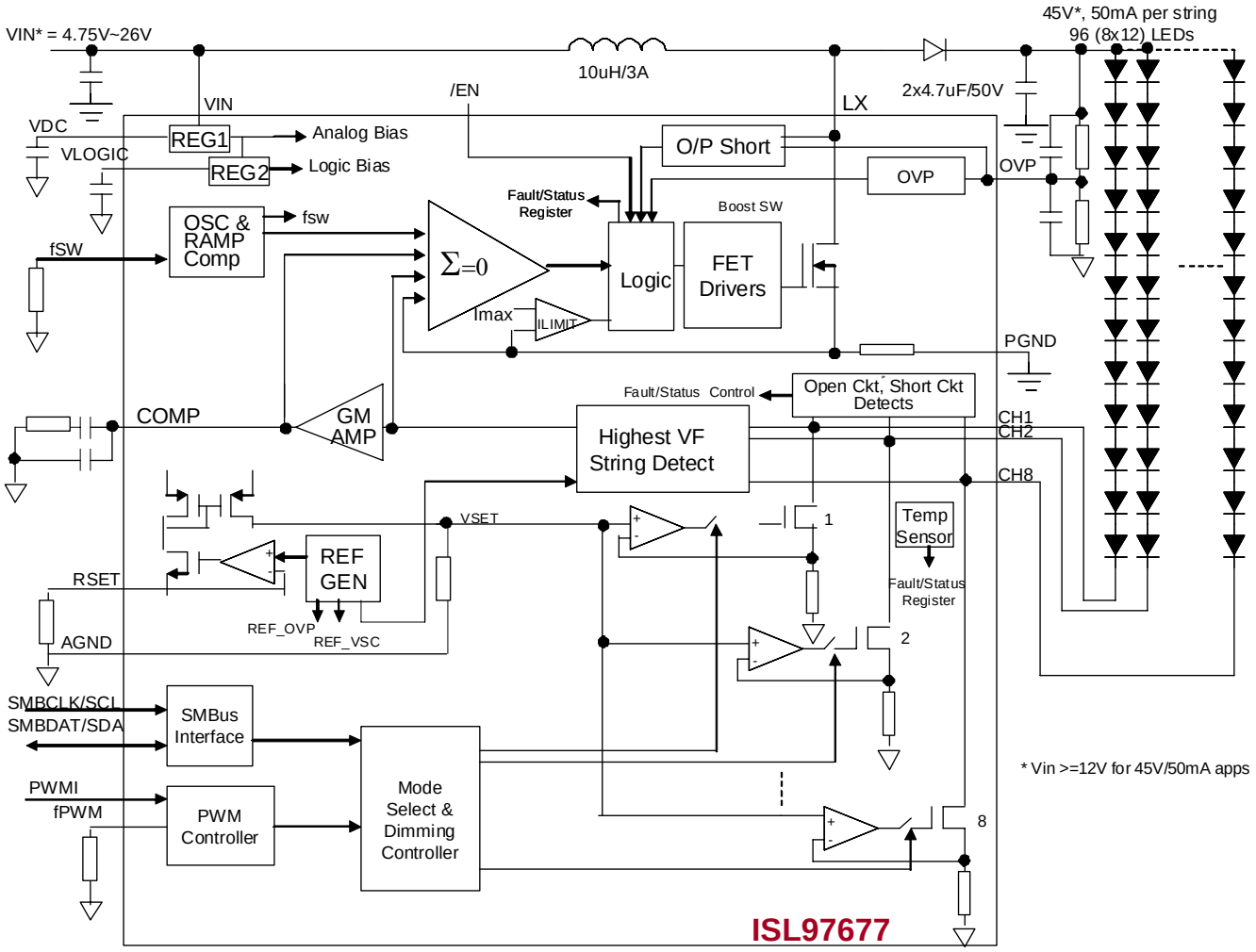


FIGURE 2. ISL97677 BLOCK DIAGRAM

Ordering Information

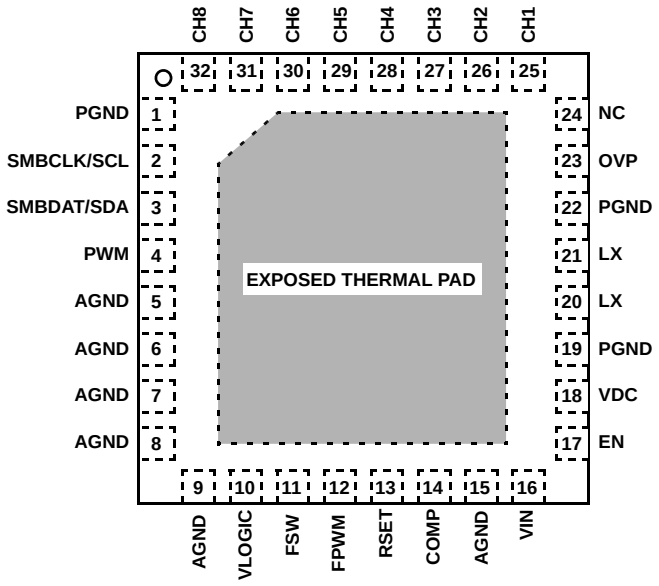
PART NUMBER	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL97677IRZ (Notes 1, 2)	ISL9767 7IRZ	32 Ld 5x5 QFN	L32.5x5B

NOTES:

1. Add “-T” or “-TK” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL97677. For more information on MSL please see techbrief TB363.

Pin Configuration

ISL97677
(32 LD 5X5 QFN)
TOP VIEW



Pin Descriptions (I = Input, O = Output, S = Supply)

PIN	NAME	TYPE	DESCRIPTION
1, 19, 22	PGND	S	Power Ground
2	SMBCLK/SCL	I	SMBus/I^{2}C Serial Clock Input
3	SMBDAT/SDA	I/O	SMBus/I^{2}C Serial Data Input and Output
4	PWM	I	PWM Brightness Control
5, 6, 7, 8, 9, 15	AGND	S	Analog Ground
10	VLOGIC	O	Internal 2.5V Logic Bias Regulator. Need Decoupling Capacitor for Regulation
11	FSW	I	When R_{fSW} is 100kΩ, f_{SW} is 500kHz. When R_{fSW} is 33kΩ, f_{SW} is 1.5MHz
12	FPWM	I	When R_{FPWM} is 333kΩ, F_{PWM} is 200Hz. When R_{FPWM} is 3.3kΩ, F_{PWM} is 20kHz.
13	RSET	I	Resistor Connection for Setting LED Current
14	COMP	O	Boost compensation
16	VIN	S	Main Power
17	EN	I	Enable
18	VDC	S	Internal 5V Analog Bias Regulator. Needs Decoupling Capacitor for Regulation
20, 21	LX	O	Boost MOSFET Drain Terminal Switching Node
23	OVP	I	Overvoltage Protection Input as well as Output Voltage FB Monitoring
24	NC	I/O	No Connect
25 ~ 32	CH1 ~ CH8	I	LED Driver PWM Dimming Monitoring

Absolute Maximum Ratings

voltage ratings are all with respect to AGND pin

VIN . . . . . -0.3V to 27V
EN . . . . . -0.3V to 27V
VLOGIC. . . . . -0.3V to 2.75V
VDC . . . . . -0.3V to 5.75V
COMP, RSET, FPWM, FSW . . . . . -0.3V to min . . . . . (VDC + 0.3V, 5.75V)
SMBCLK, SMBDAT, PWM . . . . . -0.3V to 5.75V
CH1 - CH8, LX, OVP . . . . . -0.3V to 45V
PGND, AGND . . . . . -0.3V to +0.3V

Recommended Operating Conditions

Temperature Range . . . . . -40°C to +85°C

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld QFN (Notes 4, 5)	31	3

Thermal Characterization (Typical, Note 6)	PSI_{JT} (°C/W)
32 Ld QFN	0.2

Maximum Continuous Junction Temperature . . . . . +125°C
Storage Temperature . . . . . -65°C to +150°C
Power Dissipation
T_A < +25°C 3.2W
T_A < +70°C 1.8W
T_A < +85°C 1.3W
T_A < +100°C 0.8W
Pb-Free Reflow Profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
6. PSI_{JT} is the PSI junction-to-top thermal characterization parameter. If the package top temperature can be measured with this rating then the die junction temperature can be estimated more accurately than the θ_{JC} and θ_{JC} thermal resistance ratings.

Electrical Specifications

All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 12V, /SHUT = 5V, I_{SET} = 36kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
GENERAL						
V_{IN}	Backlight Supply Voltage		**4.75**		**26 (Note 8)**	V
I_{VIN_SHDN}	VIN Shutdown Current	/SHUT = 0			**5**	µA
V_{OUT}	Output Voltage				**45**	V
V_{UVLO}	Undervoltage Lockout Threshold		**2.9**		**3.3**	V
V_{UVLO_HYS}	Undervoltage Lockout Hysteresis			300		mV
LINEAR REGULATOR						
V_{DC}	5V Analog Bias Regulator	V_{IN} > 6V	**4.8**	5	**5.1**	V
V_{DC_DROP}	VDC LDO Dropout Voltage	I_{VDC} = 30mA		71	**100**	mV
I_{VDC}	Active Current	/SHUT = 5V, R = 33kΩ		10		mA
V_{LOGIC}	2.5V Logic Bias Regulator	V_{IN} > 6V	**2.3**	2.4	**2.5**	V
V_{LOGIC_DROP}	V_{LOGIC} LDO Dropout Voltage	I_{VLOGIC} = 30mA		31	**100**	mV
BOOST SWITCHING REGULATOR						
SS	Soft-Start			16		ms
SW_{ILimit}	Boost FET Current Limit	T_A = +25°C to +85°C	**3.0**		**4.7**	A
$r_{DS(ON)}$	Internal Boost Switch ON-Resistance			130		mΩ

Electrical Specifications All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 12V, /SHUT = 5V, I_{SET} = 36kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
Eff_peak	Peak Efficiency	V_{IN} = 24V, 96LEDs, 20mA each, L = 10µH with DCR ≤ 100mΩ, f_{SW} = 600kHz, T_A = +25°C		92.4		%
		V_{IN} = 12V, 96 LEDs, 20mA each, L = 10µH with DCR ≤ 100mΩ, f_{SW}= 600kHz, T_A = +25°C		91.5		%
		V_{IN} = 6V, 96 LEDs, 20mA each, L = 10µH with DCR ≤ 100mΩ, f_{SW} = 600kHz, T_A = +25°C		81.6		%
		V_{IN} = 24V, 80 LEDs, 40mA each, L = 10µH with DCR ≤ 100mΩ, f_{SW} = 600kHz, T_A = +25°C		93.4		%
		V_{IN} = 12V, 80 LEDs, 40mA each, L = 10µH with DCR ≤ 100mΩ, f_{SW} = 600kHz, T_A = +25°C		90.7		%
D_{MAX}	Boost Maximum Duty Cycle	f_{SW} = 500kHz	**90**			%
D_{MIN}	Boost Minimum Duty Cycle	f_{SW} = 500kHz			**10**	%
f_{SW}	Boost Switching Frequency	R_{fsw} = 100kΩ	**0.45**	0.5	**0.55**	MHz
		R_{fsw} = 33kΩ	**1.35**	1.5	**1.65**	MHz
ILX_leakage	Lx Leakage Current	VLX = 45V, /SHUT = 0V			**10**	µA
REFERENCE						
I_{MATCH}	Channel-to-Channel Current Matching	I_{LED} = 20mA	**-1.1**	±0.7	**+1.1**	%
I_{ACC}	Absolute Current Accuracy	I_{RSET} = 36kΩ, T_A = +25°C	**-1.5**		**+1.5**	%
		I_{RSET} = 36kΩ, T_A = -40°C to +80°C	**-2**		**+2**	%
FAULT DETECTION						
V_{SC}	Channel Short Circuit Threshold	SMBus Register0x0F, SC[1:0] = 01	**2.4**		**3.6**	V
		SMBus Register0x0F, SC[1:0] = 10	**3.3**		**4.6**	V
		SMBus Register0x0F, SC[1:0] = 11	**4.2**		**5.6**	V
V_{temp}	Over-Temperature Threshold			150		°C
V_{temp_acc}	Over-Temperature Threshold Accuracy			5		°C
V_{OVP}	Overvoltage Limit on OVP Pin		**1.18**	1.22	**1.24**	V

Electrical Specifications All specifications below are characterized at T_A = -40°C to +85°C; V_{IN} = 12V, /SHUT = 5V, I_{SET} = 36kΩ, unless otherwise noted. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	DESCRIPTION	CONDITION	MIN (Note 7)	TYP	MAX (Note 7)	UNIT
SMBus INTERFACE (SMBus Mode, 1D_EN = 0)						
V_{IL}	Logic Input Low Voltage - SMBCLK/SCL, SMBDAT/SDA				**0.8**	V
V_{IH}	Logic Input High Voltage - SMBCLK/SCL, SMBDAT/SDA		**1.5**		**5.5**	V
V_{OL}	SMBus Data Line Logic Low Voltage with 1.1kΩ series resistor from data bus to SMBDAT pin	I_{PULLUP} = 350µA			**0.4**	V
	SMBus Data Line Logic Low Voltage without series resistor from data bus to SMBDAT pin	I_{PULLUP} = 4mA			**0.17**	V
SMBus TIMING SPECIFICATIONS						
f_{SMB}	SMBus Clock Frequency				**250**	kHz
t_{BUF}	Bus Free Time Between Stop and Start Condition		**4.7**			µs
$t_{HD:STA}$	Hold Time After (Repeated) START Condition. After this Period, the First Clock is Generated		**4.0**			µs
$t_{SU:STA}$	Repeated Start Condition Setup Time		**4.7**			µs
$t_{SU:STO}$	Stop Condition Setup Time		**4.0**			µs
$t_{HD:DAT}$	Data Hold Time (Note 9)		300			ns
$t_{SU:DAT}$	Data Setup Time (Note 9)		250			ns
t_{LOW}	Clock Low Period		**4.7**			µs
t_{HIGH}	Clock High Period		**4.0**			µs
t_F	Clock/Data Fall Time (Note 9)				300	ns
CURRENT SOURCES						
$V_{HEADROOM}$	Dominant Channel Current Source Headroom at CH Pin	I_{LED} = 50mA T_A = +25°C		1.0		V
V_{ISET}	Voltage at ISET Pin		**1.18**	1.21	**1.24**	V
ILEDmax	Maximum LED Current per Channel	LED config = 8P10S with VF = 3.4V and V_{IN} = 11V		50		mA
PWM GENERATOR						
FPWM	Generated PWM Frequency	R_{FPWM} = 330kΩ	**180**	200	**220**	Hz
		R_{FPWM} = 3.3kΩ	**18**	20	**22**	kHz
Dimming Range	PWM Dimming Duty Cycle Limits (Note 9)	$f_{PWM} \leq$ 30kHz	0.4		100	%
VFSW	FSW Voltage	R_{FSW} = 33kΩ	**1.18**	1.21	**1.24**	V
FPWMI	PWMI Input Frequency Range (Note 9)		200		20k	**Hz**
VFPWM	VFPWM Voltage	R_{FPWM} = 3.3kΩ	**1.18**	1.21	**1.25**	V

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. At maximum V_{IN} of 26V, minimum V_{OUT} is 28V. Minimum V_{OUT} can be lower at lower V_{IN}
9. Limits established by characterization and are not production tested.

Typical Performance Curves

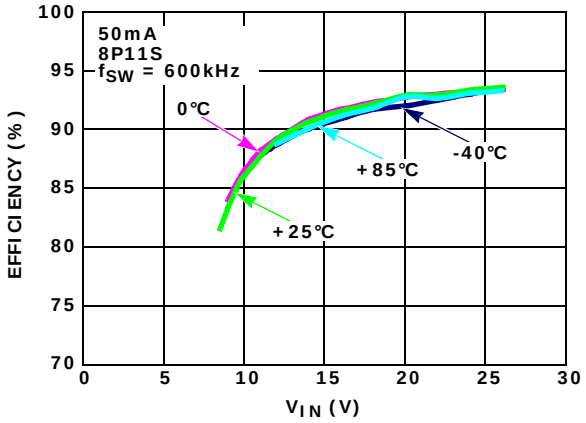


FIGURE 3. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 50mA

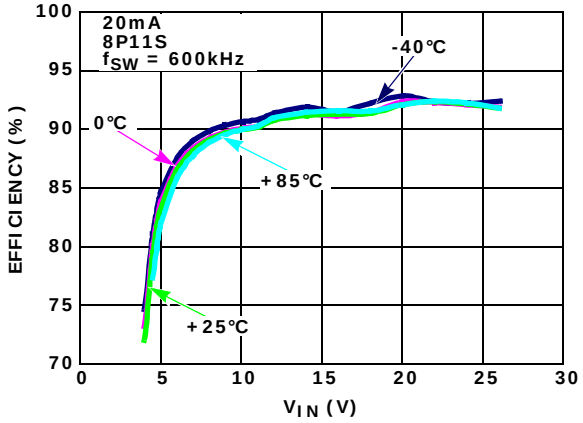


FIGURE 4. EFFICIENCY vs V_{IN} vs TEMPERATURE AT 20mA

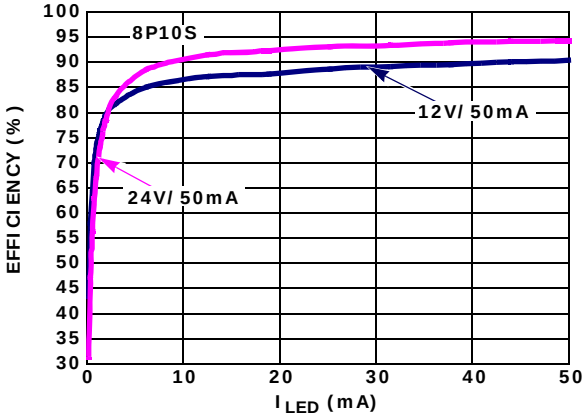


FIGURE 5. EFFICIENCY vs I_{LED}

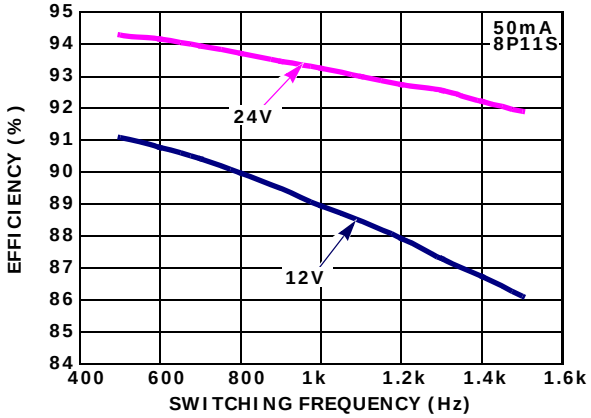


FIGURE 6. EFFICIENCY vs SWITCHING FREQUENCY

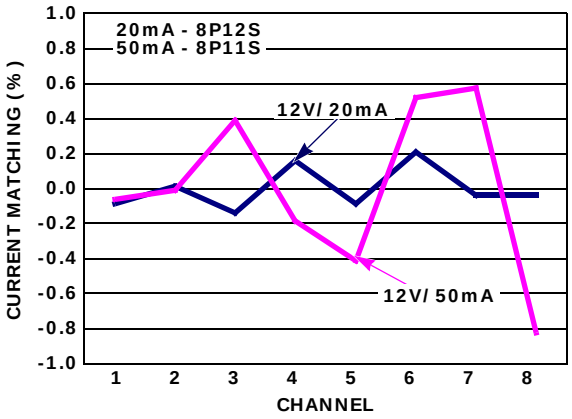


FIGURE 7. CHANNEL-TO-CHANNEL CURRENT MATCHING EXAMPLE

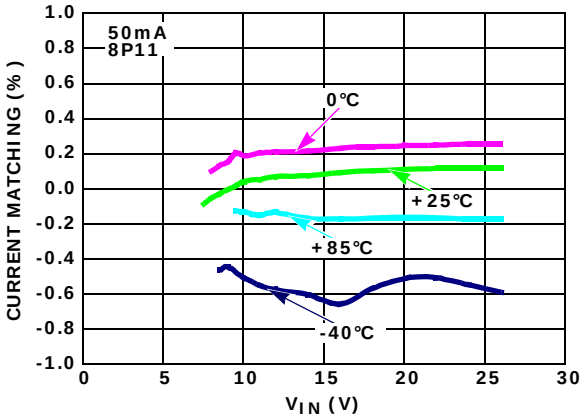


FIGURE 8. CURRENT MATCHING vs V_{IN} vs TEMPERATURE

Typical Performance Curves (Continued)

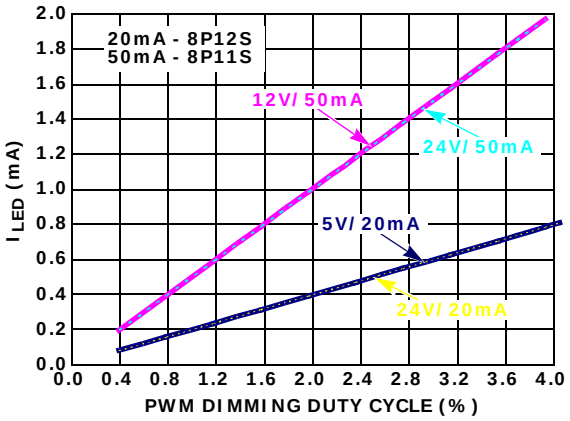


FIGURE 9. CURRENT LINEARITY vs LOW LEVEL PWM DIMMING DUTY CYCLE

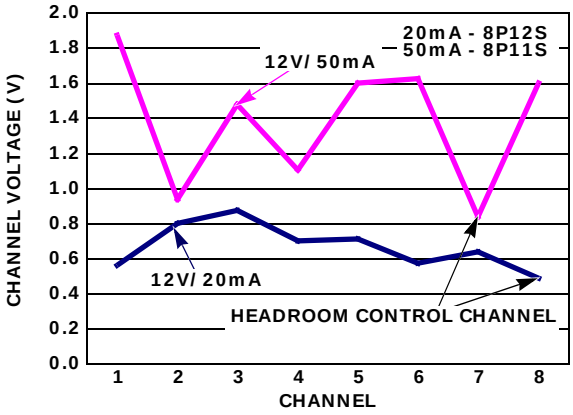


FIGURE 10. TYPICAL CHANNEL VOLTAGE EXAMPLE

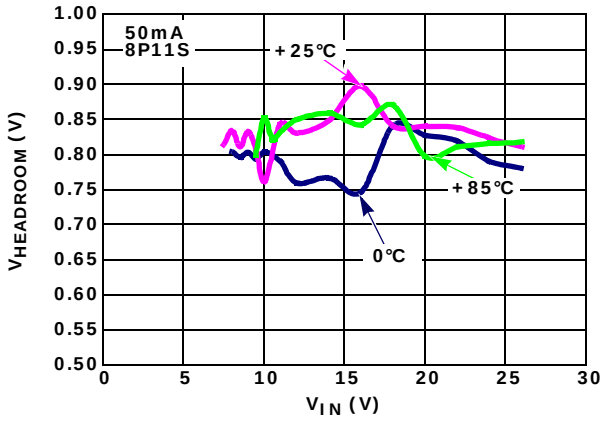


FIGURE 11. $V_{HEADROOM}$ vs V_{IN} vs TEMPERATURE AT 50mA

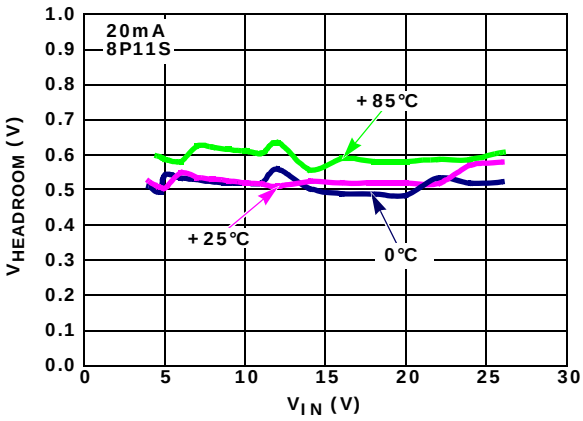


FIGURE 12. $V_{HEADROOM}$ vs V_{IN} vs TEMPERATURE AT 20mA

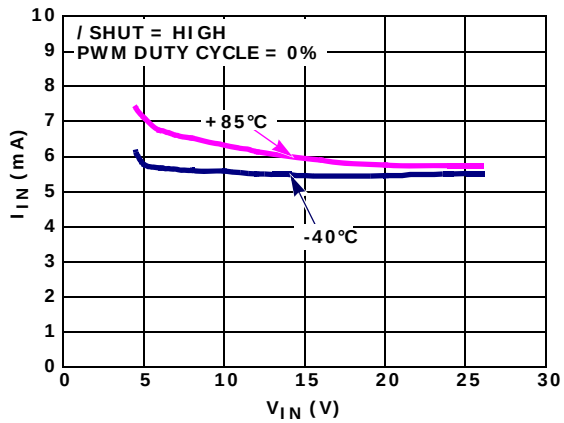


FIGURE 13. QUIESCENT CURRENT vs V_{IN} vs TEMPERATURE WITH / SHUT ENABLE

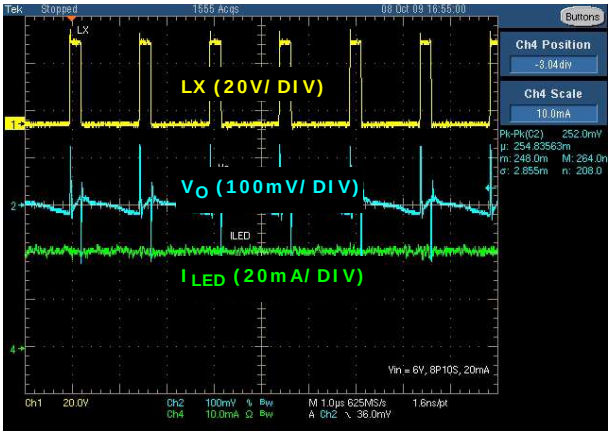


FIGURE 14. V_{OUT} RIPPLE VOLTAGE

Typical Performance Curves (Continued)

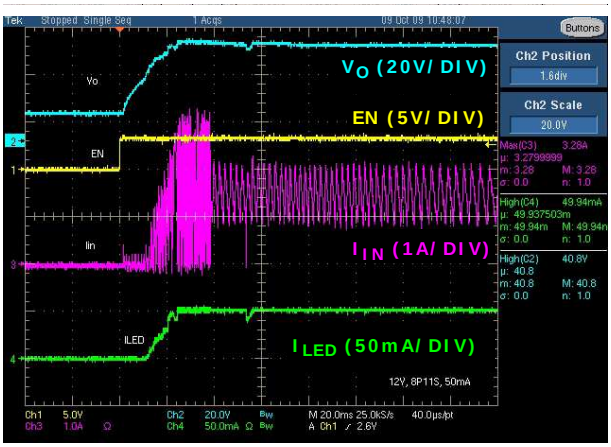


FIGURE 15. IN-RUSH CURRENT and LED CURRENT AT V_{IN} = 12V

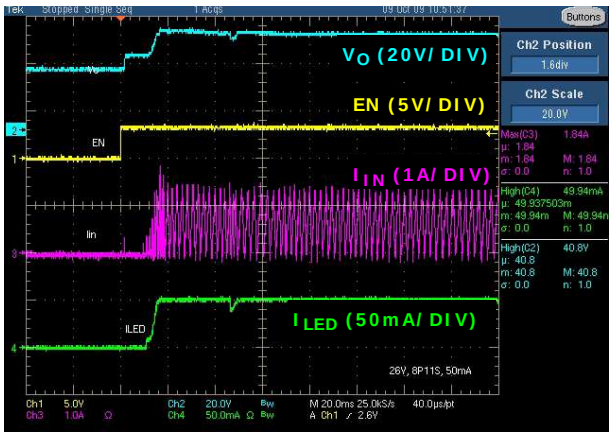


FIGURE 16. IN-RUSH CURRENT AND LED CURRENT AT V_{IN} = 26V

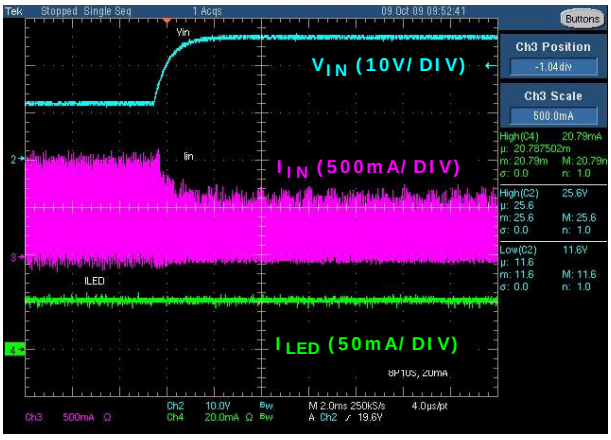


FIGURE 17. LINE REGULATION WITH V_{IN} CHANGES FROM 12V TO 26V DISABLE PROFILE

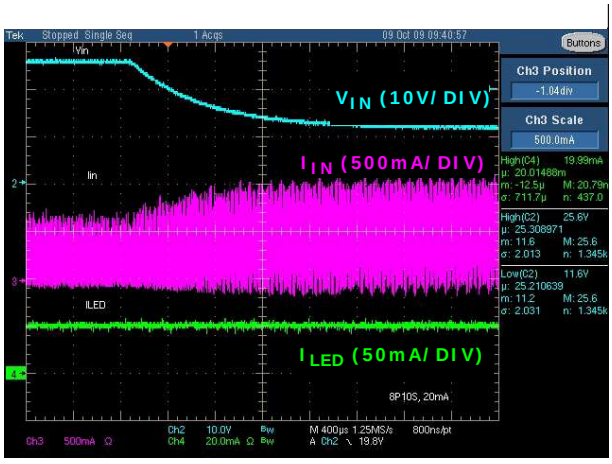


FIGURE 18. LINE REGULATION WITH V_{IN} CHANGES FROM 26V TO 12V

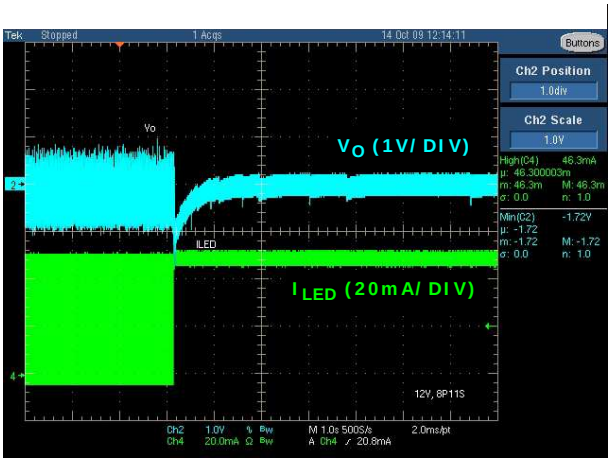


FIGURE 19. LOAD REGULATION WITH I_{LED} CHANGES FROM 0.4% TO 100% PWM DIMMING

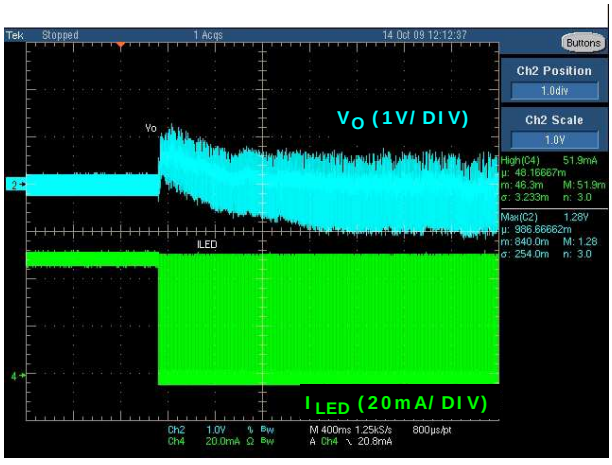


FIGURE 20. LOAD REGULATION WITH I_{LED} CHANGES FROM 100% TO 0.4% PWM DIMMING

Typical Performance Curves (Continued)

FIGURE 21. LOAD REGULATION WITH I_{LED} CHANGES FROM 0% TO 100% PWM DIMMING

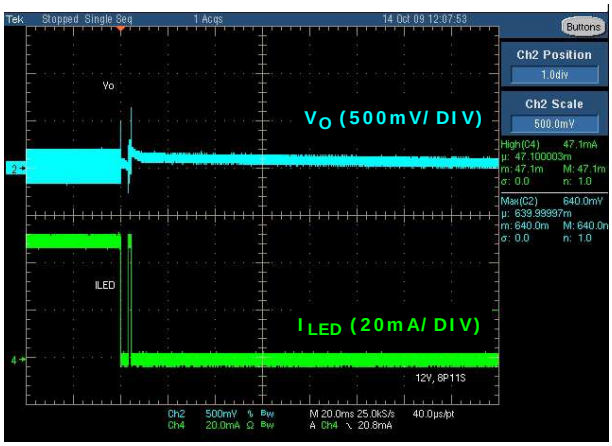


FIGURE 22. LOAD REGULATION WITH I_{LED} CHANGES FROM 100% to 0% PWM DIMMING

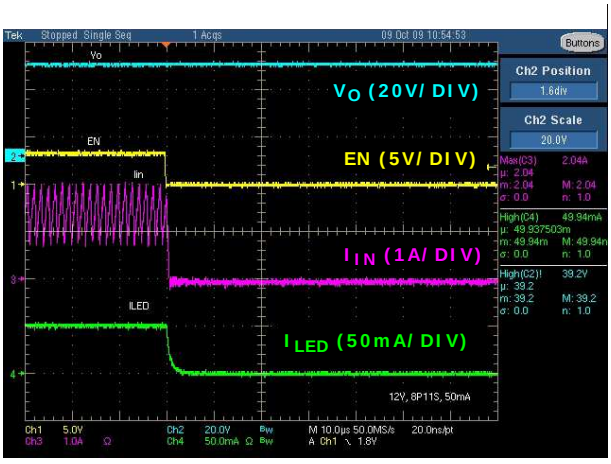


FIGURE 23. DISABLE PROFILE

Theory of Operation

PWM Boost Converter

The current mode PWM boost converter produces the minimal voltage needed to enable the LED string with the highest forward voltage drop to run at the programmed current. The ISL97677 employs current mode control boost architecture that has a fast current sense loop and a slow voltage feedback loop. Such architecture achieves a fast transient response that is essential for the notebook backlight application where the power can be several Li-ion cell batteries or instantly change to an AC/DC adapter without rendering a noticeable visual nuisance. The number of LEDs that can be driven by ISL97677 depends on the type of LED chosen in the application. The ISL97677 is capable of boosting up to 45V and drive 8 channels of LEDs at maximum of 45mA per channel.

Current Matching and Current Accuracy

Each channel of the LED current is regulated by the current source circuit, as shown in Figure 24.

The LED peak current is set by translating the R_{SET} current to the output with a scaling factor of $707.9/R_{SET}$. The source terminals of the current source MOSFETs are designed to run at 500mV to optimize power loss vs accuracy requirements. The sources of errors of the channel-to-channel current matching come from the op amps offset, internal layout, reference, and current source resistors. These parameters are optimized for current matching and absolute current accuracy. However, the absolute accuracy is additionally determined by the external R_{SET}. A 0.1% tolerance resistor is recommended.

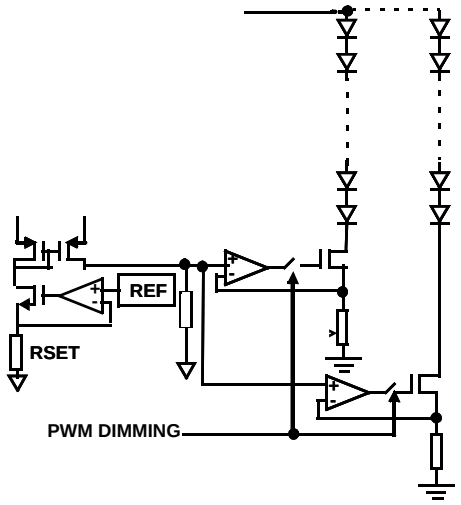


FIGURE 24. SIMPLIFIED CURRENT SOURCE CIRCUIT

Dynamic Headroom Control

The ISL97677 features a proprietary Dynamic Headroom Control circuit that detects the highest forward voltage string or effectively the lowest voltage from any of the CH pins. When this lowest I_{IN} voltage is lower than the short circuit threshold, V_{SC}, such voltage will be used as the feedback signal for the boost regulator. The boost makes the output to the correct level such that the lowest CH pin is at the target headroom voltage. Since all LED strings are connected to the same output voltage, the other CH pins will have a higher voltage, but the regulated current source circuit on each channel will ensure that each channel has the same programmed current. The output voltage will regulate cycle by cycle and is always referenced to the highest forward voltage string in the architecture.

OVP and V_{OUT} Requirement

The Overvoltage Protection (OVP) pin has a function of setting the overvoltage trip level as well as limiting the V_{OUT} regulation range.

The ISL97677 OVP threshold is set by R_{UPPER} and R_{LOWER} as shown in Equation 1:

$$V_{OUT\_OVP} = 1.21V \times (R_{UPPER} + R_{LOWER})/R_{LOWER} \quad \text{(EQ. 1)}$$

V_{OUT} can only regulate between 64% and 100% of the V_{OUT_OVP} such that:

Allowable V_{OUT} = 64% to 100% of V_{OUT_OVP}

For example, if 10 LEDs are used with the worst case V_{OUT} of 35V. If R_1 and R_2 are chosen such that the OVP level is set at 40V, then the V_{OUT} is allowed to operate between 25.6V and 40V. If the requirement is changed to a 6 LEDs 21V V_{OUT} application, then the OVP level must be reduced and users should follow V_{OUT} = (64% ~ 100%)OVP requirement. Otherwise, the headroom control will be disturbed such that the channel voltage can be much higher than expected and sometimes it can prevents the driver from operating properly.

The ratio of the OVP capacitors should be the inverse of the OVP resistors. For example, if R_{UPPER}/R_{LOWER} = 33/1, then C_{UPPER}/C_{LOWER}= 1/33 with C_{UPPER} = 100pF and C_{LOWER} = 3.3nF.

Dimming Controls

The ISL97677 allows two ways of controlling the LED current, and therefore, the brightness. They are:

1. DC current adjustment
2. PWM chopping of the LED current defined in Step 1.

There are various ways to achieve DC or PWM current control, which will be described in the following.

In any dimming controls, the EN pin must be high. EN is a high voltage pin that can be applied with a digital signal or tied directly to V_{IN} for enable function.

MAXIMUM DC CURRENT SETTING

The initial brightness should be set by choosing an appropriate value for R_{SET}. This should be chosen to fix the maximum possible LED current:

$$I_{LEDmax} = \frac{707.9}{R_{SET}} \quad \text{(EQ. 2)}$$

Alternatively, the R_{SET} can be replaced by digital potentiometer for adjustable current. On the other hand, the current accuracy is designed when RSET is set at 20m to 40mA.

PWM CONTROL

The ISL97677 also provides PWM dimming by PWM chopping of the current in the LEDs for all 8 channels to provide an average LED current. During the On periods, the LED current will be defined by the value of R_{SET}, as described in Equation 1.

PWM Dimming Frequency Adjustment

The dimming frequencies of all modes are set by an external resistor at the FPWM pin as shown in Equation 3:

$$f_{PWM} = \frac{6.66 \times 10^7}{RPWM} \quad \text{(EQ. 3)}$$

where f_{PWM} is the desirable PWM dimming frequency and R_{FPWM} is the setting resistor.

External PWM Dimming

The ISL97677 can operate as basic PWM dimming LED driver with or without the need of SMBus/I^2C interface. To do so, users need to set EN = high and SMBCLK/SCL = grounded or floating, SMBDAT/SDA = grounded or floating. The EN is a high voltage pin that can be applied with a digital I/O signal or tie to V_{IN}. The PWM output will follow the PWM input and the dimming frequency will be set by R_{PWM}.

Switching Frequency

The boost switching frequency can be adjusted by a resistor as shown in Equation 4:

$$f_{SW} = \frac{(5\times10^{10})}{R_{OSC}} \quad \text{(EQ. 4)}$$

where f_{SW} is the desirable boost switching frequency and R_{OSC} is the setting resistor.

5V and 2.3V Low Dropout Regulators

A 5V LDO regulator is present at the VDC pin to develop the necessary low voltage supply, which is used by the chips internal control circuitry. Because VDC is an LDO pin, it requires a bypass capacitor of 1µF or more for the regulation. The VDC pin can be used for a coarse regulator or reference but do not pull more than few mA from it.

Similarly, a 2.3V LDO regulator is present at the VLOGIC pin to develop the necessary low voltage supply for the chip's internal logic control circuitry. A 1µF bypass capacitor or more is needed for regulation. The VLOGIC pin can be used as a coarse regulator or reference but do not pull more than few mA from it.

Soft-Start

The ISL97677 uses a digital soft-start where the boost current limit is stepped up in 8 steps. The initial current limit level is set to one ninth of the full current limit, with subsequent steps increasing this by a ninth every 2ms. In the event that no LEDs have been conducting during the interval since the last step (for example, if the LEDs are running at low duty cycle at low PWM frequency) then the step will be delayed until the LEDs are conducting. If the LEDs are disabled and re-enabled again then soft start will be restarted when the LEDs are enabled.

Fault Protection and Monitoring

The ISL97677 features extensive protection functions to cover all the perceivable failure conditions. The failure mode of a LED can be either open circuit or as a short. The behavior of an open circuited LED can additionally take the form of either infinite resistance or, for some LEDs, a zener diode, which is integrated into the device in parallel with the now opened LED.

For basic LEDs (which do not have built-in zener diodes), an open circuit failure of an LED will only result in the loss of one channel of LEDs without affecting other channels. Similarly, a short circuit condition on a channel that results in that channel being turned off does not affect other channels unless a similar fault is occurring. All LED faults are reported via the SMBus interface to Register 0x02 (Fault/Status register).

Due to the lag in boost response to any load change at its output, certain transient events (such as significant step changes in LED duty cycle) can transiently look like LED fault modes. The ISL97677 uses feedback from the LEDs to determine when it is in a stable operating region and prevents apparent faults during these transient events from allowing any of the LED strings to fault out. See Table 1 for more details.

Short Circuit Protection (SCP)

The short circuit detection circuit monitors the voltage on each channel and disables faulty channels which are detected above the programmed short circuit threshold. There are three selectable levels of short circuit threshold (3V, 4V, and 5V) that can be programmed through the Configuration Register 0x0F. When an LED becomes shorted, the action taken is described in Table 1. The default short circuit threshold is 4V. The detection of this failure mode can be disabled by SMBus interface via Register 0x0F.

Open Circuit Protection (OCP)

When one of the LEDs becomes open circuit, it can behave as either an infinite resistance or a gradually increasing finite resistance. The ISL97677 monitors the current in each channel such that any string which reaches the intended output current is considered "good". Should the current subsequently fall below the target, the channel will be considered an "open circuit". Furthermore, should the boost output of the ISL97677 reach the OVP limit or should the lower over-temperature threshold be reached, all channels which are not "good" will immediately be considered as "open circuit". Detection of an "open circuit" channel will result in a time-out before disabling of the affected channel.

Some users employ some special types of LEDs that have zener diode structure in parallel with the LED for ESD enhancement, thus enabling open circuit operation. When this type of LED goes open circuit, the effect is as if the LED forward voltage has increased, but no light will be emitted. Any affected string will not be disabled, unless the failure results in the boost OVP limit being reached, allowing all other LEDs in the string to remain functional. Care should be taken in this case that the boost OVP limit and SCP limit are set properly, so as to make sure that multiple failures on one string do not cause all other good channels to be faulted out. This is due to the increased forward voltage of the faulty channel making all other channel look as if they have LED shorts. See Table 1 for details for responses to fault conditions.

Overvoltage Protection (OVP)

The integrated OVP circuit monitors the output voltage and keeps the voltage at a safe level. The OVP threshold is set as shown in Equation 5:

$$OVP = 1.21V \times (R_{UPPER} + R_{LOWER})/R_{LOWER} \quad \text{(EQ. 5)}$$

These resistors should be large to minimize the power loss. For example, a 1MkΩ R_{UPPER} and 30kΩ R_{LOWER} sets OVP to 41.2V. Large OVP resistors also allow C_{OUT} discharges slowly during the PWM Off time. Parallel capacitors should be placed across the OVP resistors such that $R_{UPPER}/R_{LOWER} = C_{LOWER}/C_{UPPER}$. Using a C_{UPPER} value of at least 30pF is recommended. These

capacitors reduce the AC impedance of the OVP node, which is important when using high value resistors.

Undervoltage Lockout

If the input voltage falls below the UVLO level of 2.8V, the device will stop switching and be reset. Operation will restart only if the device control interface re-enables it once the input voltage is back in the normal operating range. Also all digital settings will be reset to their default states.

Over-Temperature Protection (OTP)

The ISL97677 includes two over-temperature thresholds. The lower threshold is set to +130°C. When this threshold is reached, any channel which is outputting current at a level significantly below the regulation target will be treated as "open circuit" and disabled after a time-out period. The intention of the lower threshold is to allow bad channels to be isolated and disabled before they cause enough power dissipation (as a result of other channels having large voltages across them) to hit the upper temperature threshold.

The upper threshold is set to +150°C. Each time this is reached, the boost will stop switching and the output current sources will be switched off and stay off until the control interface disables and re-enables it. Hitting of the upper threshold will also set the thermal fault bit of the Fault/Status register 0x02. Unless disabled via the /SHUT pin, the device stays in an active state throughout, allowing the external processor to interrogate the fault condition.

For the extensive fault protection conditions, please refer to Figure 25 and Table 1 for details.

Shutdown

When the EN pin is low the entire chip is shut down to give close to zero shutdown current. The digital interfaces will not be active during this time.

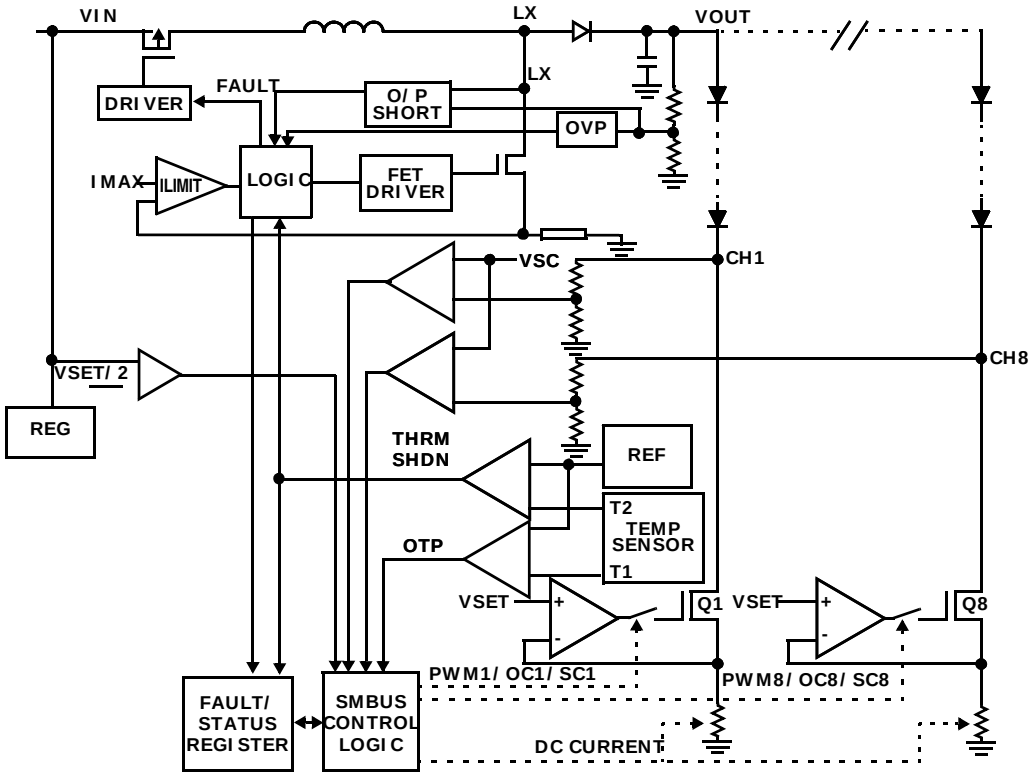
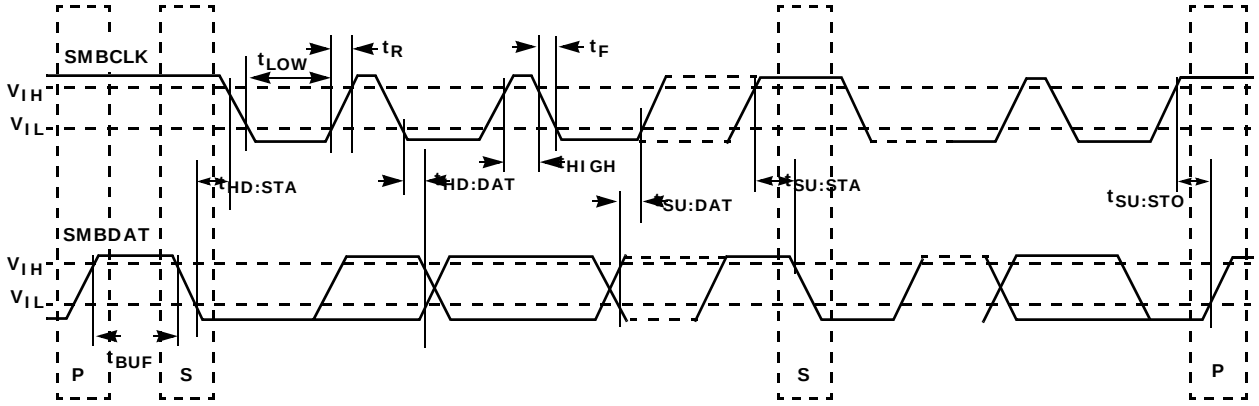


FIGURE 25. SIMPLIFIED FAULT PROTECTIONS

TABLE 1. PROTECTIONS TABLE

CASE	FAILURE MODE	DETECTION MODE	FAILED CHANNEL ACTION	GOOD CHANNELS ACTION	V_{OUT} REGULATED BY
1	CH1 Short Circuit	Upper Over-Temperature Protection limit (OTP) not triggered and VI_{IN0} < VSC	CH1 ON and burns power	CH2 through CH8 Normal	Highest VF of CH2 through CH8
2	CH1 Short Circuit	Upper OTP triggered but V_{IN1} < VSC	CH1 goes off	Same as CH1	Highest VF of CH2 through CH8
3	CH1 Short Circuit	Upper OTP not triggered but VI_{IN1} > VSC	CH1 disabled after 6 PWM cycles time-out.	If 3 channels are already shut down, all channels will be shut down. Otherwise CH2-8 will remain as normal	Highest VF of CH2 through CH8
4	CH1 Open Circuit with infinite resistance	Upper OTP not triggered and VIIN1 < VSC	V_{OUT} will ramp to OVP. CH1 will time-out after 6 PWM cycles and switch off. V_{OUT} will drop to normal level.	CH2 through CH8 Normal	Highest VF of CH2 through CH8
5	CH1 LED Open Circuit but has paralleled Zener	Upper OTP not triggered and VI_{IN1} < VSC	CH1 remains ON and has highest VF, thus V_{OUT} increases	CH2 through CH8 ON, Q2 through Q8 burn power	VF of CH1
6	CH1 LED Open Circuit but has paralleled Zener	Upper OTP triggered but VI_{IN1} < VSC	CH1 goes off	Same as CH1	VF of CH1
7	CH1 LED Open Circuit but has paralleled Zener	Upper OTP not triggered but VIIN1 > VSC	CH1 OFF	CH2 through CH8 Normal	Highest VF of CH2 through CH8
		Upper OTP not triggered but VIINx > VSC	CH1 remains ON and has highest VF, thus V_{OUT} increases.	V_{OUT} increases then CH-X switches OFF. This is an unwanted shut off and can be prevented by setting OVP and/or VSC at an appropriate level.	VF of CH1
8	Channel-to-Channel ΔVF too high	Lower OTP triggered but VIINx < VSC	Any channel at below the target current will fault out after 6 PWM cycles. Remaining channels driven with normal current.		Highest VF of CH1 through CH8
9	Channel-to-Channel ΔVF too high	Upper OTP triggered but VIINx < VSC	All channels switched off		Highest VF of CH1 through CH8
10	Output LED string voltage too high	V_{OUT} > VOVP	Driven with normal current. Any channel that is below the target current will time-out after 6 PWM cycles.		Highest VF of CH1 through CH8
11	V_{OUT}/LX shorted to GND		LX will not switch		



NOTES:

SMBus Description

S = Start condition

P = Stop condition

A = Acknowledge

$\overline{A}$ = Not acknowledge

R/$\overline{W}$ = Read enable at high; Write enable at low

FIGURE 26. SMBUS INTERFACE

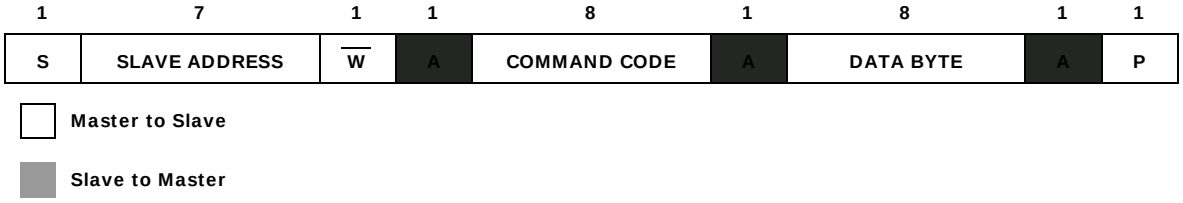


FIGURE 27. WRITE BYTE PROTOCOL

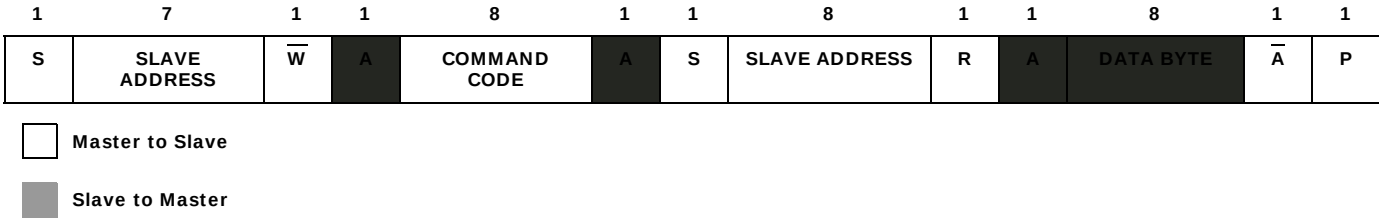


FIGURE 28. READ BYTE PROTOCOL

Write Byte

The Write Byte protocol is only three bytes long. The first byte starts with the slave address followed by the "command code," which translates to the "register index" being written. The third byte contains the data byte that must be written into the register selected by the "command code". A shaded label is used on cycles during which the slaved backlight controller "owns" or "drives" the Data line. All other cycles are driven by the "host master."

Read Byte

As shown in the Figure 28, the four byte long Read Byte protocol starts out with the slave address followed by the "command code" which translates to the "register index." Subsequently, the bus direction turns around with the rebroadcast of the slave address with bit 0 indicating a read ("R") cycle. The fourth byte contains the data being returned by the backlight controller. That byte value in the data byte reflects the value of the register being queried at the "command code" index. Note the bus directions, which are highlighted by the shaded label that is used on cycles during which the slaved backlight controller "owns" or "drives" the Data line. All other cycles are driven by the "host master."

Slave Device Address

The slave address contains 7 MSB plus one LSB as R/W bit, but these 8 bits are usually called Slave Address bytes. As shown in Figure 29, the high nibble of the slave address byte is 0x5 or 0101b to denote the "backlight controller class." Bit 3 in the lower nibble of the slave address byte is 1. Bit 0 is always the R/W bit, as specified by the SMBus protocol. Note: In this document, the device address will always be expressed as a full 8-bit address instead of the shorter 7-bit address typically used in other backlight controller specifications to avoid confusion. Therefore, if the device is in the write mode where bit 0 is 0, the slave address byte is 0x58 or 01011000b. If the device is in the read mode where bit 0 is 1, the slave address byte is 0x59 or 01011001b.

The backlight controller may sense the state of the pins at POR or during normal operation—the pins will not change state while the device is in operation.

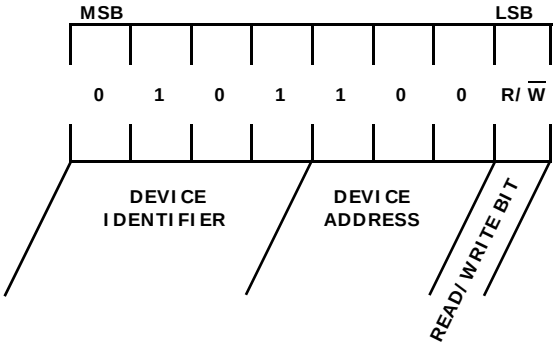


FIGURE 29. SLAVE ADDRESS BYTE DEFINITION

SMBus Register Definitions

The backlight controller registers are Byte wide and accessible via the SMBus Read/Write Byte protocols. Their bit assignments are provided in the following sections with reserved bits containing a default value of "0".

TABLE 2A. REGISTER LISTING

ADDRESS	REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	DEFAULT VALUE	SMBUS PROTOCOL
0x00	PWM Brightness Control Register	BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0	0xFF	Read and Write
0x01	Device Control Register	Reserved	Reserved	Reserved	Reserved	Reserved	PWM_MD	PWM_SEL	BL_CTL	0x00	Read and Write
0x02	Fault/Status Register	Reserved	Reserved	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	FAULT	0x00	Read Only
0x03	Identification Register	LED PANEL	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0	0xC8	Read Only

TABLE 2B. DATA BIT DESCRIPTIONS

ADDRESS	REGISTER	DATA BIT DESCRIPTIONS
0x00	PWM Brightness Control Register	BRT[7..0] = 256 steps of DPWM duty cycle brightness control
0x01	Device Control Register	PWM_MD = PWM mode select bit (1 = absolute brightness, 0 = % change), default = 0 PWM_SEL = Brightness control select bit (1 = control by PWMI, 0 = control by SMBus), default = 0 BL_CTL = BL On/Off (1 = On, 0 = Off), default = 0
0x02	Fault/Status Register	2_CH_SD = Two LED output channels are shutdown (1 = shutdown, 0 = OK) 1_CH_SD = One LED output channel is shutdown (1 = shutdown, 0 = OK) BL_STAT = BL status (1 = BL On, 0 = BL Off) OV_CURR = Input overcurrent (1 = Overcurrent condition, 0 = Current OK) THRM_SHDN = Thermal Shutdown (1 = Thermal fault, 0 = Thermal OK) FAULT = Fault occurred (Logic "OR" of all of the fault conditions)
0x03	Identification Register	MFG[3..0] = Manufacturer ID (16 vendors available. Intersil is vendor ID 9) REV[2..0] = Silicon rev (Rev 0 through Rev 7 allowed for silicon spins)

PWM_MD	PWM_SEL	MODE
X	1	PWMI Mode
1	0	SMBus Mode
0	0	SMBus and PWMI mode with DPST

PWM Brightness Control Register (0x00)

The Brightness control resolution has 256 steps of PWM duty cycle adjustment. The bit assignment is shown in Tables 2A and 2B. All of the bits in this Brightness Control Register can be read or write. Step 0 corresponds to the minimum step where the current is less than 10µA. Steps 1 to 255 represent the linear steps between 0.39% and 100% duty cycle with approximately 0.39% duty cycle adjustment per step.

- An SMBus Write Byte cycle to Register 0x00 sets the PWM brightness level only if the backlight controller is in SMBus mode (see Table 3 "Operating Modes selected by Device Control Register Bits 1 and 2").
- An SMBus Read Byte cycle to Register 0x00 returns the programmed PWM brightness level, regardless of the value of PWM_SEL.
- An SMBus setting of 0xFF for Register 0x00 sets the backlight controller to the maximum brightness.
- An SMBus setting of 0x00 for Register 0x00 sets the backlight controller to the minimum brightness output in which the LED current is guaranteed to be less than 10µA.
- Default value for Register 0x00 is 0xFF.

Device Control Register (0x01)

This register has 2 bits that control the operating mode of the backlight controller and a single bit that controls the BL ON/OFF state. The remaining bits are reserved. The bit assignment is shown in Tables 2A and 2B. All other bits in the Device Control Register will read as low unless otherwise written. Bits 7 and 6 are not implemented and will always read low.

TABLE 3. OPERATING MODES SELECTED BY DEVICE CONTROL REGISTER BITS 1 AND 2

PWM_MD	PWM_SEL	MODE
X	1	PWMI Mode
1	0	SMBus Mode
0	0	SMBus and PWMI Mode with DPST

The PWM_SEL bit determines whether the SMBus or PWMI input should drive the output brightness in terms of PWM dimming. When PWM_SEL bit is 1, the PWMI drives the output brightness regardless of what the PWM_MD is.

When the PWM_SEL bit is 0, the PWM_MD bit selects the manner in which the PWM dimming is to be interpreted; when this bit is 1, the PWM dimming is based on the SMBus brightness setting. When this bit is 0, the PWM dimming reflects a percentage change in the current brightness programmed in the SMBus Register 0x00, i.e. DPST (Display Power Saving Technology) mode, as shown in Equation 6:

$$\text{DPST Brightness} = \text{Cbt} \times \text{PWMI} \quad \text{(EQ. 6)}$$

Where:

Cbt = Current brightness setting from SMBus Register 0x00 without influence from the PWMI

PWMI = is the percent duty cycle of the PWMI

For example, the Cbt = 50% duty cycle programmed in the SMBus Register 0x00 and the PWM frequency is tuned to be 200Hz with an appropriate capacitor at the FPWM pin. On the other hand, PWMI is fed with a 1kHz 30% high PWM signal. When PWM_SEL = 0 and PWM_MD = 0, the device is in DPST operation where DPST brightness = 15% PWM dimming at 200Hz.

- All reserved bits return a “0” when read.
- All reserved bits have no functional effect when written.
- All defined control bits return their current, latched value when read.
- A value of 1 written to BL_CTL turns on the BL in4ms or less after the write cycle completes. The BL is deemed to be on when Bit 3 BL_STAT of Register 0x02 is 1 and Register 0x09 is not 0. See Tables 2A and 2B.
- A value of 0 written to BL_CTL immediately turns off the BL. The BL is deemed to be off when Bit 3 BL_STAT of Register 0x02 is 0 and Register 0x09 is 0. See Tables 2A and 2B.
- **Note that the behavior of Register 0x00 (Brightness Control Register) is affected by certain combinations of the control bits, as shown in Table 3 “Operating Modes Selected by Device Control Register Bits 1 and 2.”
- When an SMBus mode is selected, Register 0x00 reflects the last value written to it. But, when any non-SMBus mode is selected, Register 0x00 reflects the current brightness value based on the current mode of operation, with the exception of SMBus mode with DPST, where PWM_MD = 0 and PWM_SEL = 0.
- When SMBus mode with DPST is selected, Register 0x00 reflects the last value written to it from SMBus.
- When a write to Register 0x01 (Device Control Register) causes the backlight controller to transition to an SMBus mode, the brightness of the BL does not change. On the other hand, when a write to Register 0x01causes the backlight controller to transition to a non-SMBus mode, the brightness of the BL changes as appropriate for the new mode.
- The default value for Register 0x01 is 0x00.

Fault/ Status Register (0x02)

This register has 6 status bits that allow monitoring of the backlight controller’s operating state. Bit 0 is a logical “OR” of all fault codes to simplify error detection. Not all of the bits in this register are fault related (Bit 3 is a simple BL status indicator). The remaining bits are reserved and return a “0” when read and ignore the bit value when written. All of the bits in this register are read-only, with the exception of bit 0, which can be cleared by writing to it.

- A Read Byte cycle to Register 0x02 indicates the current BL on/off status in BL_STAT (1 if the BL is on, 0 if the BL is off).
- A Read Byte cycles to Register 0x2 also returns FAULT as the logical OR of THRM_SHDN, OV_CURR, 2_CH_SD, and 1_CH_SD should these events occur.
- 1_CH_SD returns a 1 if one or more channels have faulted out.
- 2_CH_SD returns a 1 if two or more channels have faulted out.
- A fault will not be reported in the event that theBL is commanded on and then immediately off by the system.
- When FAULT is set to 1, it will remain at 1 even if the signal which sets it goes away. FAULT will be cleared when the BL_CTL bit of the Device Control Register is toggled or when written low. At that time, if the fault condition is still present or reoccurs, FAULT will be set to 1 again. BL_STAT will not cause FAULT to be set.
- The controller will not indicate a fault if the VBL+ goes away, whether or not the LEDs were on at the time of the power loss. This can occur if there is some hang condition that causes the user to force the system off by holding the power button down for 4s.
- The default value for Register 0x02 is 0x00.

Identification Register (0x03)

The ID register contains 3-bit fields to denote the LED driver (always set to 1), manufacturer and the silicon revision of the controller IC. The bit field widths allow up to 16 vendors with up to 8 silicon revisions each. In order to keep the number of silicon revisions low, the revision field will not be updated unless the part will make it out to the user’s factory. Thus, if during the engineering development process, 3 silicon spins were needed, the next available revision ID would be used for all 3 spins until that same ID made it to the factory. Except Bit 7, which has to be 1, all of the bits in this register are read-only.

- Vendor ID 9 represents Intersil Corporation.
- The default value for Register 0x03 is 0xC8.

The initial value of REV shall be 0. Subsequent values of REV will increment by 1.

Components Selections

According to the inductor Voltage-Second Balance principle, the change of inductor current during the switching regulator On-time is equal to the change of inductor current during the switching regulator Off-time.

Since the voltage across an inductor is as shown in Equation 7:

$$V_L = L \times \Delta I_L / \Delta t \quad \text{(EQ. 7)}$$

and ΔI_L @ On = ΔI_L @ Off, therefore:

$$(V_I - 0)/L \times D \times t_S = (V_O - V_D - V_I)/L \times (1 - D) \times t_S \quad \text{(EQ. 8)}$$

where D is the switching duty cycle defined by the turn-on time over the switching periods. V_D is Schottky diode forward voltage that can be neglected for approximation.

Rearranging the terms without accounting for V_D gives the boost ratio and duty cycle respectively as Equations 9 and 10:

$$V_O/V_I = 1/(1 - D) \quad \text{(EQ. 9)}$$

$$D = (V_O - V_I)/V_O \quad \text{(EQ. 10)}$$

Input Capacitor

Switching regulators require input capacitors to deliver peak charging current and to reduce the impedance of the input supply. This reduces interaction between the regulator and input supply, thereby improving system stability. The high switching frequency of the loop causes almost all ripple current to flow in the input capacitor, which must be rated accordingly.

A capacitor with low internal series resistance should be chosen to minimize heating effects and improve system efficiency, such as X5R or X7R ceramic capacitors, which offer small size and a lower value of temperature and voltage coefficient compared to other ceramic capacitors.

It is recommended that an input capacitor of at least 10µF be used. Ensure the voltage rating of the input capacitor is suitable to handle the full supply range.

Inductor

The selection of the inductor should be based on its maximum and saturation current (I_{SAT}) characteristics, power dissipation (DCR), EMI susceptibility (shielded vs unshielded), and size. Inductor type and value influence many key parameters, including ripple current, current limit, efficiency, transient performance and stability.

The inductor's maximum current capability must be adequate enough to handle the peak current at the worst case condition. Additionally if an inductor core is chosen with too low a current rating, saturation in the core will cause the effective inductor value to fall, leading to an increase in peak to average current level, poor efficiency and overheating in the core. The series resistance, DCR, within the inductor causes conduction loss and heat dissipation. A shielded inductor is usually more suitable for EMI susceptible applications, such as LED backlighting.

The peak current can be derived from the voltage across the inductor during the Off-period, as expressed in Equation 11:

$$IL_{peak} = (V_O \times I_O)/(85\% \times V_I) + 1/2[V_I \times (V_O - V_I)/(L \times V_O \times f_{SW}) \quad \text{(EQ. 11)}$$

The choice of 85% is just an average term for the efficiency approximation. The first term is the average current, which is inversely proportional to the input voltage. The second term is the inductor current change, which is inversely proportional to L and f_{SW}. As a result, for a given switching.

REGISTER 0x00	PWM BRIGHTNESS CONTROL REGISTER

BRT7	BRT6	BRT5	BRT4	BRT3	BRT2	BRT1	BRT0
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
BRT[7..0]	= 256 steps of PWM brightness levels

FIGURE 30. DESCRIPTIONS OF BRIGHTNESS CONTROL REGISTER

REGISTER 0x01	DEVICE CONTROL REGISTER

RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	PWM_MD	PWM_SEL	BL_CTL
Bit 7 (R/W)	Bit 6 (R/W)	Bit 5 (R/W)	Bit 4 (R/W)	Bit 3 (R/W)	Bit 2 (R/W)	Bit 1 (R/W)	Bit 0 (R/W)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
PWM_MD	= PWM mode select bit (1 = absolute brightness, 0 = % change) default = 0
PWM_SEL	= Brightness control select bit (1 = control by PWMI, 0 = control by SMBus) default = 0
BL_CTL	= BL On/Off (1 = On, 0 = Off) default = 0

FIGURE 31. DESCRIPTIONS OF DEVICE CONTROL REGISTER

REGISTER 0x02	FAULT/ STATUS REGISTER

RESERVED	RESERVED	2_CH_SD	1_CH_SD	BL_STAT	OV_CURR	THRM_SHDN	FAULT
Bit 7 (R)	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT	BIT ASSIGNMENT	BIT FIELD DEFINITIONS
Bit 5	2_CH_SD	= Two LED output channels are shutdown (1 = shutdown, 0 = OK)
Bit 4	1_CH_SD	= One LED output channel is shutdown (1 = shutdown, 0 = OK)
Bit 3	BL_STAT	= BL Status (1 = BL On, 0 = BL Off)
Bit 2	OV_CURR	= Input Overcurrent (1 = Overcurrent condition, 0 = Current OK)
Bit 1	THRM_SHDN	= Thermal Shutdown (1 = Thermal Fault, 0 = Thermal OK)
Bit 0	FAULT	= Fault occurred (Logic “OR” of all of the fault conditions)

FIGURE 32. DESCRIPTIONS OF FAULT/ STATUS REGISTER

REGISTER 0x03	ID REGISTER

LED PANEL	MFG3	MFG2	MFG1	MFG0	REV2	REV1	REV0
Bit 7 = 1	Bit 6 (R)	Bit 5 (R)	Bit 4 (R)	Bit 3 (R)	Bit 2 (R)	Bit 1 (R)	Bit 0 (R)

BIT ASSIGNMENT	BIT FIELD DEFINITIONS
MFG[3..0]	= Manufacturer ID. See “Identification Register (0x03)” on page 19. Data 0 to 8 in decimal correspond to other vendors data 9 in decimal represents Intersil ID data 10 to 14 in decimal are reserved data 15 in decimal Manufacturer ID is not implemented
REV[2..0]	= Silicon rev (Rev 0 through Rev 7 allowed for silicon spins)

FIGURE 33. DESCRIPTIONS OF ID REGISTER

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
11/13/09	FN6996.1	Changed in OVP and VOUT Requirement Changed from: VOUT can only regulate between 61% and 100% of the VOUT_OVP such that: To: VOUT can only regulate between 64% and 100% of the VOUT_OVP such that From: Allowable VOUT = 61% to 100% of VOUT_OVP To: Allowable VOUT = 64% to 100% of VOUT_OVP From: ...then the VOUT is allowed to operate between 24.4V and 40V. To: ...then the VOUT is allowed to operate between 25.6V and 40V. From: ...should follow VOUT = (61% ~100%)OVP requirement To: ...should follow VOUT = (64% ~100%)OVP requirement. Changed VSC spec from “2.5Vmin, 3.4Vmax, 3.3min, 4.4max, 4.2min, 5.4max to “2.4Vmin, 3.6Vmax, 3.3min, 4.6max, 4.2min, 5.6max”.
10/21/09	FN6996.0	Initial Release.

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

* For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL97677

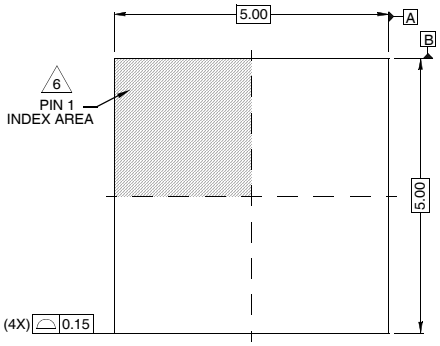
To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

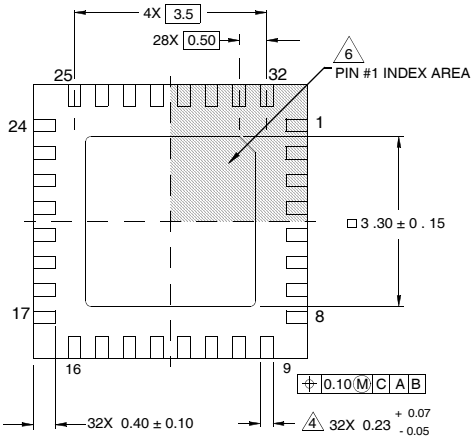
Package Outline Drawing

L32.5x5B

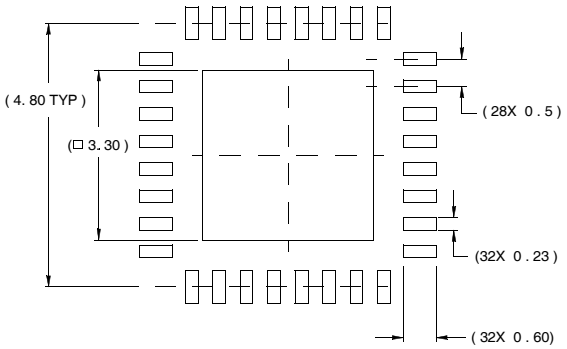
32 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 2, 11/07



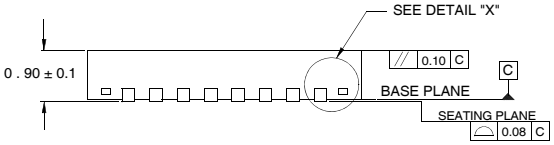
TOP VIEW



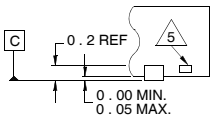
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.