Synchronous Step-Down MOSFET Drivers

ZL1505

The ZL1505 is an integrated high-speed, high-current N-channel MOSFET driver for synchronous step-down DC/DC conversion applications. When used with Zilker Labs Digital-DC™ PWM controllers, the ZL1505 enables dynamically adaptive dead-time control that optimizes efficiency under all operating conditions. A dual input PWM configuration enables this efficiency optimization while minimizing complexity within the driver.

Operating from a 4.5V to 7.5V input, the ZL1505 combines a 5A, 0.5W low-side driver and a 3A, 0.8W high-side driver to support high step-down buck applications. A unique adjustable gate drive current scheme allows the user to adjust the drive current on both drivers to optimize performance for a wide rage of input/output voltages, load currents, power MOSFETs and switching frequencies up to 1.4MHz. An integrated 30V bootstrap Schottky diode is used to charge the external bootstrap capacitor. An internal watchdog circuit prevents excessive shoot-through currents and protects the external MOSFET switches.

The ZL1505 is specified over a wide -40°C to +125°C junction temperature range and is available in an exposed pad DFN-10 package.

Features

- High-speed, high-current drivers for synchronous N-channel MOSFETs
- Adaptive dead-time control optimizes efficiency when used with Digital-DC controllers
- Integrated 30V bootstrap Schottky diode
- Capable of driving 40A per phase
- Supports switching frequency up to 1.4MHz
  - >4A source, >5A sink low-side driver
  - >3A source/sink high-side driver
  - <10ns rise/fall times, low propagation delay
- Adjustable gate drive strength optimizes efficiency for different V_{IN}, V_{OUT}, I_{OUT}, F_{SW} and MOSFET combinations
- Internal non-overlap watchdog prevents shoot-through currents

Applications*(see page 12)

- High efficiency, high-current DC/DC buck converters with digital control and PMBus™
- Multi-phase digital DC/DC converters with phase adding/dropping
- Power train modules
- Synchronous rectification for secondary side isolated power converters

Related Literature*(see page 12)

- ZL2004 Adaptive Digital DC/DC Controller with Current Sharing

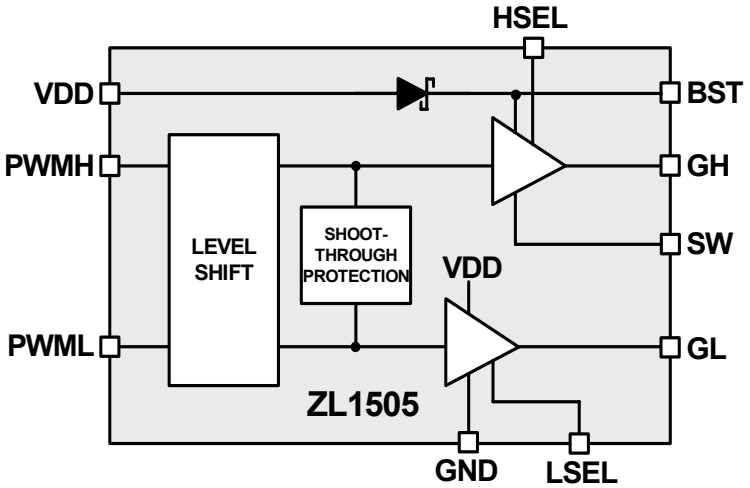

FIGURE 1. ZL1505 BLOCK DIAGRAM

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Typical Application Circuit

The following application circuit represents the typical implementation of the ZL1505 (Notes 1, 2).

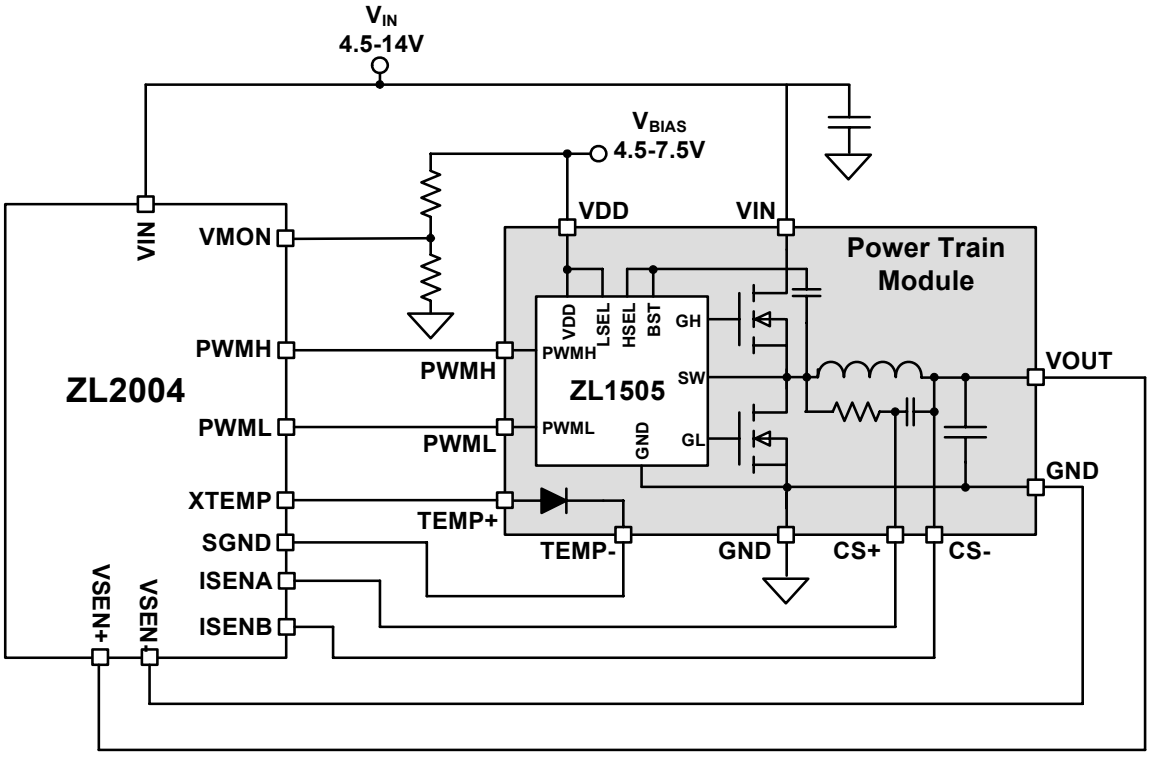


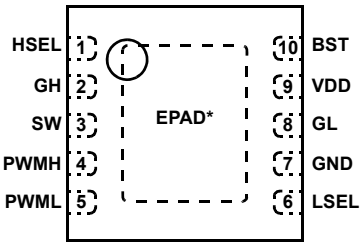
FIGURE 2. POWER TRAIN MODULE USING ZL2004 PWM CONTROLLER

NOTES:

1. For V_{DD} of 4.5V to 7.5V, the maximum V_{IN} of the ZL1505 is 22.5V to 25.5V. ZL1505 input supply voltage range (V_{IN}) is specified in Figure 2.
2. V_{IN} for this application circuit is limited by the ZL2004 V_{IN} of 4.5V to 14V.

Pin Configuration

ZL1505
(10 LD DFN)
TOP VIEW



*CONNECT TO GND

Pin Descriptions

PIN NUMBER	PIN NAME	TYPE (Note 3)	DESCRIPTION
1	HSEL	I	High-side gate drive current selector. Connect to BST for maximum gate drive current; connect to SW for 50% of maximum gate drive current.
2	GH	O	Output of high-side gate driver. Connect to the gate of high-side FET.
3	SW	I/O	Phase node. Return path for high-side driver. Connect to source of high-side FET and drain of low-side FET.
4	PWMH	I	High-side PWM control input.
5	PWML	I	Low-side PWM control input.
6	LSEL	I	Low-side gate drive current selector. Connect to VDD for maximum gate drive current; connect to GND for 50% of maximum gate drive current.
7	GND	PWR	Ground. All signals return to this pin.
8	GL	O	Output of low-side gate driver. Connect to the gate of low-side FET.
9	VDD	PWR	Gate drive bias supply. Connect a high-quality bypass capacitor from this pin to GND.
10	BST	PWR	Bootstrap supply. Connect external capacitor to SW node.
EPAD	GND	PWR	Ground.

NOTE:

3. I = Input, O = Output, PWR = Power OR Ground.

Ordering Information

PART NUMBER (Notes 4, 7)	PART MARKING	TEMP RANGE (°C)	PACKAGE Tape and Reel (Pb-free)	PKG. DWG. #
ZL1505ALNNT (Note 5)	1505	-40 to +125	10 Ld 3x3 DFN	L10.3x3D
ZL1505ALNNT1 (Note 5)	1505	-40 to +125	10 Ld 3x3 DFN	L10.3x3D
ZL1505ALNNT6 (Note 5)	1505	-40 to +125	10 Ld 3x3 DFN	L10.3x3D
ZL1505ALNFT (Note 6)	1505	-40 to +125	10 Ld 3x3 DFN	L10.3x3D
ZL1505ALNFT1 (Note 6)	1505	-40 to +125	10 Ld 3x3 DFN	L10.3x3D
ZL1505ALNFT6 (Note 6)	1505	-40 to +125	10 Ld 3x3 DFN	L10.3x3D

NOTES:

4. Please refer to Tech Brief TB347 for details on reel specifications.
5. These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
6. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
7. For Moisture Sensitivity Level (MSL), please see device information page for ZL1505. For more information on MSL please see Tech Brief TB363.

Absolute Maximum Ratings

Voltage Measured with Respect to GND
DC Supply Voltage for VDD Pin . . . . . -0.3V to 8V
High-Side Supply Voltage for BST Pin. . . . . -0.3V to 30V
High-Side Drive Voltage for
GH Pin . . . . . (V_{SW} - 0.3V) to (V_{BST} + 0.3V)
Low-Side Drive Voltage for
GL Pin. . . . . (GND - 0.3V) to (V_{DD} + 0.3V)
Boost to Switch Differential (V_{BST} - V_{SW}) for
BST, SW Pins. . . . . -0.3V to 8V
Switch Voltage for SW Pin
Continuous . . . . . (GND - 0.3V) to 30V
<100ns . . . . . (GND - 5V) to 30V
Logic I/O Voltage for PWMH, PWML, LSEL Pins. . . . . -0.3V to 6V
HSEL Pin . . . . . (V_{SW} - 0.3V) to (V_{BST} + 0.3V)
ESD Rating
Human Body Model 2kV
GL Pin. 1.5kV
Machine Model 500V
Latch Up. . . . . Tested to JESD78

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld DFN (Notes 8, 9)	50	7

Junction Temperature Range . . . . . -55°C to +150°C
Storage Temperature Range. . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Gate Drive Bias Supply Voltage Range
VDD . . . . . 4.5V to 7.5V
Input Supply Voltage Range, V_{IN} . . . . . 3V to 30V - V_{DD}
Operating Junction Temperature Range, T_J . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

8. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
9. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

V_{DD} = 6.5V, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C.**

PARAMETER	CONDITIONS		MIN (Note 10)	TYP	MAX (Note 10)	UNIT
BIAS CURRENT CHARACTERISTICS						
I_{DD} supply current	Not switching		–	110	180	µA
PWM INPUT CHARACTERISTICS						
PWM Input Bias Current	V_{PWM} = 5 V		–	5	–	µA
	V_{PWM} = 0 V		–	–	1	µA
PWM Input Logic Low, V_{IL}	PWMH or PWML	V_{DD} = 6.5V	–	–	**1.7**	V
		V_{DD} = 5.0V	–	–	**1.4**	V
PWM Input Logic High, V_{IH}	PWMH or PWML	V_{DD} = 6.5V	**3.4**	–	–	V
		V_{DD} = 5.0V	**2.7**	–	–	V
Hysteresis	PWMH or PWML	V_{DD} = 6.5V	-	1.1	-	V
		V_{DD} = 5.0V	-	0.8	-	V
Minimum PWMH On-time to Produce GH Pulse, $t_{PWMH,ON}$ (Note 11)	C_{GH} = 0		–	12	-	ns
Minimum GH On-time Pulse, $t_{GH,ON}$ (Note 12)	C_{GH} = 0		–	14	-	ns
	C_{GH} = 3 nF, V_{HSEL} = V_{BST}		-	20	-	ns
Minimum PWMH Off-time to Produce Valid GH Pulse, $t_{PWMH,OFF}$	C_{GH} = 0		–	17	-	ns
BOOTSTRAP DIODE CHARACTERISTICS						
Forward Voltage (V_F)	Forward bias current 100 mA		–	0.8	–	V

Electrical Specifications V_{DD} = 6.5V, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	CONDITIONS		MIN (Note 10)	TYP	MAX (Note 10)	UNIT
THERMAL PROTECTION						
Thermal Trip Point			–	150	–	°C
Thermal Reset Point			–	134	–	°C
UPPER GATE DRIVER CHARACTERISTICS						
Driver Voltage (V_{BST} – V_{SW})			–	6	–	V
High-side Driver Peak Gate Drive Current (Pull-up)	(V_{GH} – V_{SW}) = 2.5V	HSEL connected to BST	**2.0**	3.2	–	A
		HSEL connected to SW	**1.0**	1.7	-	A
High-side Driver Peak Gate Drive Current (Pull-down)	(V_{GH} – V_{SW}) = 2.5V	HSEL connected to BST	**2.0**	3.2	–	A
		HSEL connected to SW	**1.0**	1.6	-	A
High-side Driver Pull-up Resistance	(V_{BST} – V_{GH}) = 50mV	HSEL connected to BST	–	0.7	**0.9**	Ω
		HSEL connected to SW	-	0.9	**1.2**	Ω
High-side Driver Pull-down Resistance	(V_{GH} – V_{SW}) = 50mV	HSEL connected to BST	–	0.8	**1.1**	Ω
		HSEL connected to SW	–	1.1	**1.5**	Ω
LOWER GATE DRIVER CHARACTERISTICS						
Driver voltage (V_{DD})			-	6.5	-	V
Low-side Driver Peak Gate Drive Current (Pull-up)	(V_{GL} - V_{GNG}) = 2.5V	LSEL connected to VDD	**3.0**	4.5	–	A
		LSEL connected to GND	**1.5**	2.4	-	A
Low-side Driver Peak Gate Drive Current (Pull-down)	(V_{GL} – V_{GND}) = 2.5V	LSEL connected to VDD	**3.5**	5.4	–	A
		LSEL connected to GND	**1.8**	2.8	-	A
Low-side Driver Pull-up Resistance	(V_{DD} - V_{GL}) = 50mV	LSEL connected to VDD	–	0.7	**0.9**	Ω
		LSEL connected to GND	-	1.0	**1.3**	Ω
Low-side Driver Pull-down Resistance	(V_{GL} – GND) = 50mV	LSEL connected to VDD	–	0.5	**0.7**	Ω
		LSEL connected to GND	-	0.7	**1.0**	Ω
SWITCHING CHARACTERISTICS						
GH rise time, t_{RH}	C_{GH} = 3nF	HSEL connected to BST	–	5.3	**8.5**	ns
		HSEL connected to SW	-	10.5	**16.5**	ns

Electrical Specifications V_{DD} = 6.5V, T_J = -40°C to +125°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +125°C. (Continued)**

PARAMETER	CONDITIONS		MIN (Note 10)	TYP	MAX (Note 10)	UNIT
GH fall time, t_{FH}	C_{GH} = 3nF	HSEL connected to BST	-	4.8	**7.5**	ns
		HSEL connected to SW	-	9.5	**15**	ns
GL rise time, t_{RL}	C_{GL} = 3nF	LSEL connected to VDD	–	4.0	**6.0**	ns
		LSEL connected to GND	-	7.8	**12**	ns
GL fall time, t_{FL}	C_{GL} = 3nF	LSEL connected to VDD	-	3.0	**4.5**	ns
		LSEL connected to GND	-	5.5	**8.5**	ns
GH turn-on propagation delay, t_{DHR}	HSEL connected to BST		–	30.0	–	ns
	HSEL connected to SW		-	31.5	-	ns
GH turn-off propagation delay, t_{DHF}	HSEL connected to BST		–	37.5	–	ns
	HSEL connected to SW		-	39.0	-	ns
GL turn-on propagation delay, t_{DLR}	LSEL connected to V_{DD}		–	26.5	–	ns
	LSEL connected to GND		-	28.0	-	ns
GL turn-off propagation delay, t_{DLF}	LSEL connected to V_{DD}		–	30.0	–	ns
	LSEL connected to GND		-	31.5	-	ns

NOTES:

10. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
11. The minimum PWMH on-time pulse ($t_{PWMH,ON}$) is specified from VPWM = 2.5V on the rise edge to VPWM = 2.5V on the falling edge.
12. The minimum GH on-time pulse ($t_{GH,ON}$) is specified at V_{GH} = 2.5V.

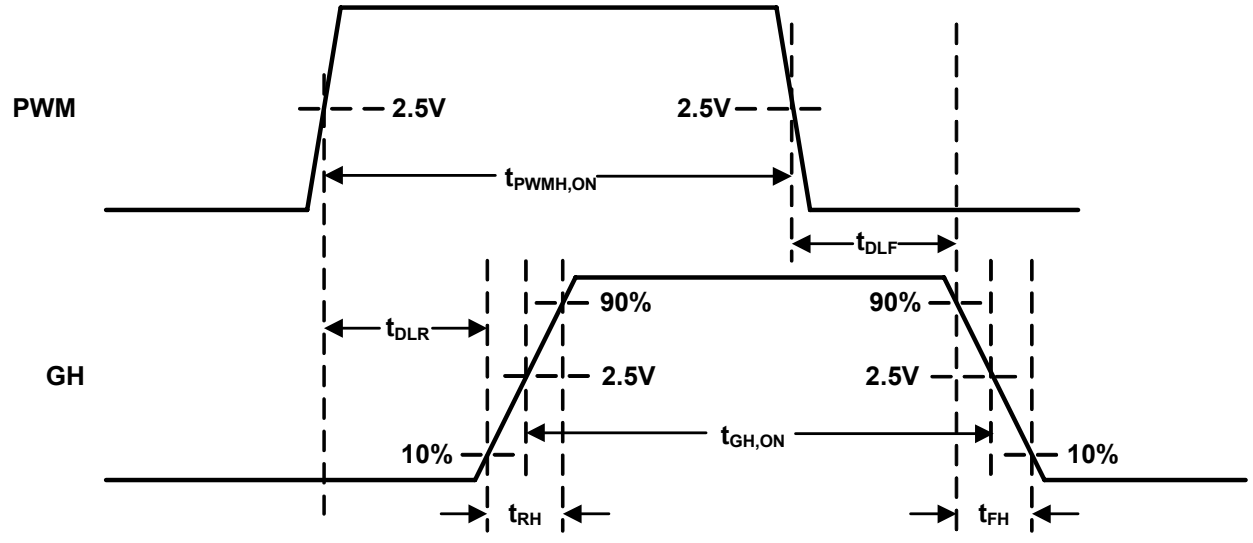


FIGURE 3. TIMING DIAGRAM

Typical Performance Curves

Performance curves with temperature are measured at ambient temperatures (T_A) of +85°C, +25°C, and -25°C.

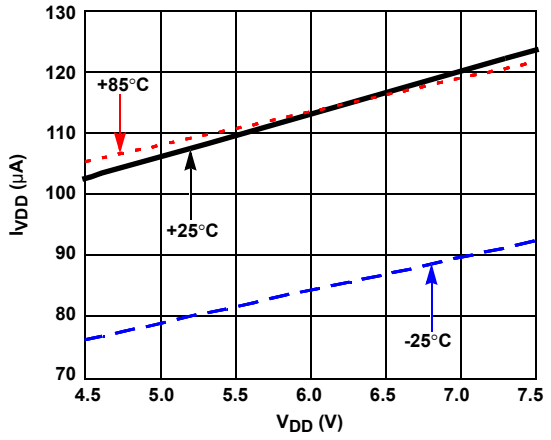


FIGURE 4. I_{VDD} vs V_{DD} WITH TEMPERATURE (NO SWITCHING)

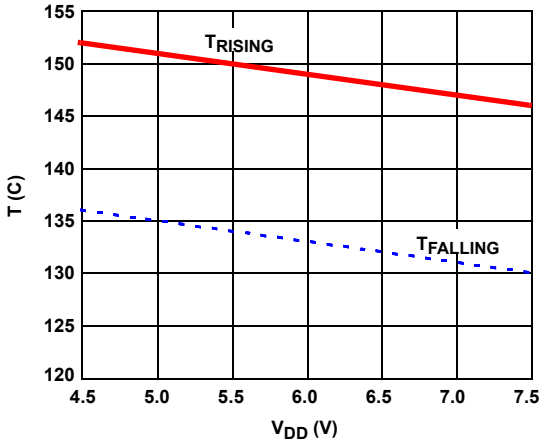


FIGURE 5. THERMAL PROTECTION THRESHOLDS

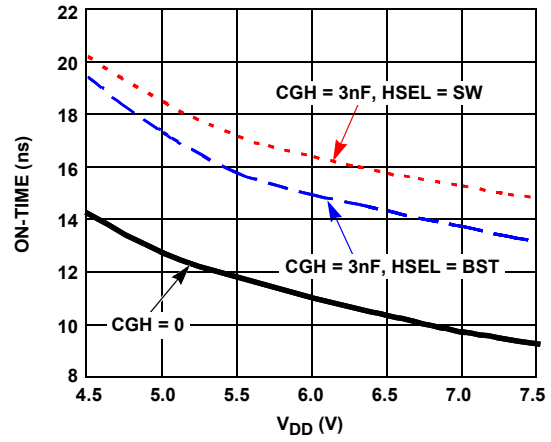


FIGURE 6. MINIMUM GH ON-TIME, $t_{GH,ON}$ (T_A = +25°C)

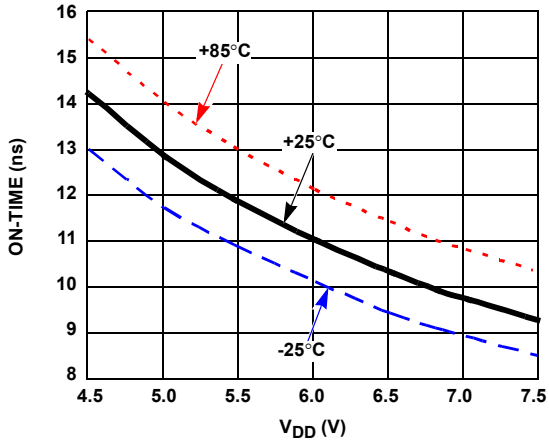


FIGURE 7. $t_{GH,ON}$ WITH TEMPERATURE (CGH = 0) (see Figure 3 for $t_{GH,ON}$ timing)

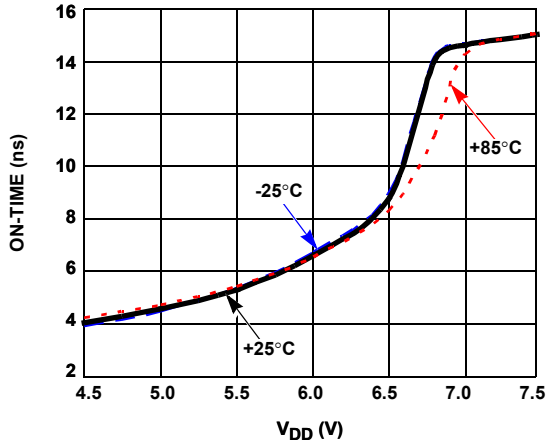


FIGURE 8. MINIMUM PWMH ON-TIME, $t_{PWMH,ON}$ (CGH = 0)

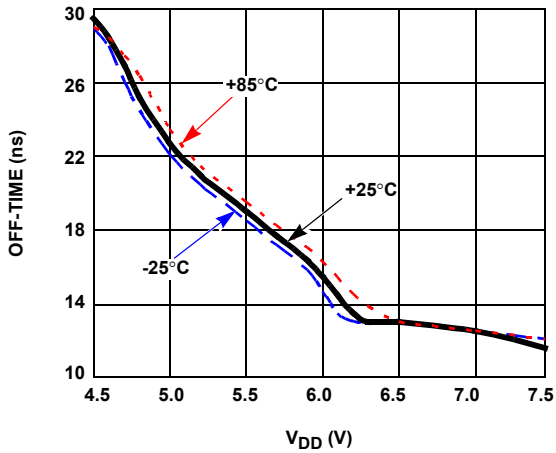


FIGURE 9. MINIMUM PWMH OFF-TIME, $t_{PWMH,OFF}$ (CGH = 0)

Typical Performance Curves

Performance curves with temperature are measured at ambient temperatures (T_A) of +85°C, +25°C, and -25°C. **(Continued)**

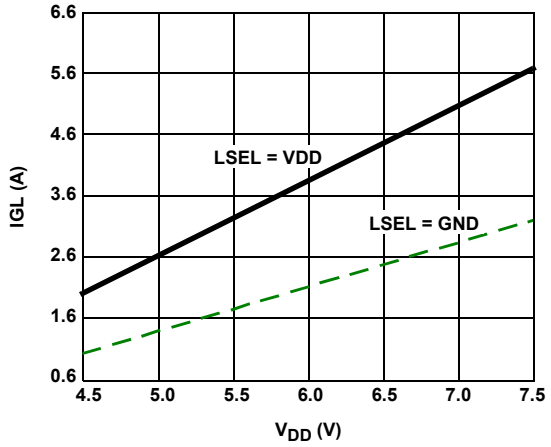


FIGURE 10. LOW-SIDE DRIVER PULL-UP CURRENT (V_{GL} = 2.5V, T_A = +25°C)

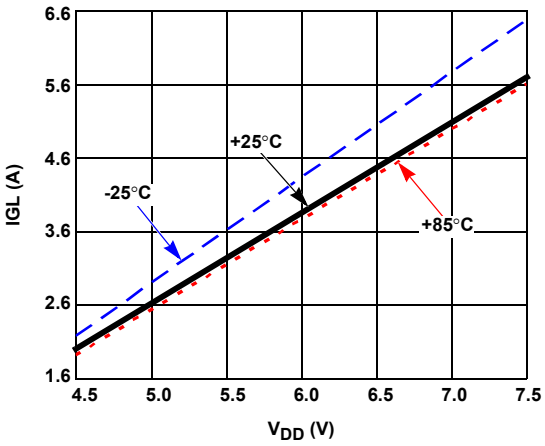


FIGURE 11. LS PULL-UP CURRENT WITH TEMPERATURE (V_{GL} = 2.5V, LSEL = VDD)

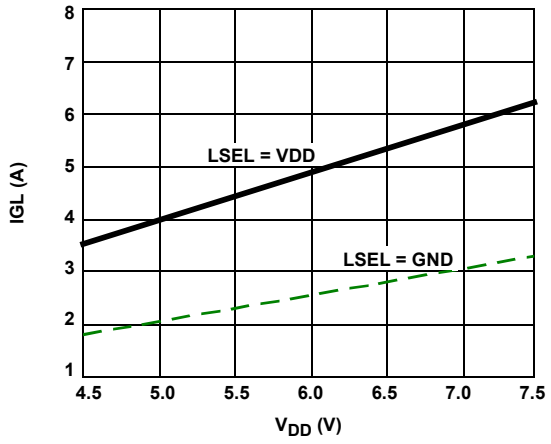


FIGURE 12. LOW-SIDE DRIVER PULL-DOWN CURRENT (V_{GL} = 2.5V, T_A = +25°C)

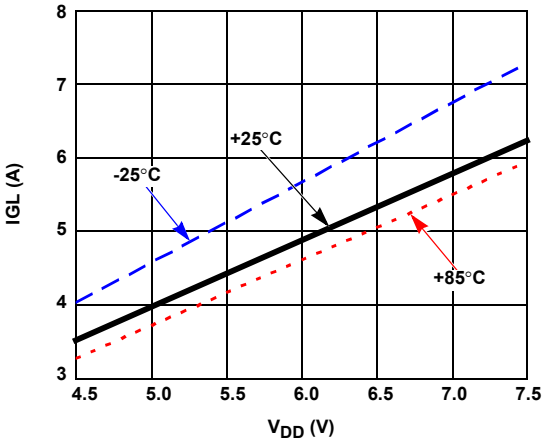


FIGURE 13. LS PULL-DOWN CURRENT WITH TEMPERATURE (V_{GL} = 2.5V, LSEL = VDD)

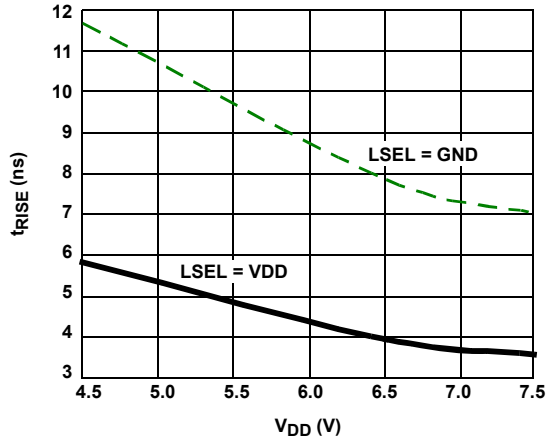


FIGURE 14. LOW-SIDE DRIVER RISE TIME, t_{RL} (CGL = 3nF, T_A = +25°C)

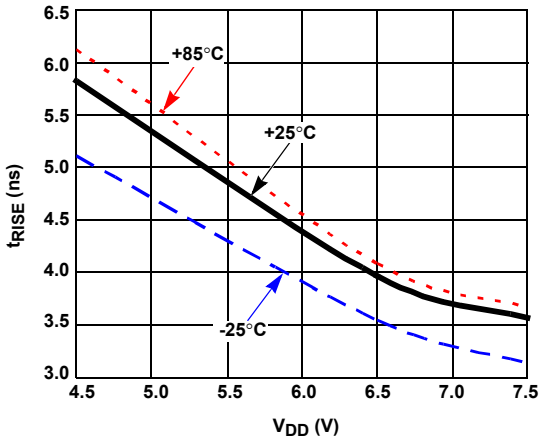


FIGURE 15. t_{RL} WITH TEMPERATURE (C_{GL} = 3nF, LSEL = VDD)

Typical Performance Curves

Performance curves with temperature are measured at ambient temperatures (T_A) of +85°C, +25°C, and -25°C. **(Continued)**

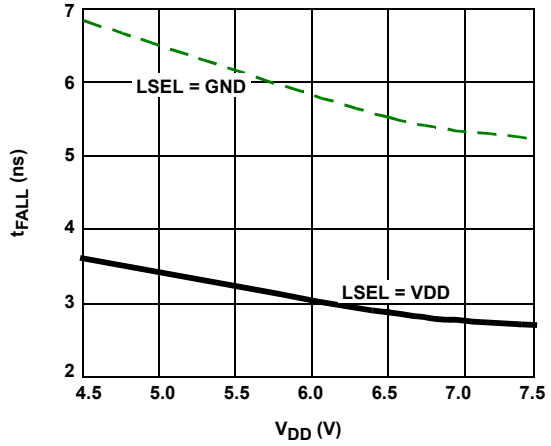


FIGURE 16. LOW-SIDE DRIVER FALL TIME, t_{FL} (CGL = 3nF, T_A = +25°C)

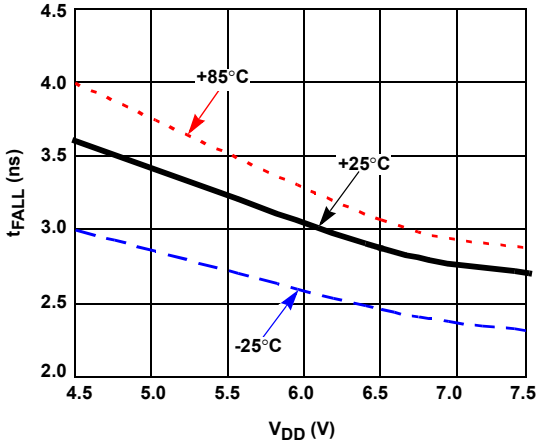


FIGURE 17. t_{FL} WITH TEMPERATURE (C_{GL} = 3nF, LSEL = VDD)

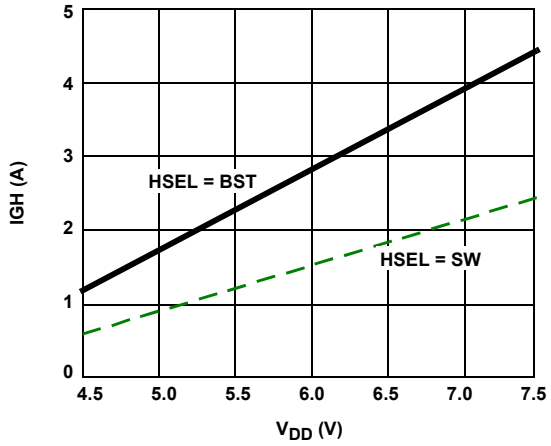


FIGURE 18. HIGH-SIDE DRIVER PULL-UP CURRENT (V_{GH} - V_{SW} = 2.5V, T_A = +25°C)

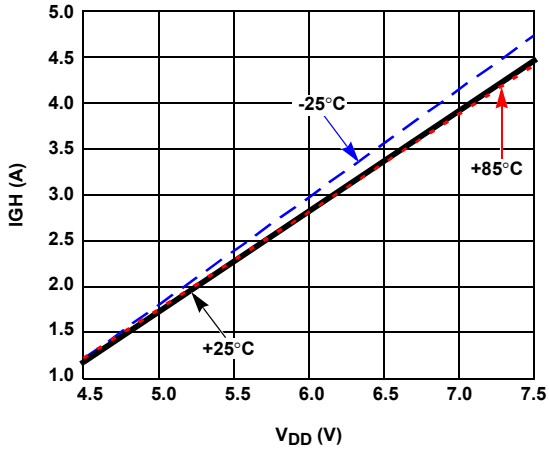


FIGURE 19. HS PULL-UP CURRENT WITH TEMPERATURE (V_{GH} - V_{SW} = 2.5V, HSEL = BST)

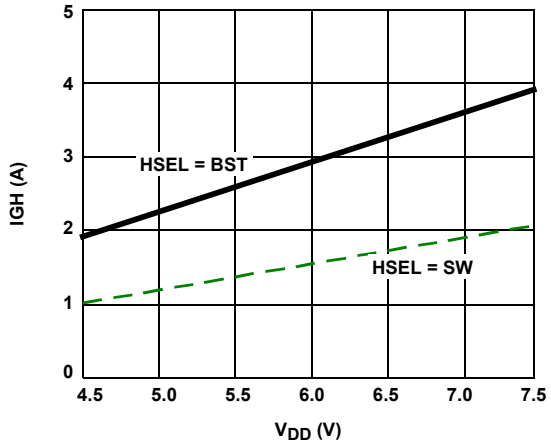


FIGURE 20. HIGH-SIDE DRIVER PULL-DOWN CURRENT (V_{GH} - V_{SW} = 2.5V, T_A = +25°C)

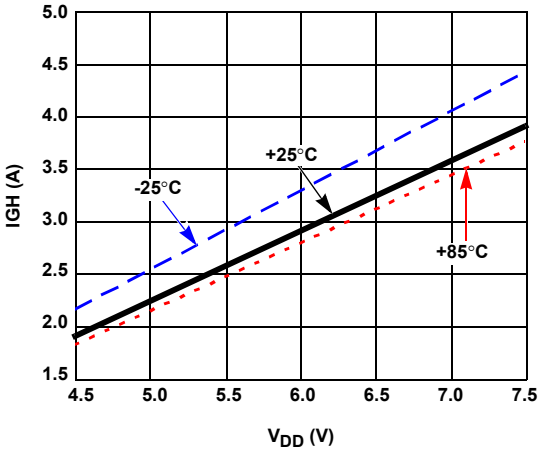


FIGURE 21. HS PULL-DOWN CURRENT WITH TEMPERATURE (V_{GH} - V_{SW} = 2.5V, HSEL = BST)

Typical Performance Curves

Performance curves with temperature are measured at ambient temperatures (T_A) of +85°C, +25°C, and -25°C. **(Continued)**

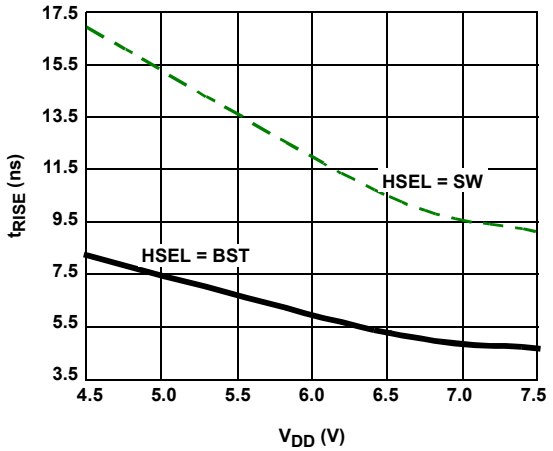


FIGURE 22. HIGH-SIDE DRIVER RISE TIME, t_{RH} (CGH = 3nF, T_A = +25°C)

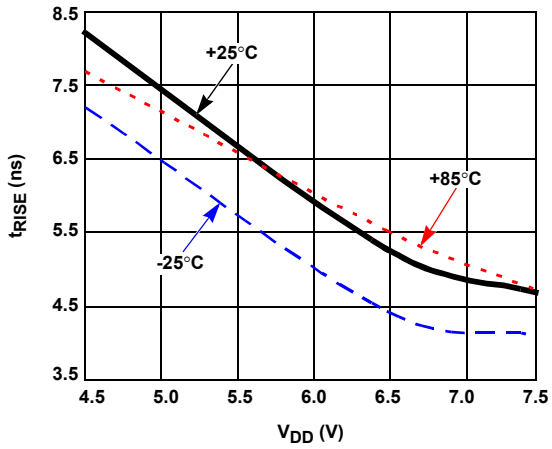


FIGURE 23. t_{RH} WITH TEMPERATURE (C_{GH} = 3nF, HSEL = BST)

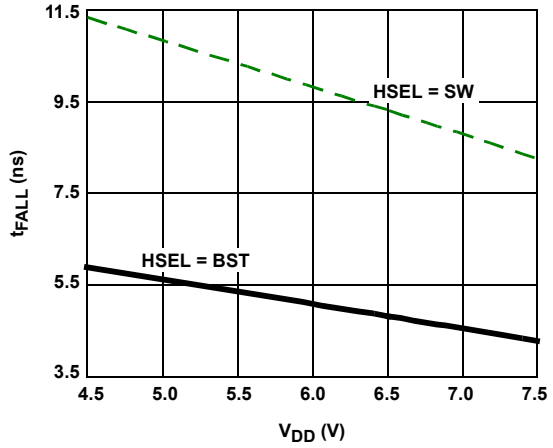


FIGURE 24. HIGH-SIDE DRIVER FALL TIME, t_{FH} (CGH = 3nF, T_A = +25°C)

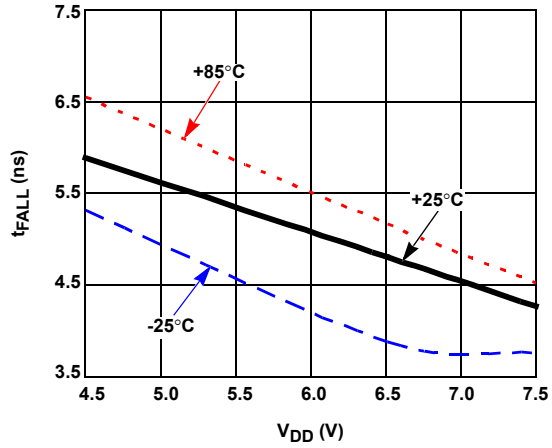


FIGURE 25. t_{FH} WITH TEMPERATURE (C_{GH} = 3nF, HSEL = BST)

ZL1505 Overview

Theory of Operation

The ZL1505 is a synchronous N-channel MOSFET driver that is intended for use with Zilker Labs Digital-DC PWM controllers to enable a high-efficiency DC/DC conversion scheme. The patented Digital-DC control scheme utilizes a closed-loop algorithm to optimize the dead-time applied between the gate drive signals for the high-side and low-side MOSFETs. By monitoring the duty cycle of the resulting DC/DC converter circuit, this dynamic routine continuously varies the MOSFET dead times to optimize conversion efficiency in response to varying circuit conditions. The ZL1505's dual PWM input configuration enables this optimization scheme to be applied while minimizing the complexity within the driver device. Please refer to the ZL2004 data sheet for details on the dynamic dead-time optimization routine.

The ZL1505 integrates two powerful gate drivers that have been optimized for step-down DC/DC conversion circuit configurations whose output current can exceed 40A per phase. The ZL1505 also integrates a 30V bootstrap Schottky diode to minimize the external components and provide a high drive voltage to the high-side driver device.

Variable Gate Drive Current

The ZL1505 incorporates an innovative variable drive current scheme that enables the user to optimize the gate drive current levels to the requirements of the external MOSFETs used over a wide range of operating frequencies. Each of the gate drivers incorporates a logic input (HSEL and LSEL) that allows the user to select the gate drive strength to 50% or 100% of the total rated drive current.

With the HSEL pin connected to the BST pin, the high-side driver can deliver the full rated gate drive current; with the HSEL pin connected to the SW pin, the output current will be limited to 50% of the full rated output capability. With the LSEL pin connected to VDD, the low-side driver can deliver the full rated gate drive current; with the LSEL pin connected to GND, the

output current will be limited to 50% of the full rated output capability. Using HSEL and LSEL, the ZL1505 can be used across a wide range of applications using only a simple PCB layout change.

Also, the VDD pin is the gate drive bias supply for the external MOSFETs. VDD can be used to vary the gate drive strength as shown for the low-side driver in Figures 9 through 12 and for the high-side driver in Figures 17 through 20.

Overlap Protection Circuit

The ZL1505 includes an internal watchdog circuit that prevents excessive shoot-through current from occurring in the unlikely event that the PWM converter places both switches in the ON position. If the overlap time between the PWMH and PWML pulses exceeds 30ns, the PWMH signal will be forced to the LOW state until the overlap condition ceases, allowing normal switching operation to continue.

Start-up Requirements

During power-up, the ZL1505 maintains both GH and GL outputs in the LOW state while the V_{IN} voltage is ramping up. Once the V_{DD} supply is within specification, the GH and GL pins may be operated using the PWMH and PWML logic inputs respectively.

In the case where the PWM controller is powered from a supply other than the ZL1505's V_{DD} supply, and the PWM controller is powered up first, the PWM controller gate outputs should be kept in low or in high-impedance state until the V_{DD} supply is within specification. Additionally, if the ZL1505 begins its power-down sequence prior to the PWM controller then the PWM controller gate outputs should be set in low or in high-impedance state before the V_{DD} voltage supply drops below its specified range.

Thermal Protection

When the junction temperature exceeds +150°C the high-side driver output GH is forced to logic low state. The driver output is allowed to switch logic states again once the junction temperature drops below +134°C.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
2/15/11	FN6845.3	Added ZL1505ALNFT, ZL1505ALNFT1 and ZL1505ALNFT6 to “Ordering Information” on page 3. Added applicable lead finish note (note 6).
2/9/11		Pg. 4: under “Absolute Maximum Ratings,” changed maximum voltage from 8V to 6V for the following pins: From: “Logic I/O Voltage for PWMH, PWML, LSEL Pins . . . -0.3V to 8V” To: “Logic I/O Voltage for PWMH, PWML, LSEL Pins . . . -0.3V to 6V”
10/19/10	FN6845.2	“PWM Input Logic Low, VIL” on page 4, changed Max spec from 2.2V to 1.7V for “VDD = 6.5V”. Removed Min/Typ specs of 1.7/2 “PWM Input Logic Low, VIL” on page 4, changed Max spec from 1.9V to 1.4V for “VDD = 5.0V”. Removed Min/Typ specs of 1.5/1.7 “PWM Input Logic High, VIH” on page 4, changed Min spec from 2.8V to 3.4V for “VDD = 6.5V”. Removed Typ/Max specs of 3.1/3.4 “PWM Input Logic High, VIH” on page 4, changed Min spec from 2.2V to 2.7V for “VDD = 5.0V”. Removed Typ/Max specs of 2.5/2.7
7/9/10		On page 4, Electrical Specifications Table, the parameter “Minimum GH On-time Pulse, tGH,ON (Note 12)”, removed 14 and 20 from Max column. In TYP column, changed 10 to 14 and 14 to 20. On page 4, Electrical Specifications Table, the parameter “Minimum PWMH On-time to Produce GH Pulse, tPWMH,ON (Note 11)”, removed 12 from Max column. In TYP column, changed 8.5 to 12. On page 4, Electrical Specifications Table, the parameter “Minimum PWMH Off-time to Produce Valid GH Pulse, tPWMH,OFF”, removed 17 from Max column. In TYP column, changed 13 to 17. Replaced POD drawing with updated revisions and changes were as follows: Converted to new standards by adding land pattern and moving dimensions from table onto drawing
2/14/09	FN6845.1	Assigned file number FN6845 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to datasheet content
12/4/09	FN6845.0	Converted to new Intersil template. Changed in Abs Max Ratings “Low-Side Drive Voltage for GL pin” from “(GND - 0.3) to (VIN + 0.3)” to “(GND - 0.3) to (VDD + 0.3)”. Removed Bullet "Adjustable gate drive voltage: 4.5V to 7.5V" and "Exposed pad 3mmx3mm DFN-10 Package" from Features. Intersil Standards applied are: Added Related Information, Updated ordering information with Notes that includes MSL. Updated Abs Max Ratings with notes, added ESD Ratings and Latchup, added Boldface text in Electrical Spec Table. Added POD

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*For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ZL1505

To report errors or suggestions for this datasheet, please go to www.intersil.com/askourstaff

FITs are available from our website at http://rel.intersil.com/reports/search.php

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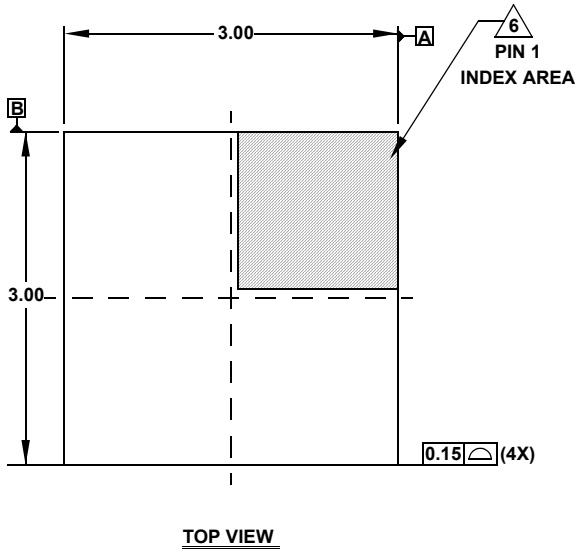
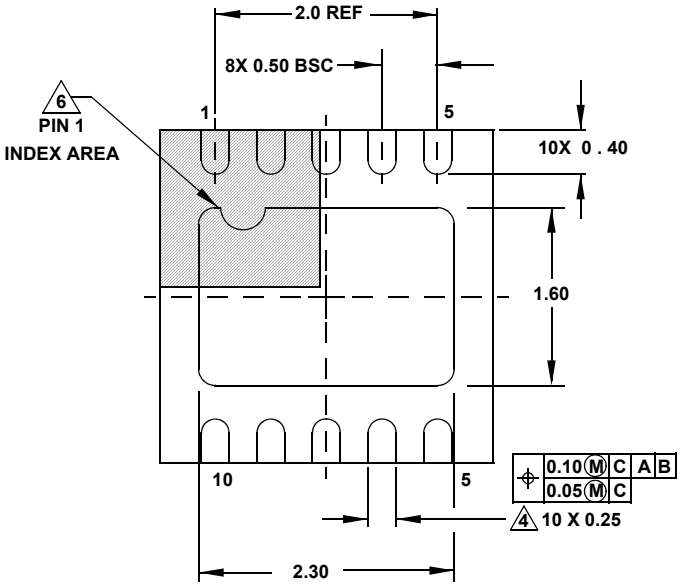
Package Outline Drawing

L10.3x3D

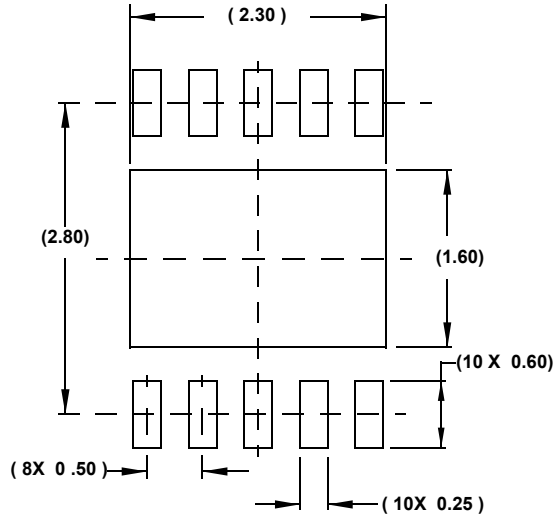
10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 3/10



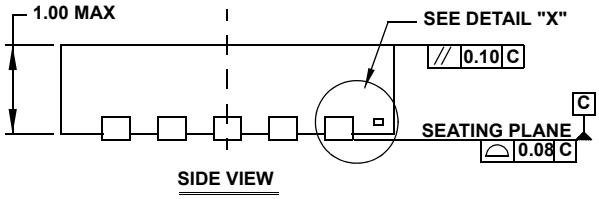
TOP VIEW



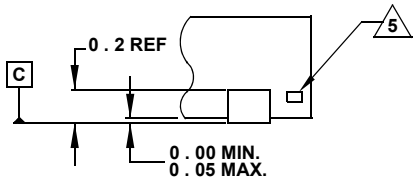
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
   Angular: ±2.50°
4. Dimension applies to the metallized terminal and is measured between 0.015mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-229-WEED-3 except exposed pad length (2.30mm).