Complete Current Share 10A DC/ DC Power Module

ISL8200MM

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The ISL8200MMREP is a simple and easy to use high power, current-sharing DC\DC power module for Datacom\Telecom\FPGA power hungry applications. All that is needed is the ISL8200MMREP, a few passive components and one V_{OUT} setting resistor to have a complete 10A design ready for market.

The ease of use virtually eliminates the design and manufacturing risks while dramatically improving time to market.

Need more output current? Just simply parallel up to six ISL8200MMREP modules to scale up to a 60A solution (see Figure 6 on page 10).

The simplicity of the ISL8200MMREP is in its "Off The Shelf", unassisted implementation. Patented current sharing in multi-phase operation greatly reduces ripple currents, BOM cost and complexity.

The ISL8200MMREP's thermally enhanced, compact QFN package, operates at full load and over-temperature, without requiring forced air cooling. It's so thin it can even fit on the back side of the PCB. Easy access to all pins with few external components, reduces the PCB design to a component layer and a simple ground layer.

Features

- Specifications per DLA VID V62/10608
- Full Mil-Temp Electrical Performance from -55°C to +125°C
- Full Traceability Through Assembly and Test by Date/Trace Code Assignment
- Enhanced Process Change Notification
- Enhanced Obsolescence Management
- Complete Switch Mode Power Supply in One Package
- Patented CurrentShare Architecture Reduces Layout Sensitivity When Modules are Paralleled
- Programmable Phase Shift (1, 2, 3, 4, and 6 phase)
- Extremely Low Profile (2.2mm height)
- Input Voltage Range +3.0 Vto +20V at 10A, Current Share up to 60A
- A Single Resistor Sets V_{OUT} from +0.6V to +6V
- Output Overvoltage, Overcurrent and Over-Temperature, Built-in Protection and Undervoltage indication

Applications* (see page 21)

- Servers, Telecom and Datacom Applications
- Industrial and Medical Equipment
- Point of Load Regulation

Related Literature* (see page 21)

- iSim Model - (See Respective Device Information Page at http//:www.intersil.com)

Complete Functional Schematic

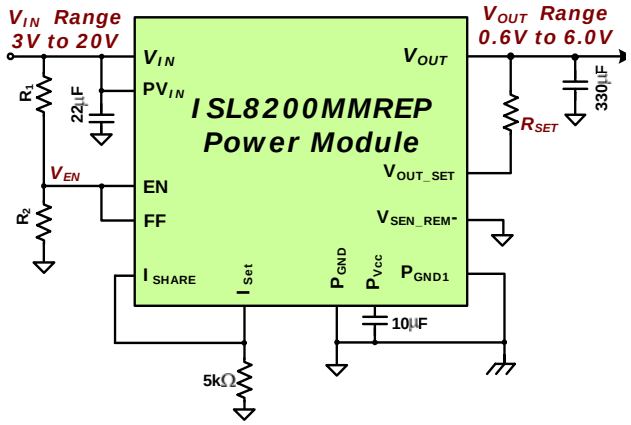


FIGURE 1. COMPLETE 10A DESIGN, JUST SELECT R_{SET} FOR THE DESIRED V_{OUT}

ISL8200MMREP Package

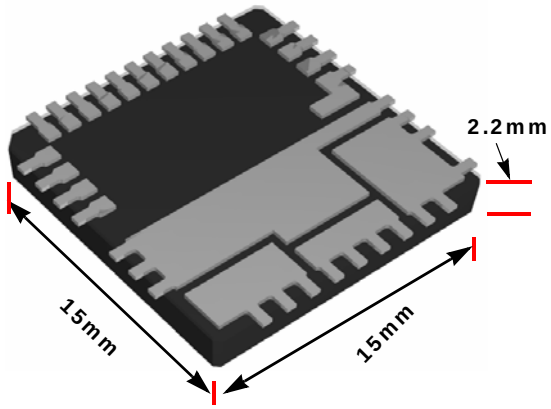


FIGURE 2. THE 2.2mm HEIGHT IS IDEAL FOR THE BACKSIDE OF PCBS WHEN SPACE AND HEIGHT IS A PREMIUM

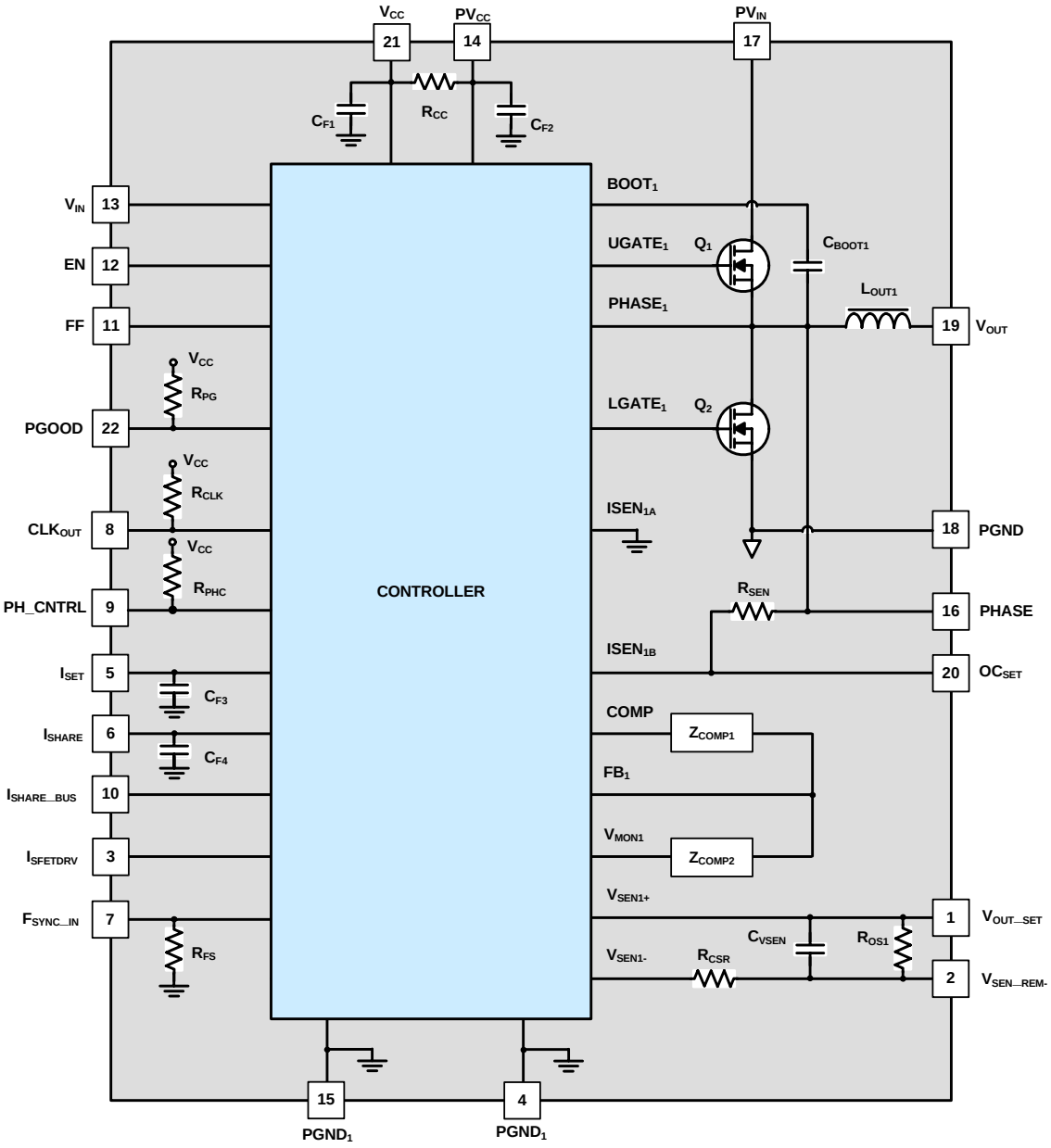
Ordering Information

PART NUMBER (Notes 1, 2)	VENDOR ITEM DRAWING	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL8200MMREP	V62/10608-01XB	8200MMREP	-55 to +125	23 Ld QFN	L23.15x15

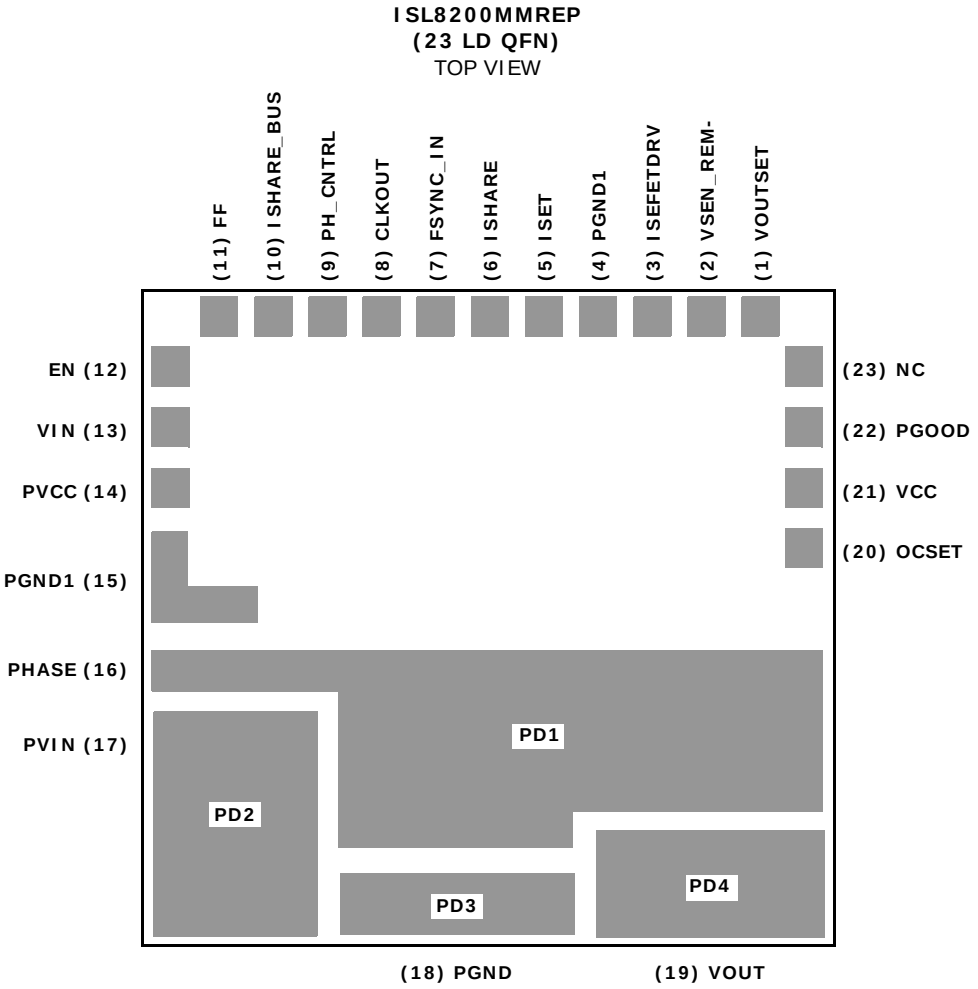
NOTE:

1. Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. For Moisture Sensitivity Level (MSL), please see device information page for ISL8200MMREP. For more information on MSL please see techbrief TB363.

Pinout Internal Circuit



Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	VOUT_SET	Analog Voltage Input - Used with V_{OUT} to program the regulator output voltage. The typical input impedance of VSEN1+ with respect to VSEN1- is 500kΩ Voltage input typ. 0.6V.
2	VSEN_REM-	Analog Voltage Input - This pin is the negative input of standard unity gain operational amplifier for differential remote sense for the regulator, and should connect to the negative rail of the load/processor. This pin can be used for V_{OUT} trimming by connecting a resistor from this pin to the VOUT_SET pin.
3	ISFETDRV	Digital Output - This pin is used to drive an optional NFET, which will connect ISHARE with the system ISHARE bus upon completing a pre-bias start-up. Voltage Output Range: 0V to 5V.
4, 15	PGND1	Normal Ground - All voltage levels are referenced to this pad.This pad provides a return path for the low-side MOSFET drives and internal power circuitries as well as all analog signals. PGND and PGND1 should be connected together with a ground plane.
5	ISET	Analog Current Output - This pin sources a 15µA offset current plus Channel 1's average current. The voltage (VISET) set by an external resistor (RISET) represents the average current level of the local active module. For full-scale current, RISET should be ~10kΩ Output current range: 15µA to 108µA typ.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	PIN DESCRIPTION
6	ISHARE	Analog Current Output - Cascaded system level overcurrent shutdown pin. This pin is used where you have multiple modules configured for current sharing and is used with a common current share bus. The bus sums each of the modules' average current contribution to the load to protect for a overcurrent condition at the load. The pin sources 15µA plus average module's output current. The shared bus voltage (VISHARE) is developed across an external resistor (RISHARE). VISHARE represents the average current of all active channel(s) that connected together. The ISHARE bus voltage is compared with each module's internal reference voltage set by each module's RISET resistor. This will generate and individual current share error signal in each cascaded controller. The share bus impedance RISHARE should be set as RISET/NCTRL, RISET divided by number of active current sharing controllers. The output current from this pin generates a voltage across the external resistor. This voltage, VISHARE, is compared to and internal 1.2V threshold for average overcurrent protection. For full-scale current, RISHARE should be ~10kΩ. Typically 10kΩ is used for RSHARE and RSET. Output Current Range: 15µA to 108µA typ.
7	FSYNC IN	Analog input Control Pin - An optional external resistor (RFS-ext) connected to this pin and ground will increase the oscillator switching frequency. It has an internal 59kΩ resistor for a default frequency of 700kHz. The internal oscillator will lock to an external frequency source when connected to a square wave form. The external source is typically the CLKOUT signal from another ISL8200MMREP or an external clock. The internal oscillator synchronizes with the leading positive edge of the input signal. Input Voltage Range for external source: 0V to 5V Square Wave.
8	CLKOUT	Digital Voltage Output - This pin provides a clock signal to synchronize with other ISL8200MMREP(s). When there is more than one ISL8200MMREP in the system, the two independent regulators can be programmed via PH_CNTRL for different degrees of phase delay.
9	PH_CNTRL	Analog Input - The voltage level on this pin is used to program the phase shift of CLKOUT clock signal to synchronize with other module(s).
10	ISHARE_BUS	Open pin until first PWM pulse is generated. Then, via an internal FET, this pin connects the module's ISHARE to the system's ISHARE bus after pre-bias is complete and soft-start is initiated.
11	FF	Analog Voltage Input - The voltages on this pin is fed into the controller, adjusting the sawtooth amplitude to generate the feed-forward function. Voltage input 0.7 to V_{CC}.
12	EN	This is a double function pin: Analog Input Voltage - The input voltage to this pin is compared with a precision 0.8V reference and enables the digital soft-start. Input Voltage Range is 0V to V_{CC} or V_{IN} through a pull up resistor maintaining a typical current of 5mA. Analog Voltage Output - This pin can be used as a voltage monitor for input bus undervoltage lockout. The hysteresis levels of the lockout can be programmed via this pin using a resistor divider network. Furthermore, during fault conditions (such as overvoltage, overcurrent, and over-temperature), this pin is used to communicate the information to other cascaded modules by pulling low the wired OR as it is an Open Drain. Output Voltage Range is 0V to V_{CC}.
13	VIN	Analog Voltage Input - This pin should be tied directly to the input rail when using the internal linear regulator. It provides power to the internal linear drive circuitry. When used with a supply 5V or below, this pin should be tied directly to PVCC. The internal linear device is protected against the reversed bias generated by the remained charge of the decoupling capacitor at VCC when losing the input rail. Input Voltage Range 0V to 20V.
14	PVCC	Analog Output - This pin is the output of the internal series linear regulator. It provides the bias for both low-side and high-side drives. Its operational voltage range is 3V to 5.6V. The decoupling ceramic capacitor in the PVCC pin is 10µF.
16	PHASE	Analog Output = This pin is the phase node of the regulator. Output Voltage Range 0V to 30V.
17	PVIN	Analog Input - This input voltage is applied to the power FETS with the FET's ground being the PGND pin. It is recommended to place input decoupling capacitance, 22µF, directly between PVIN pin and PGND pin as close as possible to the module. Input Voltage Range: 0V to 20V.
18	PGND	All voltage levels are referenced to this pad. This is the low side MOSFET ground. PGND and PGND1 should be connected together with a ground plane.
19	VOUT	Output voltage from the module. Output Voltage Range: 0.6V to 6V.
20	OCSET	Analog Input - This pin is used with PHASE pin to set the current limit of the module. Input Voltage Range 0V to 30V.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	PIN DESCRIPTION
21	VCC	Analog Input - This pin provides bias power for the analog circuitry. It's operational range is 2.97V to 5.6V. In 3.3V applications, VCC, PVCC and VIN should be shorted to allow operation at the low end input as it relates to the V_{CC} falling threshold limit. This pin can be powered either by the internal linear regulator or by an external voltage source.
22	PGOOD	Analog Output - This pin, pulled up to VCC via a 10kΩ resistor, provides a Power-Good signal when the output is within 9% of nominal output regulation point with 4% hysteresis (13%/9%), and soft-start is complete. PGOOD monitors the outputs (VMON1) of the internal differential amplifiers. Output Voltage Range: 0V to V_{CC}.
23	NC	Not internal connected
PD1	Phase Thermal Pad	Used for both the PHASE pin (Pin # 16) and for heat removal connecting to heat dissipation layers using Vias. Potential should be floating and not electrically connected to anything except PHASE pin 16.
PD2	V_{IN} Thermal Pad	Used for both the PVIN pin (Pin # 17) and for heat removal connecting to heat dissipation layers using Vias. Potential should be floating and not electrically connected to anything except VPVIN pin 17.
PD3	PGND Thermal Pad	Used for both the PGND pin (Pin # 18) and for heat removal connecting to heat dissipation layers using Vias. Potential should be floating and not electrically connected to anything except PGND pin 18.
PD4	V_{OUT} Thermal Pad	Used for both the VOUT pin (Pin # 19) and for heat removal connecting to heat dissipation layers using Vias. Potential should be floating and not electrically connected to anything except VOUT pin 19.

Typical Application Circuits

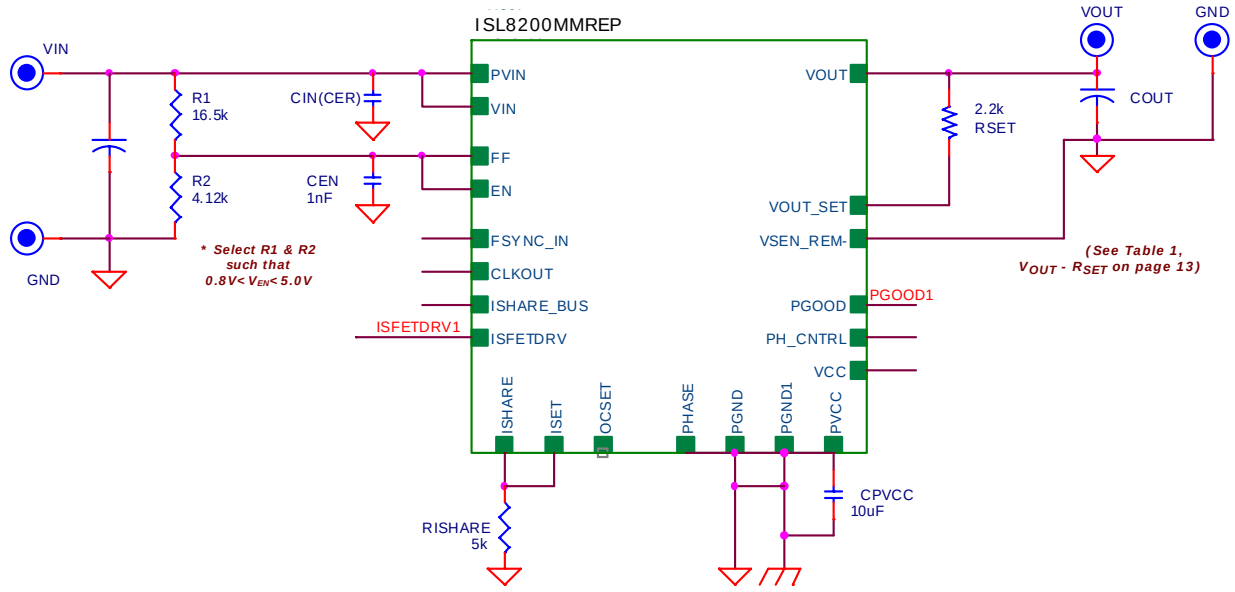


FIGURE 3. SINGLE PHASE 10A 1.2V OUTPUT CIRCUIT

Typical Application Circuits (Continued)

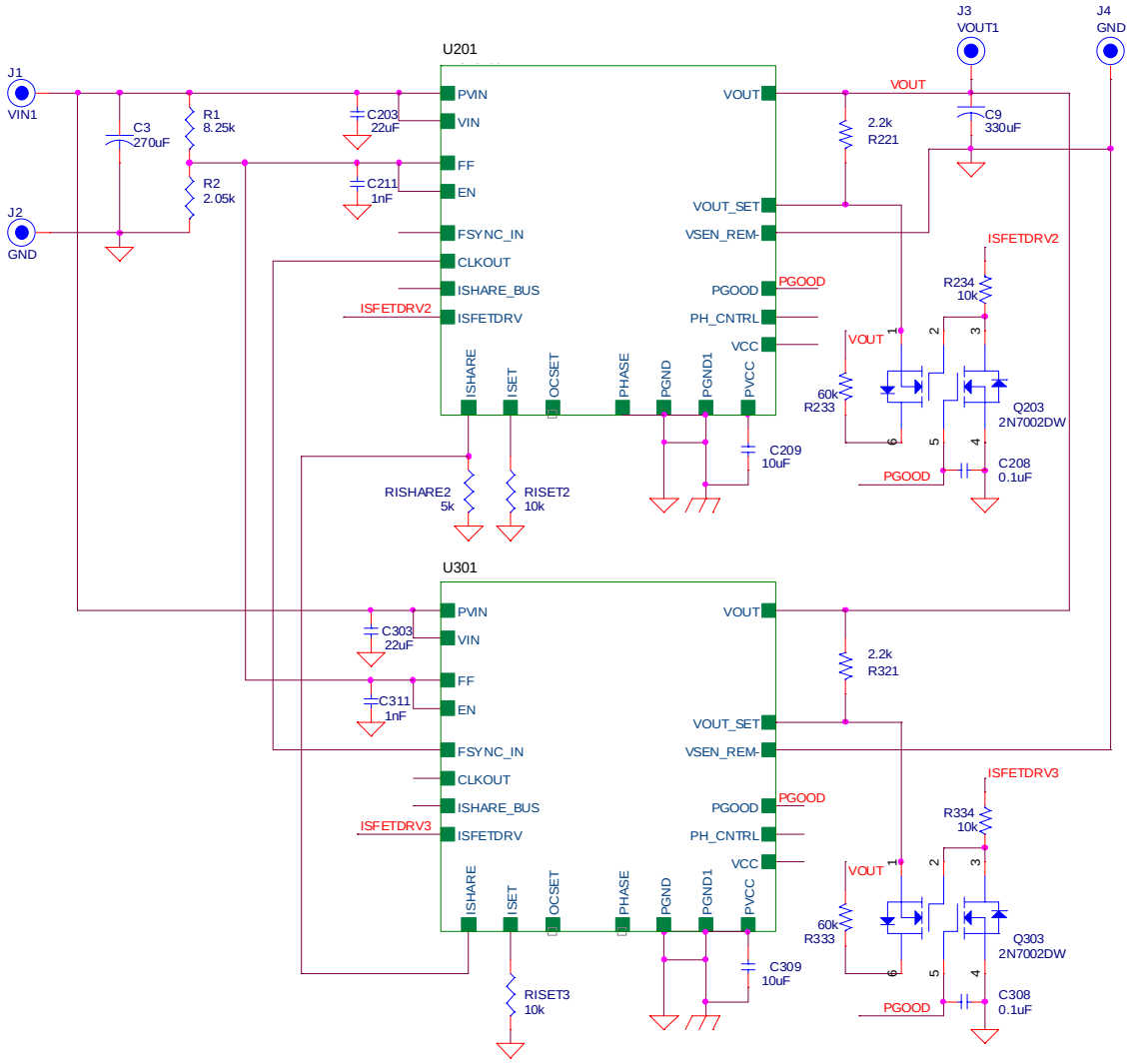


FIGURE 4. TWO PHASE 20A 1.2V OUTPUT CIRCUIT

Absolute Maximum Ratings

Input Voltage, PVIN, V_{IN} . . . . . -0.3V to +27V
Driver Bias Voltage, PVCC . . . . . -0.3V to +6.5V
Signal Bias Voltage, V_{CC} . . . . . -0.3V to +6.5V
BOOT/UGATE Voltage, V_{BOOT} . . . . . -0.3V to +36V
Phase Voltage, V_{PHASE} . . . . . V_{BOOT} - 7V to V_{BOOT} + 0.3V
BOOT to PHASE Voltage,
V_{BOOT} - V_{PHASE} . . . . . -0.3V to V_{CC} + 0.3V
Input, Output or I/O Voltage . . . . . -0.3V to V_{CC} + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charge Device Model (Tested per JESD22-C101C) 1kV
Latch Up (Tested per JESD-78B; Class 2, Level A) . . . 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 3, 4)	13	2.0

Maximum Storage Temperature Range . . . -55°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Input Voltage, PVIN, V_{IN} . . . . . .3V to 20V
Driver Bias Voltage, PVCC . . . . . 3V to 5.6V
Signal Bias Voltage, V_{CC} . . . . . 3V to 5.6V
Boot to Phase Voltage (Overcharged),
V_{BOOT} - V_{PHASE} . . . . . <6V
Junction Temperature Range . . . . . -55°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

3. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. (i.e. 4-layer type without thermal vias – see tech brief TB379) per JEDEC standards except that the top and bottom layers assume solid planes.
4. For θ_{JC}, case temperature location is the center of the package underside.

Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 5)	MAX	UNITS
VCC SUPPLY CURRENT						
Nominal Supply V_{IN} Current	I_{Q_VIN}	PVIN = V_{IN} = 20V; No Load; F_{SW} = 700kHz		36		mA
Nominal Supply V_{IN} Current	I_{Q_VIN}	PVIN = V_{IN} = 4.5V; No Load; F_{SW} = 700kHz		27		mA
Shutdown Supply V_{CC} Current	I_{VCC}	EN = 0V, V_{CC} = 2.97V		9		mA
INTERNAL LINEAR REGULATOR (Note 6)						
Maximum Current	I_{PVCC}	PVCC = 4V TO 5.6V		250		mA
		PVCC = 3V TO 4V		150		mA
Saturated Equivalent Impedance	R_{LDO}	P-Channel MOSFET (V_{IN} = 5V)		1		Ω
POWER-ON RESET (Note 6)						
Rising VCC Threshold				2.85	(Note 8)	V
Falling VCC Threshold				2.65	(Note 8)	V
Rising PVCC Threshold				2.85	(Note 8)	V
Falling PVCC Threshold				2.65	(Note 8)	V
System Soft-start Delay	t_{SS_DLY}	After PLL, V_{CC}, and PVCC PORs, and EN above their thresholds		384		Cycles
ENABLE (Note 6)						
Turn-On Threshold Voltage			(Note 8)	0.8	(Note 8)	V
Hysteresis Sink Current	I_{EN_HYS}		(Note 8)	30	(Note 8)	µA
Undervoltage Lockout Hysteresis	V_{EN_HYS}	V_{EN_RTH} = 10.6V; V_{EN_FTH} = 9V R_{UP} = 53.6kΩ, R_{DOWN} = 5.23kΩ		1.6		V
Sink Current	I_{EN_SINK}	V_{EN} = 1V	(Note 8)			mA
Sink Impedance	R_{EN_SINK}	V_{EN} = 1V			(Note 8)	Ω

Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 5)	MAX	UNITS
OSCILLATOR						
Oscillator Frequency	FOSC	R_{FS} = 59kΩ; Figure 27		700		kHz
Total Variation (Note 6)		V_{CC} = 5V	(Note 8)		(Note 8)	%
FREQUENCY SYNCHRONIZATION AND PHASE LOCK LOOP (Note 6)						
Synchronization Frequency		V_{CC} = 5V		FOSC	(Note 8)	kHz
Input Signal Duty Cycle Range (Note 7)			(Note 8)	50	(Note 8)	%
PWM (Note 6)						
Minimum PWM OFF Time	t_{MIN_OFF}		(Note 8)	345	(Note 8)	ns
Current Sampling Blanking Time	$t_{BLANKING}$			175		ns
OUTPUT CHARACTERISTICS						
Output Continuous Current Range	$I_{OUT(DC)}$	PVIN = V_{IN} = 12V, V_{OUT} = 1.2V	0	-	10	A
Line Regulation Accuracy	$\Delta V_{OUT}/\Delta V_{IN}$	V_{OUT} = 1.2V, I_{OUT} = 0A, PVIN = V_{IN} = 3.5V to 20V	-	0.15	-	%
		V_{OUT} = 1.2V, I_{OUT} = 10A, PVIN = V_{IN} = 5V to 20V	-	0.15	-	%
Load Regulation Accuracy	$\Delta V_{OUT}/\Delta I_{OUT}$	I_{OUT} = 0A to 10A, V_{OUT} = 1.2V, PVIN = V_{IN} = 12V	-	0.1	-	%
Output Ripple Voltage	ΔV_{OUT}	I_{OUT} = 10A, V_{OUT} = 1.2V, PVIN = V_{IN} = 12V	-	30	-	mV_{P-P}
DYNAMIC CHARACTERISTICS						
Voltage Change For Positive Load Step	ΔV_{OUT-DP}	I_{OUT} = 0A to 5A. Current slew rate = 2.5A/µs, PVIN = V_{IN} = 12V, V_{OUT} = 1.2V	-	45	-	mV_{P-P}
Voltage Change For Negative Load Step	ΔV_{OUT-DN}	I_{OUT} = 5A to 0A. Current slew rate = 2.5A/µs, PVIN = V_{IN} = 12V, V_{OUT} = 1.2V	-	55	-	mV_{P-P}
REFERENCE (Note 6)						
Reference Voltage (Include Error and Differential Amplifiers' Offsets)	V_{REF1}			0.6		V
			(Note 8)		(Note 8)	%
DIFFERENTIAL AMPLIFIER (Note 6)						
DC Gain	UG_DA	Unity Gain Amplifier		0		dB
Unity Gain Bandwidth	UGBW_DA			5		MHz
Maximum Source Current for Current Sharing	I_{VSEN1-}	VSEN1- Source Current for Current Sharing when parallel multiple modules each of which has its own voltage loop		350		µA
Output Voltage Swing (Note 7)			0		V_{CC} - 1.8	V
Disable Threshold	V_{VSEN-}	V_{MON1} = Tri-State		V_{CC} - 0.4		V
OVERCURRENT PROTECTION (Note 6)						
Channel Overcurrent Limit	I_{SOURCE}	V_{CC} = 2.97V to 5.6V		108		µA
		V_{CC} = 5V;	(Note 8)	108	(Note 8)	µA
Share Pin OC Threshold	V_{OC_SET}	V_{CC} = 5V (comparator offset included)	(Note 8)	1.20	(Note 8)	V
POWER-GOOD MONITOR (Note 6)						
Undervoltage Falling Trip Point	V_{UVF}	Percentage Below Reference Point	(Note 8)	-13	(Note 8)	%
Undervoltage Rising Hysteresis	V_{UVR_HYS}	Percentage Above UV Trip Point		4		%

Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP (Note 5)	MAX	UNITS
Overvoltage Rising Trip Point	V_{OVR}	Percentage Above Reference Point	(Note 8)	13	(Note 8)	%
Overvoltage Falling Hysteresis	V_{OVF_HYS}	Percentage below OV Trip Point		4		%
PGOOD Low Output Voltage		I_{PGOOD} = 2mA			(Note 8)	V
Sinking Impedance		I_{PGOOD} = 2mA			(Note 8)	Ω
Maximum Sinking Current		V_{PGOOD} < 0.8V		10		mA
OVERVOLTAGE PROTECTION (Note 6)						
OV Latching Up Trip Point		EN = UGATE = LATCH Low, LGATE = High	(Note 8)	120	(Note 8)	%
OV Non-Latching Up Trip Point		EN = Low, UGATE = Low, LGATE = High		113		%
LGATE Release Trip Point		EN = Low/HIGH, UGATE = Low, LGATE = Low		87		%
OVER-TEMPERATURE PROTECTION (Note 6)						
Over-Temperature Trip				150		℃
Over-Temperature Release Threshold				125		℃
INTERNAL COMPONENT VALUES						
Internal Resistor Between PVCC and VCC pin	R_{CC}			5		Ω
Internal Resistor Between PHASE and OCSET Pins	R_{SEN1}			2.2k		Ω
Internal Resistor Between FSYNC_IN and SGND Pins	R_{FS}			59k		Ω
Internal Resistor Between PGOOD and VCC Pins	R_{PG}			10k		Ω
Internal Resistor Between CLKOUT and VCC Pins	R_{CLK}			10k		Ω
Internal Resistor Between PH_CNTRL and VCC Pins	R_{PHC}			10k		Ω
Internal Resistor Between VOUT_SET and VSEN_REM- pin	R_{OS1}			2.2k		Ω

5. Parameters with TYP limits are not production tested, unless otherwise specified.
6. Parameters are 100% tested for internal IC prior to module assembly.
7. Limits should be considered typical and are not production tested.
8. Refer to Defense Logistics Agency (DLA) drawing number V62/10608 for min/max parameters.

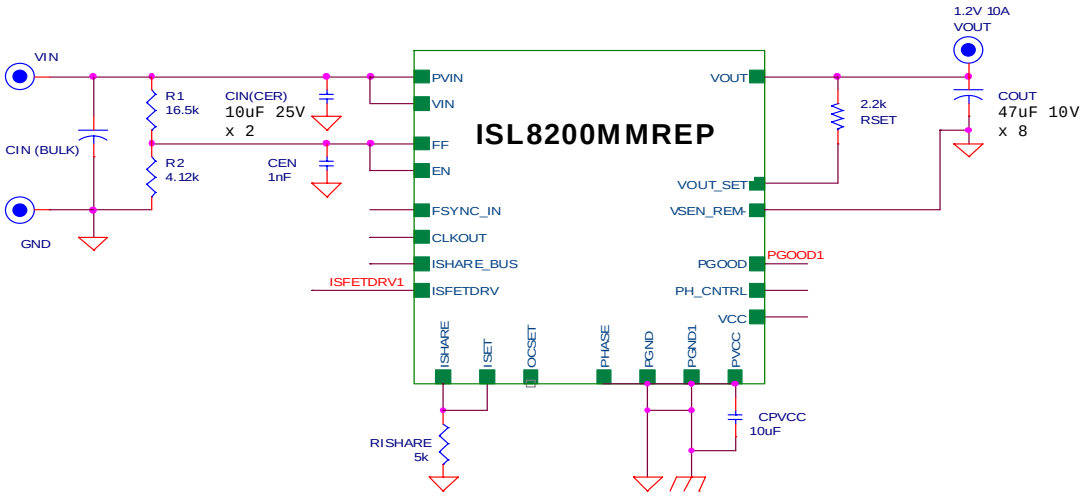


FIGURE 5. TEST CIRCUIT FOR ALL PERFORMANCE AND DERATING GRAPHS

Typical Performance Characteristics

Efficiency Performance

T_A = +25°C, PV_{IN} = V_{IN}, C_{IN} = 220µFx1, 10µF/Ceramic x 2, C_{OUT} = 47µF/Ceramic x 8. The efficiency equation is:

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{OUT}}{P_{IN}} = \frac{(V_{OUT} x I_{OUT})}{(V_{IN} x I_{IN})}$$

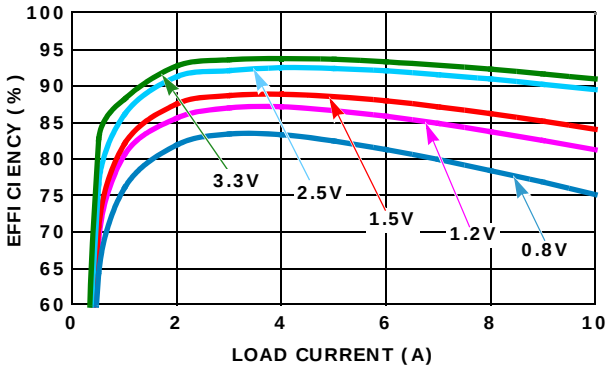


FIGURE 6. EFFICIENCY vs LOAD CURRENT ($5V_{IN}$)

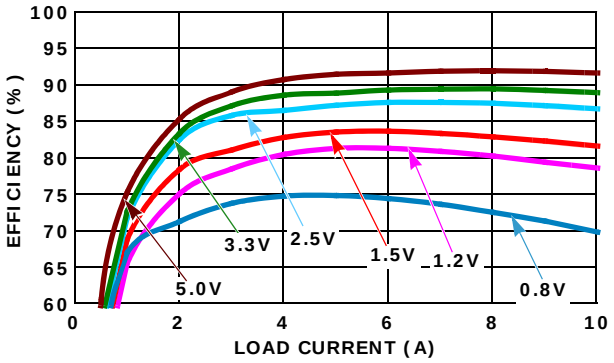


FIGURE 7. EFFICIENCY vs LOAD CURRENT ($12V_{IN}$)

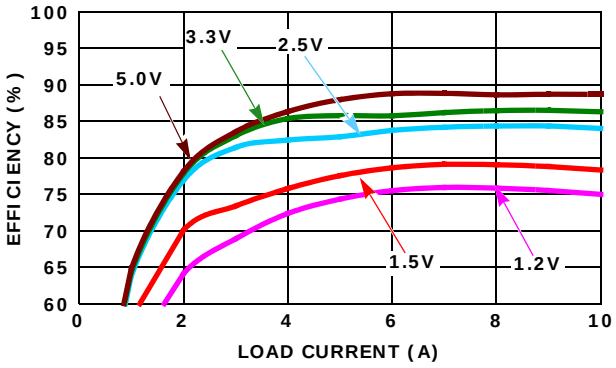


FIGURE 8. EFFICIENCY vs LOAD CURRENT ($20V_{IN}$)

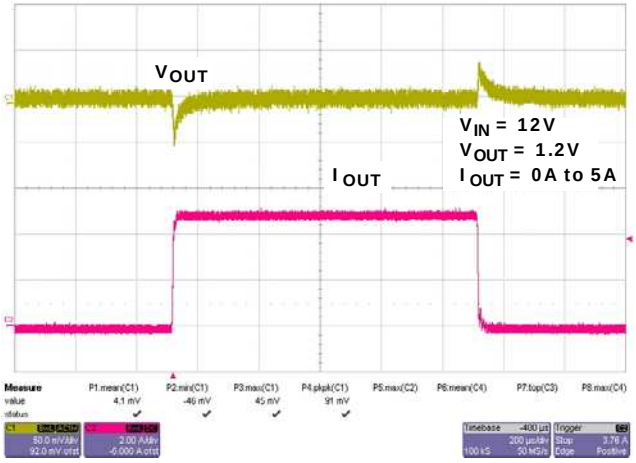


FIGURE 9. 1.2V TRANSIENT RESPONSE

Typical Performance Characteristics (Continued)

Transient Response Performance

T_A = +25°C, PV_{IN} = V_{IN} = 12V, C_{IN} = 220µFx1, 10µF/Ceramic x 2, C_{OUT} = 47µF/Ceramic x 8 I_{OUT} = 0A to 5A, Current slew rate = 2.5A/µs

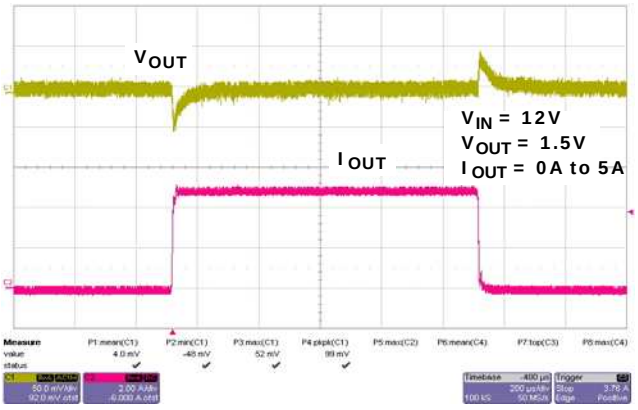


FIGURE 10. 1.5V TRANSIENT RESPONSE

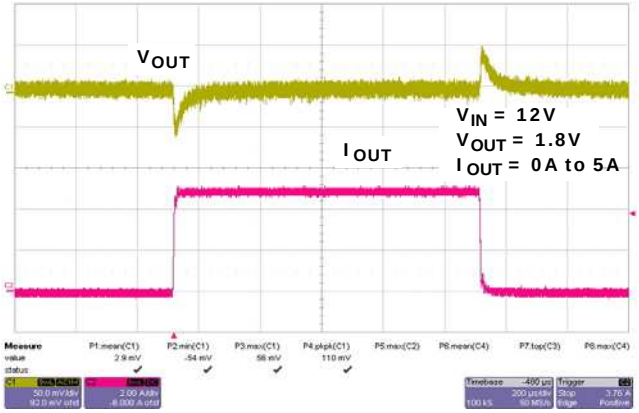


FIGURE 11. 1.8V TRANSIENT RESPONSE

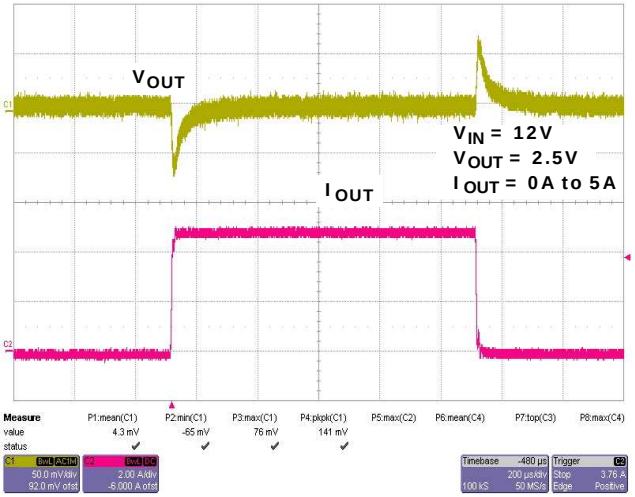


FIGURE 12. 2.5V TRANSIENT RESPONSE

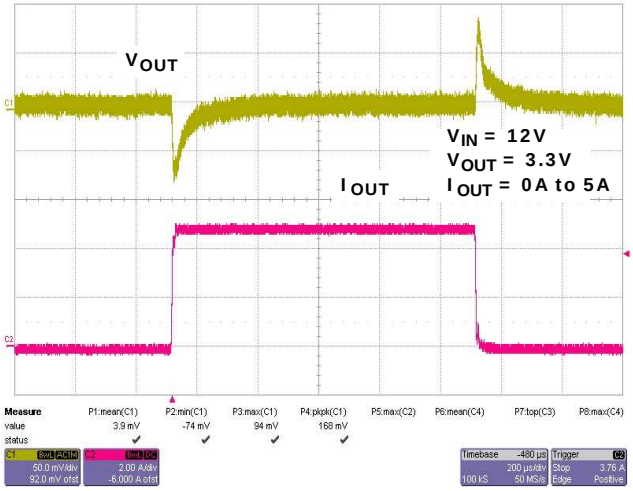


FIGURE 13. 3.3V TRANSIENT RESPONSE

Typical Performance Characteristics (Continued)

Output Ripple Performance T_A = +25°C, PV_{IN} = V_{IN} = 12V, C_{IN} = 220µFx1, 10µF/Ceramic x 2, C_{OUT} = 47µF/Ceramic x 8 I_{OUT} = 0, 5, 10A

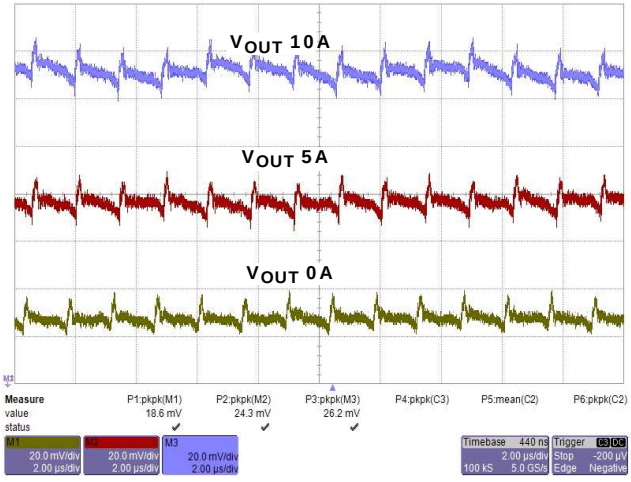


FIGURE 14. 1.2V OUTPUT RIPPLE

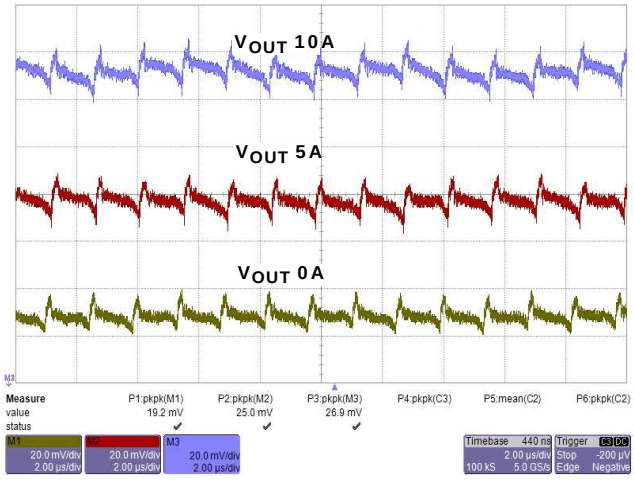


FIGURE 15. 1.5V OUTPUT RIPPLE

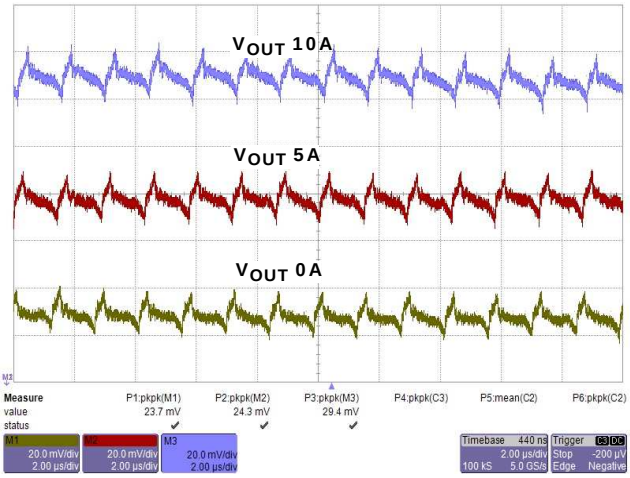


FIGURE 16. 2.5V OUTPUT RIPPLE

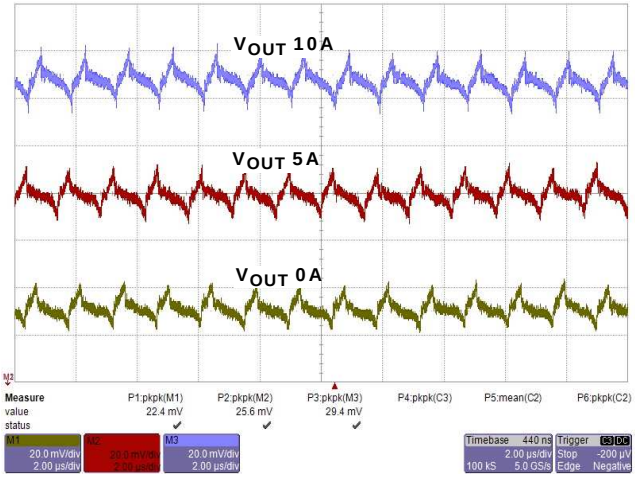


FIGURE 17. 3.3V OUTPUT RIPPLE

Typical Performance Curves

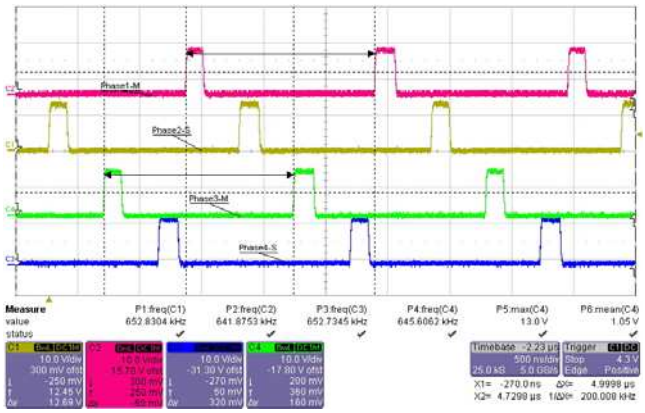


FIGURE 18. 4-BOARD CLOCK SYNC (V_{IN} = 12V)

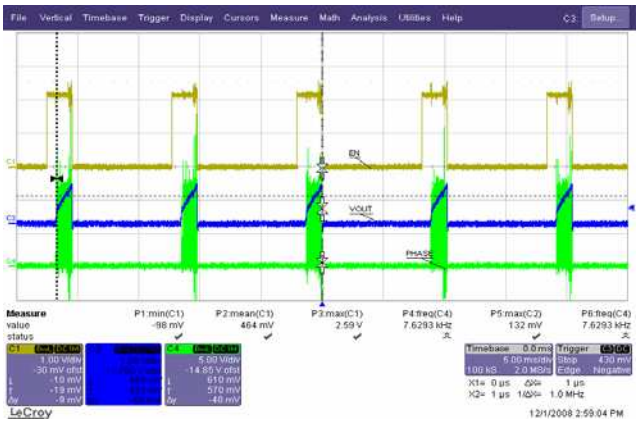


FIGURE 19. OVERCURRENT PROTECTION

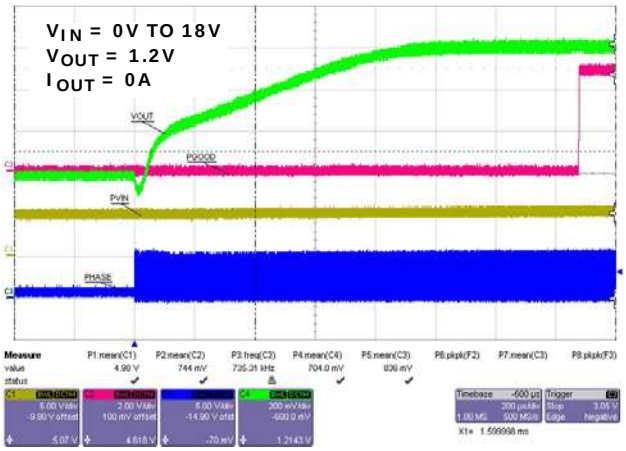


FIGURE 20. 50% PRE-BIAS START-UP

Applications Information

Programming the Output Voltage (R_{SET})

The ISL8200MMREP has an internal 0.6V ± 0.9% reference voltage. Programming the output voltage requires a dividing resistor (R_{SET}) between VOUT_SET pin and VOUT regulation point. The output voltage can be calculated as shown in Equation 1:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{SET}}{R_{OS}}\right) \quad \text{(EQ. 1)}$$

Note: ISL8200MMREP has integrated 2.2kΩ resistances into the module dividing resistor for bottom side (R_{OS1}).

The resistor needed for different output voltages are as shown in Table 1:

TABLE 1. V_{OUT}-R_{SET}

V_{OUT}	0.6V	0.8V	1.0V	1.2V
R_{SET}	0Ω	732Ω	1.47kΩ	2.2kΩ

V_{OUT}	1.5V	1.8V	2.0V	2.5
R_{SET}	3.32kΩ	4.42kΩ	5.11kΩ	6.98kΩ

V_{OUT}	3.3	5.0	6.0	
R_{SET}	10kΩ	16.2kΩ	20kΩ	

The output voltage accuracy can be improved by maintaining the impedance at V_{OUTSET} (internal V_{SEN1+}) at or below 1kΩ effective impedance. Note: the impedance between V_{SEN1+} and V_{SEN1-} is about 500kΩ

Input Supply Voltage Considerations

The module has minimum input voltage PVIN at a given output voltage, which needs to be a minimum of 1.43x output voltage if operating at F_{SW} = 700kHz switching frequency. This is due to the Minimum PWM OFF Time ($t_{MIN-OFF}$).

The equation to determine the minimum V_{IN} to support the required V_{OUT} is given by Equations 2 and 3:

$$V_{IN\_MIN} = \frac{V_{OUT} \times t_{SW}}{t_{SW} - t_{MIN\_OFF}} \quad \text{(EQ. 2)}$$

t_{SW} = switching period = $1/F_{SW}$

for the 700kHz switching frequency = 1428ns

$$V_{IN\_MIN} = 1.43 \times V_{OUT} \quad \text{(EQ. 3)}$$

The voltage on PVCC is recommended to be 5V or above for sufficient gate drive voltage. This can be accomplished by directly connecting a voltage source greater than or equal to 5V (but below 5.6V) to both VIN and PVCC when VIN is below 5V.

Selection of the Input Capacitor

The input filter capacitor should be based on how much ripple the supply can tolerate on the DC input line. The larger the capacitor, the less ripple expected, but consideration should be taken for the higher surge current during power-up. The ISL8200MMREP provides the soft-start function that controls and limits the current surge. The value of the input capacitor can be calculated by Equation 4:

$$C_{IN} = \frac{I_{IN} \times \Delta t}{\Delta V} \quad \text{(EQ. 4)}$$

Where:

C_{IN} is the input capacitance (µF)

I_{IN} is the input current (A)

Δt is the turn on time of the high-side switch (µs)

ΔV is the allowable peak-to-peak voltage (V)

In addition to the bulk capacitance, some low Equivalent Series Inductance (ESL) ceramic capacitance is recommended to decouple between the drain terminal of the high-side MOSFET and the source terminal of the low side MOSFET. This is used to reduce the voltage ringing created by the switching current across parasitic circuit elements.

Output Capacitors

The ISL8200MMREP is designed for low output voltage ripple. The output voltage ripple and transient requirements can be met with bulk output capacitors (C_{OUT}) with low enough Equivalent Series Resistance (ESR). C_{OUT} can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor. The typical capacitance is 330µF and decoupled ceramic output capacitors are used per phase. The internally optimized loop compensation provides sufficient stability margins for all ceramic capacitor applications with a recommended total value of 300µF per phase. Additional output filtering may be needed if further reduction of output ripple or dynamic transient spike is required.

Functional Description

Initialization

The ISL8200MMREP requires V_{CC} and PVCC to be biased by a single supply. Power-On Reset (POR) circuits continually monitor the bias voltages (PVCC and V_{CC}) and the voltage at EN pin. The POR function initiates soft-start operation 384 clock cycles after the EN pin voltage is pulled to be above 0.8V, all input supplies exceed their POR thresholds and the PLL locking time expires. The enable pin can be used as a voltage monitor and to set desired hysteresis with an internal 30µA sinking current going through an external resistor divider. The sinking current is disengaged after the system is enabled. This feature is especially designed for applications that require higher input rail POR for better undervoltage protection. For example, in 12V applications, R_{UP} = 53.6k and R_{DOWN} = 5.23k will set the turn-on threshold (V_{EN_RTH}) to 10.6V and turn-off threshold (V_{EN_FTH}) to 9V, with 1.6V hysteresis (V_{EN_HYS}).

During shutdown or fault conditions, the soft-start is quickly reset while UGATE and LGATE immediately change state (< 100ns) upon the input dropping below POR.

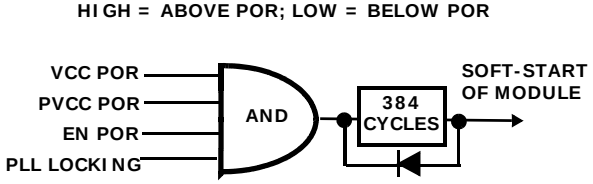


FIGURE 21. SOFT-START INITIALIZATION LOGIC

Voltage Feed-forward

The voltage applied to the FF pin is fed to adjust the sawtooth amplitude of the channel. The amplitude the sawtooth is set to 1.25x the corresponding FF voltage when the module is enabled. This configuration helps to maintain a constant gain ($G_M = V_{IN} \cdot D_{MAX}/\Delta V_{RAMP}$) and input voltage to achieve optimum loop response over a wide input voltage range. The sawtooth ramp offset voltage is 1V (equal to 0.8V* 1.25), and the peak of the sawtooth is limited to V_{CC} - 1.4V. With V_{CC} = 5.4V, the ramp has a maximum peak-to-peak amplitude of V_{CC} - 2.4V (equal to 3V); thus the feed-forward voltage effective range is typically 3x as the ramp amplitude ranges from 1V to 3V.

A 384 cycle delay is added after the system reaches its rising POR and prior to the soft-start. The RC timing at the FF pin should be sufficiently small to ensure that the input bus reaches its static state and the internal ramp circuitry stabilizes before soft-start. A large RC could cause the internal ramp amplitude not to synchronize with the input bus voltage during output start-up or when recovering from faults. A 1nF capacitor is recommended as a starting value for typical application. The voltage on the FF pin needs to be above 0.7V prior to soft-start and during PWM switching to ensure reliable regulation. In a typical application, FF pin can be shorted to EN pin.

Fault Handshake

In a multi-module system, with the EN pins wired OR'ed together, all modules can immediately turn off, at one time, when a fault condition occurs in one or more modules. A fault would pull the EN pin low, disabling all the modules and would not creating current bounce. Thus, no single channel would be over stressed when a fault occurs.

Since the EN pins are pulled down under fault conditions, the pull-up resistor (RUP) should be scaled to sink no more than 5mA current from EN pin. Essentially, the EN pins cannot be directly connected to VCC.

Soft-Start

The ISL8200MMREP has an internal digital pre-charged soft-start circuitry, which has a rise time inversely proportional to the switching frequency and is determined by an digital counter that increments with every pulse of the phase clock. The full soft-start time from 0V to 0.6V can be estimated by Equation 5.

$$t_{SS} = \frac{2560}{f_{SW}} \quad \text{(EQ. 5)}$$

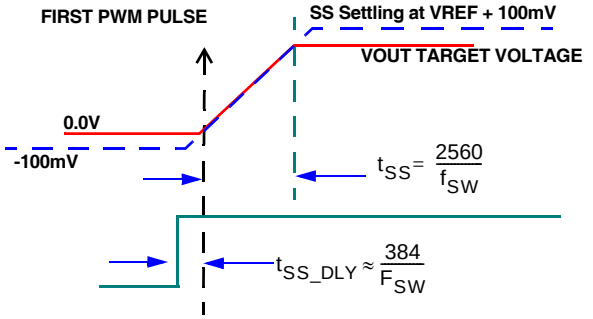


FIGURE 22. SOFT-START WITH VOUT = 0V

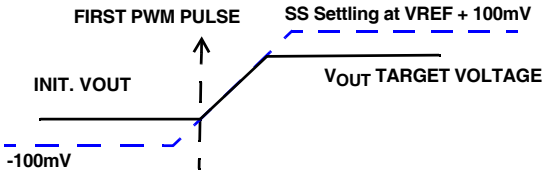


FIGURE 23. SOFT-START WITH V_{OUT} < TARGET VOLTAGE

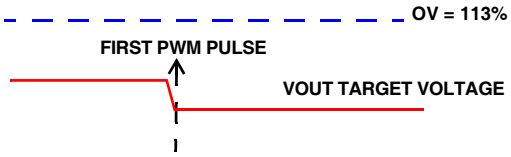


FIGURE 24. SOFT-START WITH V_{OUT} BELOW OV BUT ABOVE FINAL TARGET VOLTAGE

$$R_{UP} = \frac{V_{EN\_HYS}}{I_{EN\_HYS}} \qquad R_{DOWN} = \frac{R_{UP} \bullet V_{EN\_REF}}{V_{EN\_FTH} - V_{EN\_REF}}$$

$$V_{EN\_FTH} = V_{EN\_RTH} - V_{EN\_HYS}$$

$$\Delta V_{RAMP} = \text{LIMIT}(V_{CC\_FF} \times G_{RAMP}, \text{VCC - 1.4V - } V_{RAMP\_OFFSET})$$

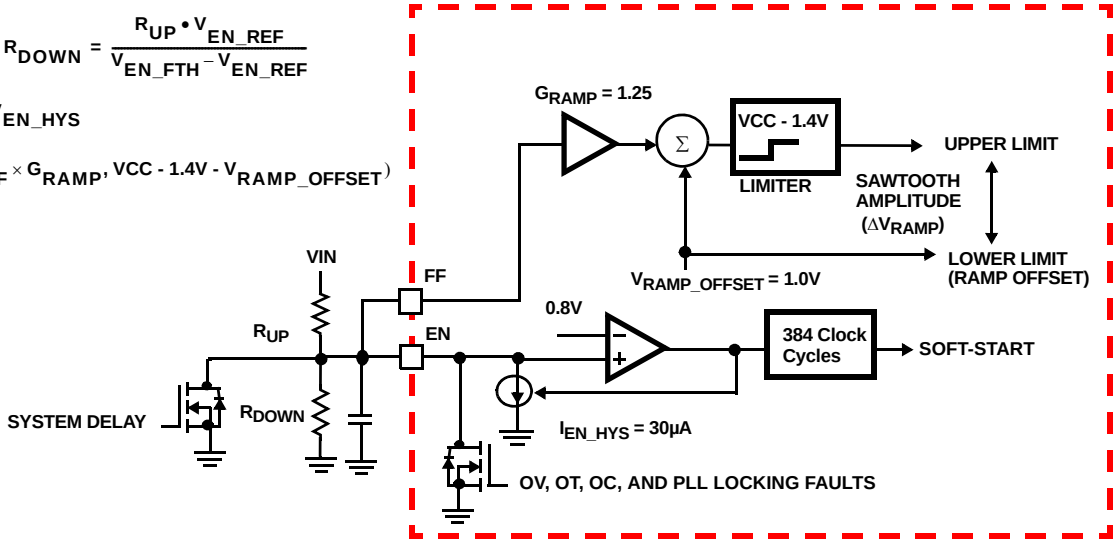


FIGURE 25. SIMPLIFIED ENABLE AND VOLTAGE FEED-FORWARD CIRCUIT

The ISL8200MMREP has the ability to work under a pre-charged output. The PWM outputs will not feed to the drivers until the first PWM pulse is seen. The low side MOSFET is being held low for first clock cycle to provide charge for the bootstrap capacitor. If the pre-charged output voltage is greater than the final target level but less than the 113% setpoint, switching will not start until the output voltage is reduced to the target voltage and the first PWM pulse is generated. The maximum allowable pre-charged level is 113%. If the pre-charged level is above 113% but below 120%, the output will hiccup between 113% (LGATE turns on) and 87% (LGATE turns off) while EN is pulled low. If the pre-charged load voltage is above 120% of the targeted output voltage, then the controller will be latched off and not be able to power-up.

The recommended sequence to start-up at cold temperature is to hold EN pin to ground and release it after PVIN and VIN voltage has reached steady state.

Power-Good

The Power-Good comparators monitor the voltage on the internal VMON1 pin. The trip points are shown in Figure 26. PGOOD will not be asserted until after the completion of the soft-start cycle. The PGOOD pulls low upon both EN's disabling it or the internal VMON1 pin's voltage is out of the threshold window. PGOOD will not be asserted until after the completion of the soft-start cycle. PGOOD will not pull low until the fault presents for three consecutive clock cycles.

The UV indication is not enabled until the end of soft-start. In a UV event, if the output drops below -13% of the target level due to some reason (cases when EN is not pulled low) other than OV, OC, OT, and PLL faults, PGOOD will be pulled low.

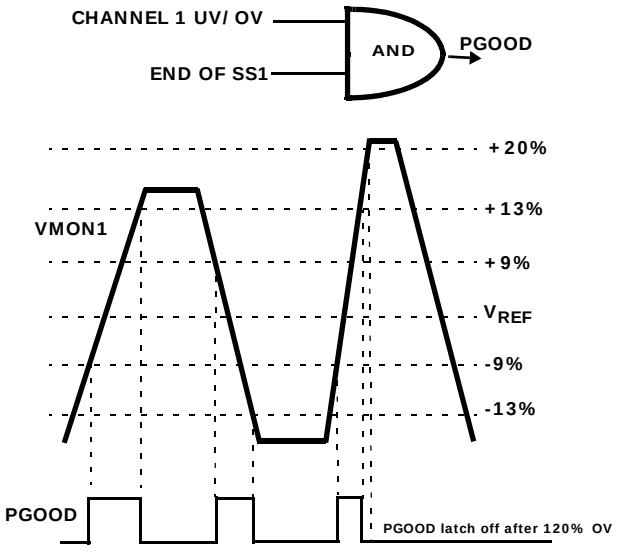


FIGURE 26. POWER-GOOD THRESHOLD WINDOW

Current Share

The IAVG_CS is the current of the module. ISHARE and ISET pins source a copy of IAVG_CS with 15µA offset, i.e., the full scale will be 123µA.

The share bus voltage (VISHARE) set by an external resistor (RISHARE = RISET/NCTRL) represents the average current of all active modules. The voltage (VISET) set by RISET represents the average current of the corresponding module and is compared with the share bus (VISHARE). The current share error signal (ICSH_ER) is then fed into current correction block to adjust each module's PWM pulse accordingly. The current share function provides at least 10% overall accuracy between ICs, when using 1% resistor to sense 10mV signal. The current share bus works for up to 6-phase. Using current sharing feature of ISL8200MMREP below -40°C ambient is not recommended. However, the operation of a single module is acceptable.

When there is only one module in the system, the ISET and ISHARE pins can be shorted together and grounded via a single resistor to ensure zero share error - a resistor value of 5k (paralleling 10k on ISET and ISHARE) will allow operation up to the OCP level.

Overvoltage Protection (OVP)

The Overvoltage (OV) protection indication circuitry monitor the voltage on the internal VMON1 pin.

OV protection is active from the beginning of soft-start. An OV condition (>120%) would latch IC off (the high-side MOSFET to latch off permanently; the low-side MOSFET turns on immediately at the time of OV trip and then turns off permanently after the output voltage drops below 87%). The EN and PGOOD are also latched low at OV event. The latch condition can be reset only by recycling V_{CC}.

There is another non-latch OV protection (113% of target level). At the condition of EN low and the output over 113% OV, the lower side MOSFET will turn on until the output drops below 87%. This is to protect the overall power trains in case of a single channel of a multi-module system detecting OV. The low-side MOSFET always turns on at the conditions of EN = LOW and the output voltage above 113% (all EN pins are tied together) and turns off after the output drops below 87%. Thus, in a high phase count application (multi-module mode), all cascaded modules can latch off simultaneously via the EN pins (EN pins are tied together in multiphase mode), and each IC shares the same sink current to reduce the stress and eliminate the bouncing among phases.

Over-Temperature Protection (OTP)

When the junction temperature of the IC is greater than +150°C (typically), EN pin will be pulled low to inform other cascaded channels via their EN pins. All connected ENs stay low and release after the IC's junction temperature drops below +125°C (typically), a +25°C hysteresis (typically).

Overcurrent Protection (OCP)

The OCP function is enabled at start-up. The module's output current (I_{CS1}) plus a fixed internal 15µA offset forms a voltage (V_{ISHARE}) across the external resistor, R_{ISHARE}. V_{ISHARE} is compared with a precision internal 1.2V threshold. The Channel Overcurrent Limit '108µA OCP' comparator, waits 7-cycles before monitoring for an OCP condition.

In multi-module operation, by connecting modules' ISHARE pin together, results in the V_{ISHARE} representing the average current of all active channels. The total system currents are compared with a precision 1.2V threshold to determine the overcurrent condition as well as each channel having additional overcurrent trip point at 108µA with 7-cycle delay. This scheme helps protect from damaging a module(s) in multi-module mode by not having a single module carrying more than 108µA. Note that it is not necessary for the R_{ISHARE} to be scaled to trip at the same level as the 108µA OCP comparator. Typically the ISHARE pin average current protection level should be higher than the phase current protection level. For instance, when Channel 1 operates independently, the OC trip set by 1.2V comparator can be lower than 108µA trip point as shown in Equation 6.

$$R_{ISEN1} = \frac{\left(I_{OC} + \frac{V_{OUT}}{L} \bullet \left(\frac{1-D}{2F_{SW}} - T_{MIN\_OFF}\right)\right) \bullet RDS}{I_{TRIP}} \quad \text{(EQ. 6)}$$

$$R_{ISHARE} = \frac{1.2V}{I_{TRIP}} \qquad R_{ISET} = R_{ISHARE} \cdot N_{CNTL}$$

where N_{CNTL} is the number of the ISL8200MMREP modules in parallel or multi-module operations; I_{TRIP} = 108µA; I_{OC} is the load overcurrent trip point; T_{MIN_OFF} is the minimum U_{GATE} turn off time that is 350ns; R_{ISHARE} in Equation 7 represents the total equivalent resistance in ISHARE pin bus of all ICs in multiphase or module parallel operation.

ISL8200MMREP has a low-side FET with typical $r_{DS(ON)}$ of 9mΩ (V_{GS} = 10V, I_{DS} = 30A).

Note: ISL8200MMREP has integrated 2.2kΩ resistance (R_{SEN-IN}). Therefore, the equivalent resistance of R_{SEN} is:

$$R_{SEN} = \frac{R_{SEN-EX} \times R_{SEN-IN}}{R_{SEN-EX} + R_{SEN-IN}} \quad \text{(EQ. 7)}$$

The OC trip point varies in a system mainly due to the MOSFET $r_{DS(ON)}$ variations (overprocess, current and temperature). To avoid overcurrent tripping in the normal operating load range, find the R_{SEN} resistor from Equation 8 of I_{PEAK} with:

1. The maximum $r_{DS(ON)}$ at the highest junction temperature
2. The minimum I_{SOURCE} from the "Electrical Specifications" table on page 8.
3. Determine I_{OC} for:

$$I_{OC} > I_{OUT(MAX)} + \frac{(\Delta I_L)}{2} \quad \text{(EQ. 8)}$$

where ΔI_L is the output inductor ripple current.

The relationships between the external R_{SEN-EX} values and the typical output current $I_{OUT(MAX)}$ OCP levels for ISL8200MMREP are shown in Table 2:

TABLE 2.

R_{SEN-EX}	OCP (A) @ V_{IN} = 12V
OPEN	17
50kΩ	15.5
20kΩ	14.5
10kΩ	14
5kΩ	12.5
3kΩ	11
2kΩ	8

In a high input voltage, high output voltage application, such as 20V input to 5V output, the inductor ripple becomes excessive due to the fix internal inductor value. In such application, the output current will be limited from the rating to approximately 70% of the module's rated current.

When OCP is triggered, the controller pulls EN low immediately to turn off UGATE and LGATE.

For overload and hard short condition, the overcurrent protection reduces the regulator RMS output current much less than full load by putting the controller into hiccup mode. A delay time, equal to 3 soft-start intervals, is entered to allow the disturbance to be cleared out. After the delay time, the controller then initiates a soft-start interval. If the output voltage comes up and returns to the regulation, PGOOD transitions high. If the OC trip is exceeded during the soft-start interval, the controller pulls EN low again. The PGOOD signal will remain low and the soft-start interval will be allowed to expire. Another soft-start interval will be initiated after the delay interval. If an overcurrent trip occurs again, this same cycle repeats until the fault is removed.

Oscillator

The Oscillator is a sawtooth waveform, providing for leading edge modulation with 350ns minimum dead time. The oscillator (Sawtooth) waveform has a DC offset of 1.0V. Each channel's peak-to-peak of the ramp amplitude is set to proportional the voltage applied to its corresponding FF pin.

Frequency Synchronization and Phase Lock Loop

The FSYNC_IN pin has two primary capabilities: fixed frequency operation and synchronized frequency

operation. By tying a resistor (R_{FS}) to PGND1 from the FSYNC_IN pin, the switching frequency can be set at any frequency between 700kHz and 1.5MHz. ISL8200MMREP has integrated 59kΩ resistor between FSYNC_IN and PGND1, which set the default frequency to 700kHz. The frequency setting curve shown in Figure 27 is provided to assist in selecting the an externally connected resistor RFS-ext between FSYNC_IN and PGND1 to increase the switching frequency.

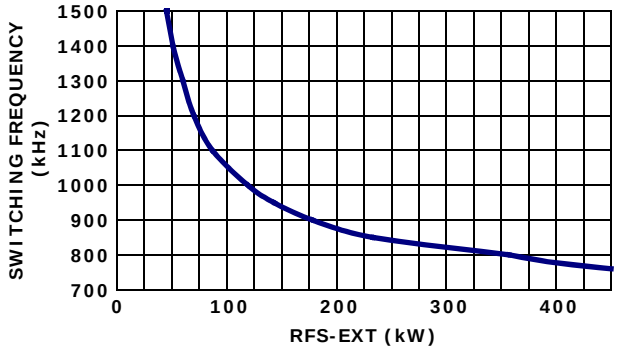


FIGURE 27. RFS-EXT vs SWITCHING FREQUENCY

By connecting the FSYNC_IN pin to an external square pulse waveform (such as the CLKOUT signal, typically 50% duty cycle from another ISL8200MMREP), the ISL8200MMREP will synchronize its switching frequency to the fundamental frequency of the input waveform. The maximum voltage to the FSYNC_IN pin is V_{CC} + 0.3V. The Frequency Synchronization feature will synchronize the leading edge of the CLKOUT signal with the falling edge of Channel 1's PWM clock signal. CLKOUT is not available until the PLL locks.

The locking time is typically 130µs for F_{SW} = 500kHz. EN is not released for a soft-start cycle until FSYNC is stabilized and the PLL is in locking. It is recommended to connect all EN pins together in multiphase configuration.

The loss of a synchronization signal for 13 clock cycles causes the IC to be disabled until the PLL returns locking, at which point a soft-start cycle is initiated and normal operation resumes. Holding FSYNC_IN low will disable the IC.

Setting Relative Phase-Shift on CLKOUT

Depending upon the voltage level at PH_CNTRL, set by the VCC resistor divider output, the ISL8200MMREP operates with CLKOUT phase shifted, as shown in Table 3. The phase shift is latched as V_{CC} raises above POR so it cannot be changed on-the-fly.

TABLE 3.

DECODING PH_CNTRL RANGE	PHASE for CLKOUT WRT CHANNEL 1	REQUIRED PH_CNTRL
< 29% of V_{CC}	-60°	15% V_{CC}
29% to 45% of V_{CC}	90°	37% V_{CC}
45% to 62% of V_{CC}	120°	53% V_{CC}
62% to V_{CC}	180°	V_{CC}

Layout Guide

To achieve stable operation, low losses, and good thermal performance some layout considerations are necessary.

- The ground connection between PGND1 (pin 15) and PGND (pin 18) should be a solid ground plane under the module.
- Place a high frequency ceramic capacitor between (1) PVIN and PGND (pin 18) and (2) a 10µF between PVCC and PGND1 (pin 15) as close to the module as possible to minimize high frequency noise. High frequency ceramic capacitors close to the module between VOUT and PGND will help to minimize noise at the output ripple.
- Use large copper areas for power path (PVIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers.
- Keep the trace connection to the feedback resistor short.
- Use remote sensed traces to the regulation point to achieve a tight output voltage regulation, and keep them in parallel. Route a trace from VSEN_REM- to a location near the load ground, and a trace from feedback resistor to the point-of-load where the tight output voltage is desire.
- Avoid routing any sensitive signal traces, such asthe VOUT and VSENREM- sensing point near the PHASE pin.
- FSYNC_IN is a sensitive pin. If it not use for receiving external synchronization signal, then keep the trace connecting to the pin short. A bypass capacitor value 100pF connecting between FSYNC_IN pin and GND1 can help to bypass the noise sensitivity on the pin.

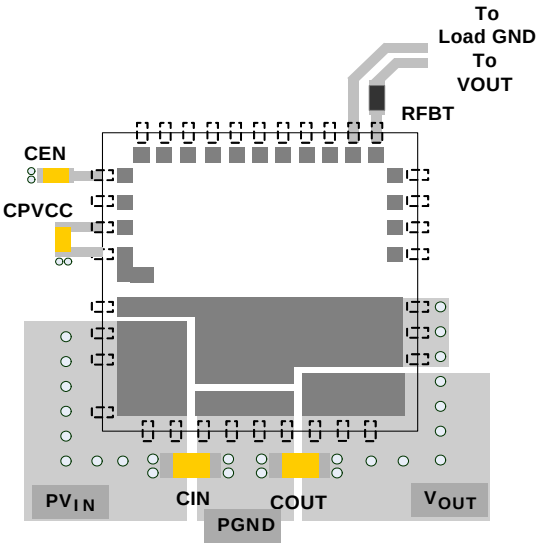


FIGURE 28. RECOMMENDED LAYOUT

Derating Curves

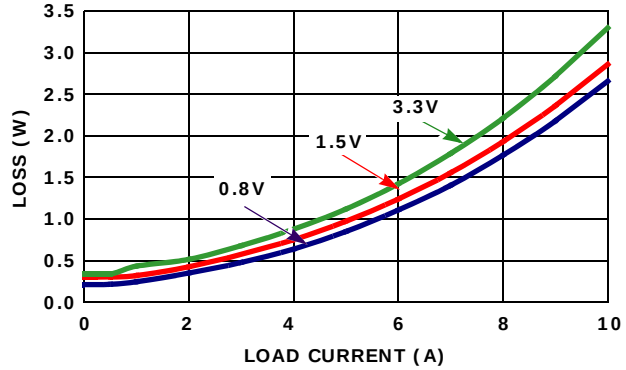


FIGURE 29. POWER LOSS vs LOAD CURRENT ($5V_{IN}$)

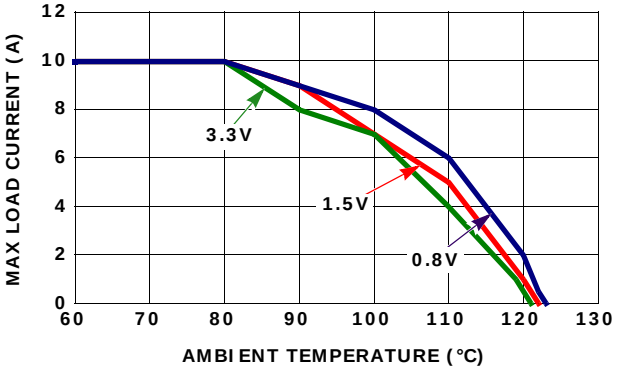


FIGURE 30. DERATING CURVE ($5V_{IN}$)

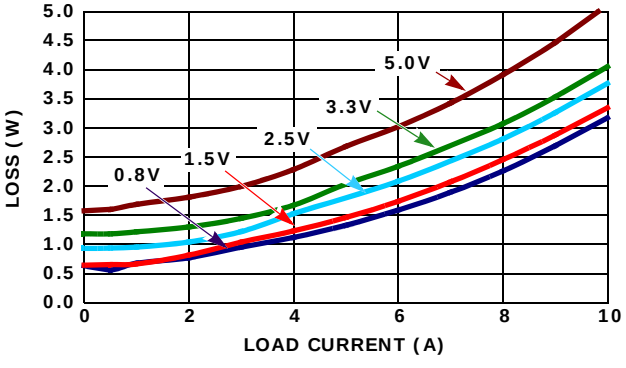


FIGURE 31. POWER LOSS vs LOAD CURRENT ($12V_{IN}$)

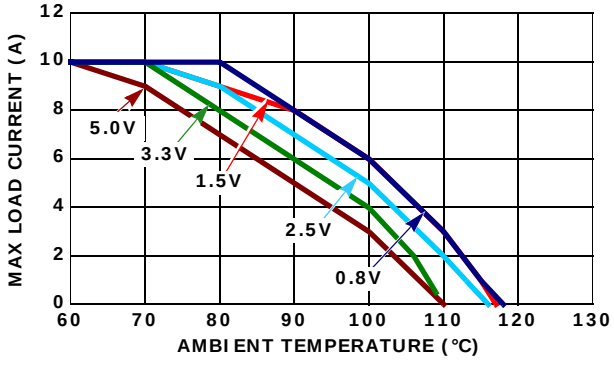


FIGURE 32. DERATING CURVE ($12V_{IN}$)

Thermal Considerations

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual application, other heat sources and design margin should be considered.

Package Description

The structure of ISL8200MMREP belongs to the Quad Flat-pack No-lead package (QFN). This kind of package has advantages, such as good thermal and electrical conductivity, low weight and small size. The QFN package is applicable for surface mounting technology and is being more readily used in the industry. The ISL8200MMREP contains several types of devices, including resistors, capacitors, inductors and control ICs. The ISL8200MMREP is a copper lead-frame based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi component assembly is overmolded with polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown in the package outline drawing L23.15x15 on page 22. The module has a small size of 15mm x 15mm x 2.2mm. Figure 33 shows typical reflow profile parameters. These guidelines are general design rules. Users could modify parameters according to their application.

PCB Layout Pattern Design

The bottom of ISL8200MMREP is a lead-frame footprint, which is attached to the PCB by surface mounting process. The PCB layout pattern is shown in the Package Outline Drawing L23.15x15 on page 22. The PCB layout pattern is essentially 1:1 with the QFN exposed pad and I/O termination dimensions, except for the PCB lands being a slightly extended distance of 0.2mm (0.4mm max) longer than the QFN terminations, which allows for solder filleting around the periphery of the package. This ensures a more complete and inspectable solder joint. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) will improve the thermal performance, diminishing returns will be seen as more and more vias are added. Simply use as many vias as practical for the thermal land size and your board design rules allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. Stencil aperture size to land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown in the Package Outline Drawing L23.15x15 on page 22. The gap width between pad to pad is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing “smooths” the aperture walls resulting in reduced surface friction and better paste release which reduces voids. Using a trapezoidal section aperture (TSA) also promotes paste release and forms a “brick like” paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) QFN.

Reflow Parameters

Due to the low mount height of the QFN, “No Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the QFN. The profile given in Figure 33 is provided as a guideline, to be customized for varying manufacturing practices and applications.

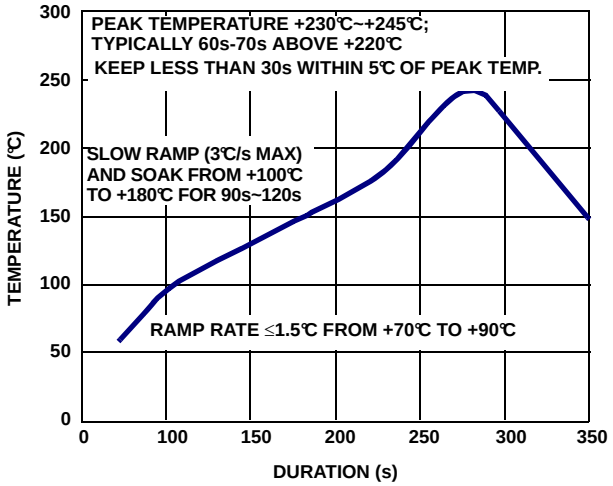


FIGURE 33. TYPICAL REFLOW PROFILE

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
11/2/11	FN7690.1	In support of new product information database & website: Device Part Number changed on page 1 and top of all following pages. (per IT: Device number on page 1 must be unique and not match Marketing Part number found in Order Info).
8/20/10	FN7690.0	Initial Release

Products

Intersil Corporation is a leader in the design and manufacture of high-performance analog semiconductors. The Company's products address some of the industry's fastest growing markets, such as, flat panel displays, cell phones, handheld products, and notebooks. Intersil's product families address power management and analog signal processing functions. Go to www.intersil.com/products for a complete list of Intersil product families.

* For a complete listing of Applications, Related Documentation and Related Parts, please see the respective device information page on intersil.com: ISL8200MMREP

To report errors or suggestions for this datasheet, please go to: www.intersil.com/askourstaff

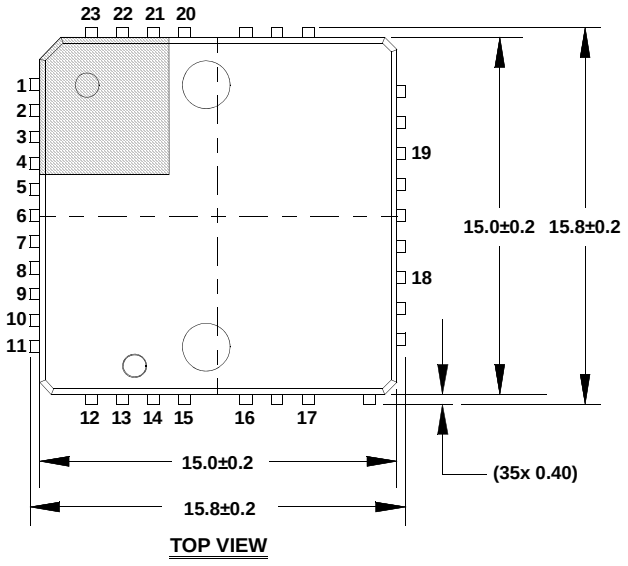
FITs are available from our website at:
http://rel.intersil.com/reports/search.php

Package Outline Drawing

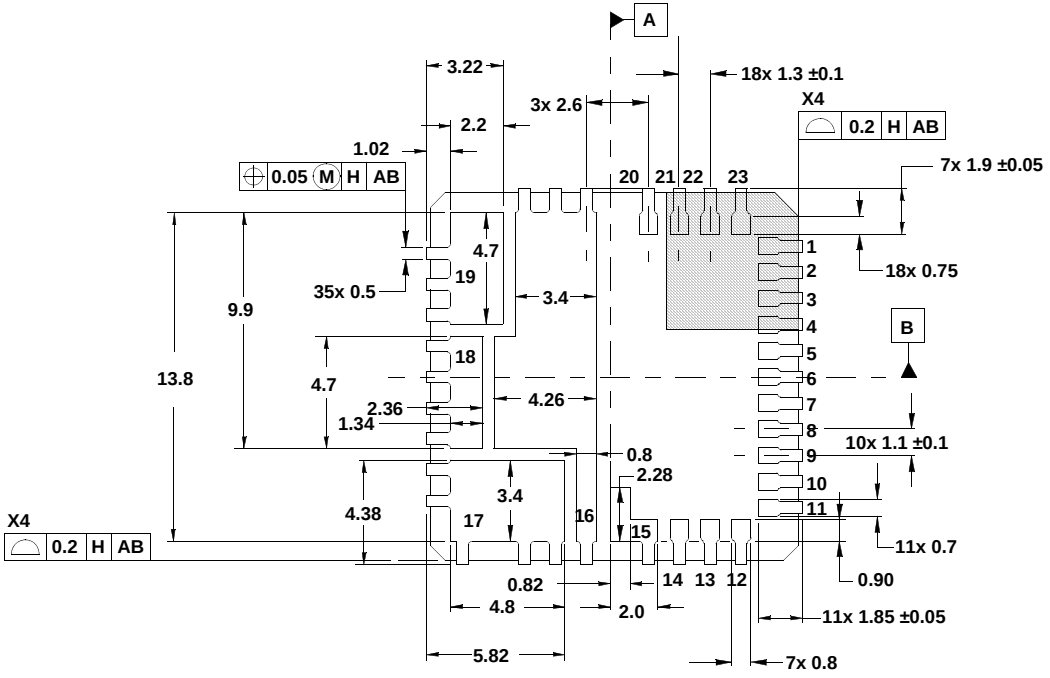
L23.15x15

23 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN)

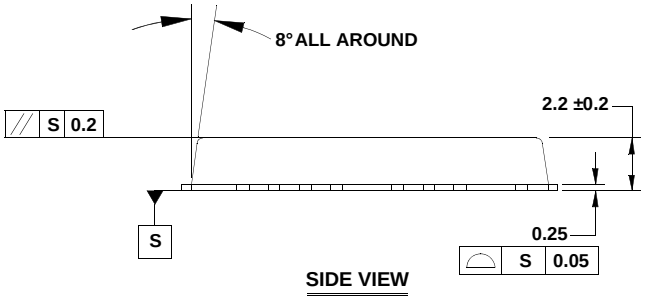
Rev 2, 4/10



TOP VIEW



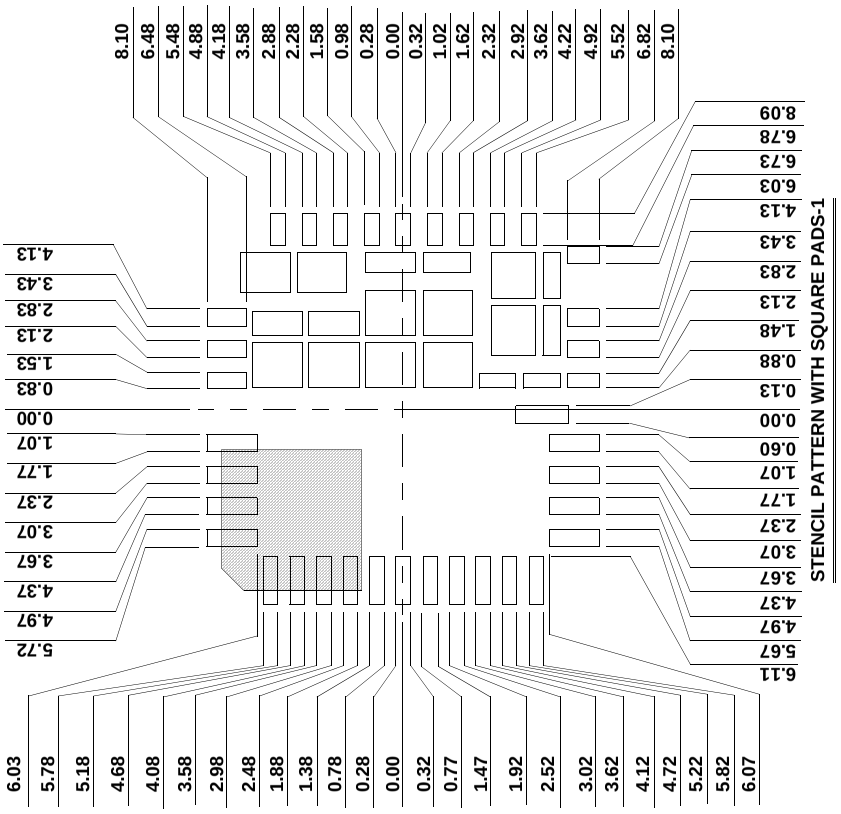
BOTTOM VIEW

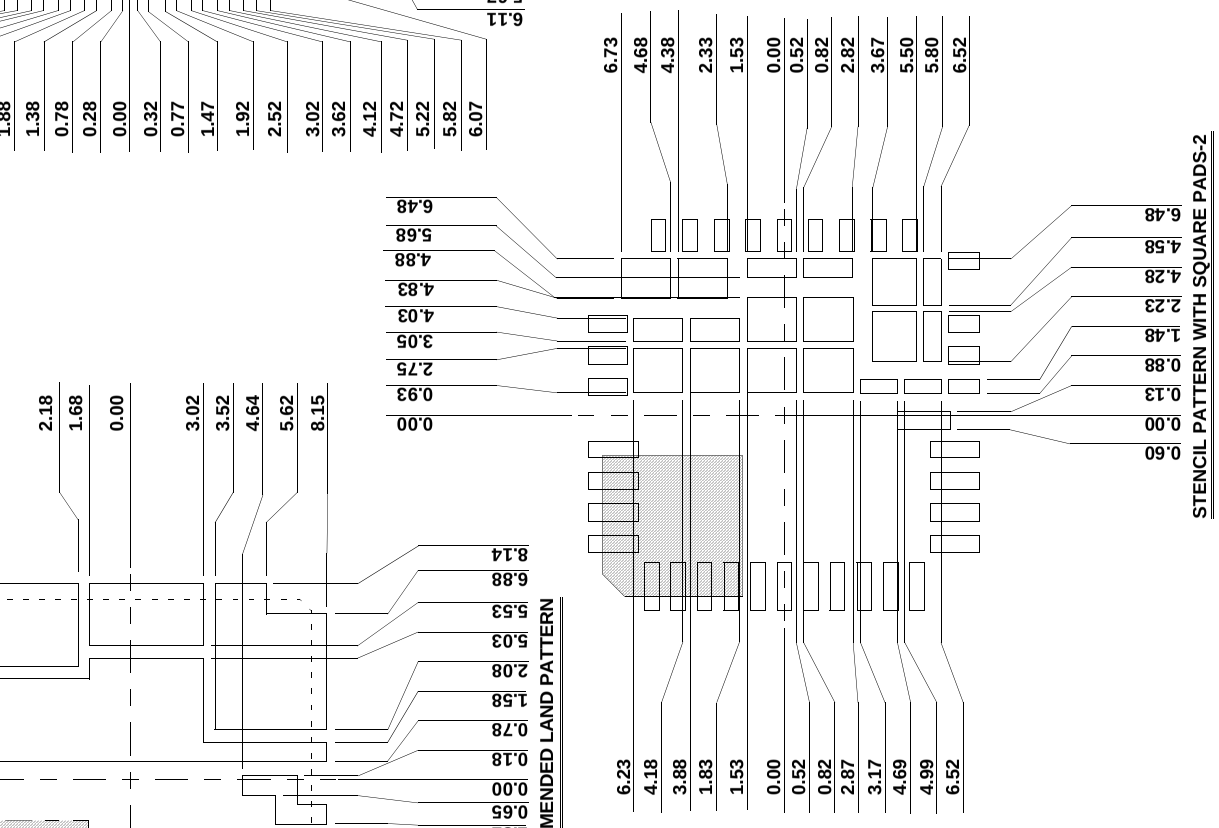


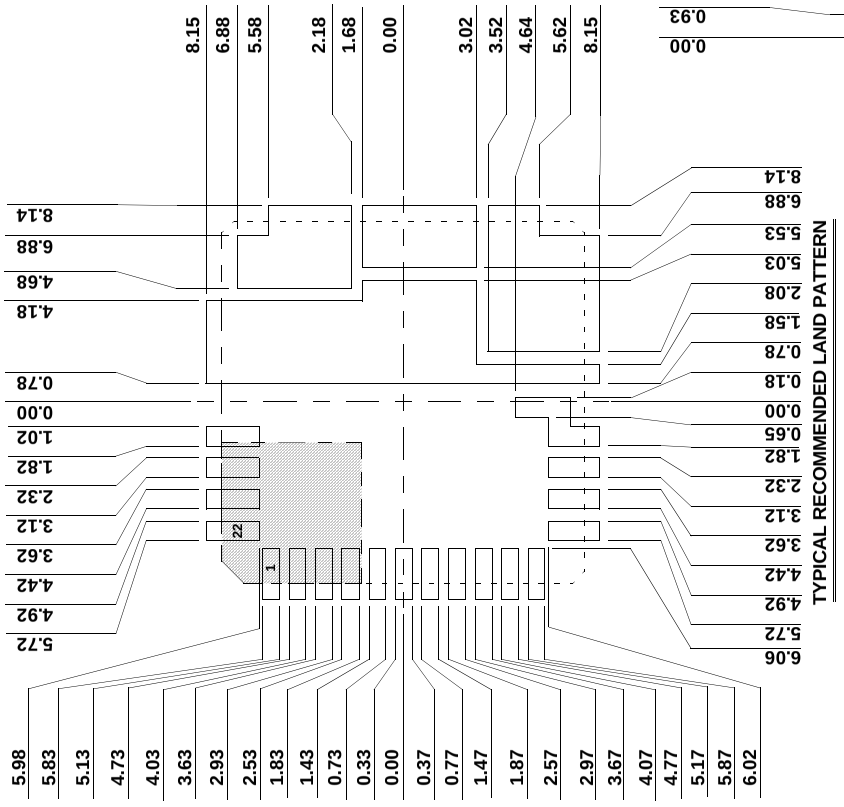
SIDE VIEW

NOTES:

1. Dimensions are in millimeters.
2. Unless otherwise specified, tolerance : Decimal ± 0.2; Body Tolerance ±0.2mm
3. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.


STENCIL PATTERN WITH SQUARE PADS-1


STENCIL PATTERN WITH SQUARE PADS-2


TYPICAL RECOMMENDED LAND PATTERN