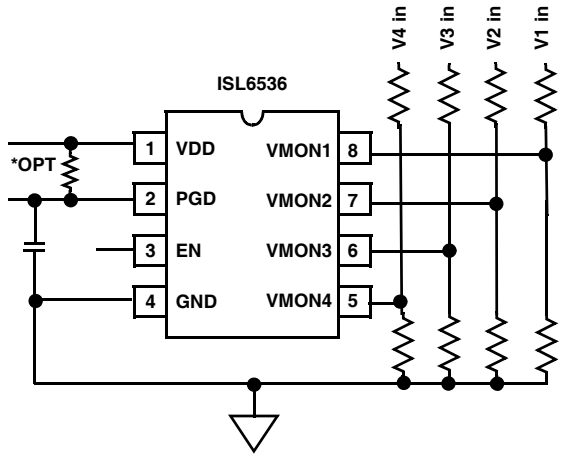
Four Channel Supervisory IC

The ISL6536 is a four channel supervisory IC designed to monitor voltages >, = 0.7V. This IC bias range is from 2.7V to 4V but can supervise any positive voltage using an external resistor divider to translate to a lower voltage for comparison to the internal 0.63V reference.

Once properly biased and enabled when all four voltage monitor (VMON) inputs are satisfied the PGOOD output will be immediately released to go high to signal that voltage is valid on all four rails. Subsequently when the monitored voltage on any rail drops below its user defined threshold point, the PGOOD output is pulled low. Each rail's VMON point is independently adjustable with a resistor divider. The PGOOD output is guaranteed to be valid with IC bias lower than 1V. The VMON inputs will ignore 30µs transients on the monitored supplies. The PGOOD output is an open-drain to allow ORing of multiple signals and interfacing to a range of logic levels. The ENABLE input provides for a reset of the PGOOD output when it is pulled down below 0.5V. With an internal 10uA pull-up to VDD it can be signalled with common logic or pulled to ground with a push button switch.

Typical Application Schematic



Features

- Adjustable undervoltage lockout for each supply
- Active high PGOOD Output
- Guaranteed PGOOD Valid to Falling VDD < 1V
- VMON Glitch Immunity
- Pb-Free (RoHS Compliant)

Applications

- Graphics Cards
- Multi voltage DSPs and Processors
- µP Voltage Monitoring
- Embedded Control Systems
- Intelligent Instruments
- Medical Equipment
- Network Routers
- Portable Battery-Powered Equipment
- Set-Top Boxes
- Telecommunications Systems

Ordering Information

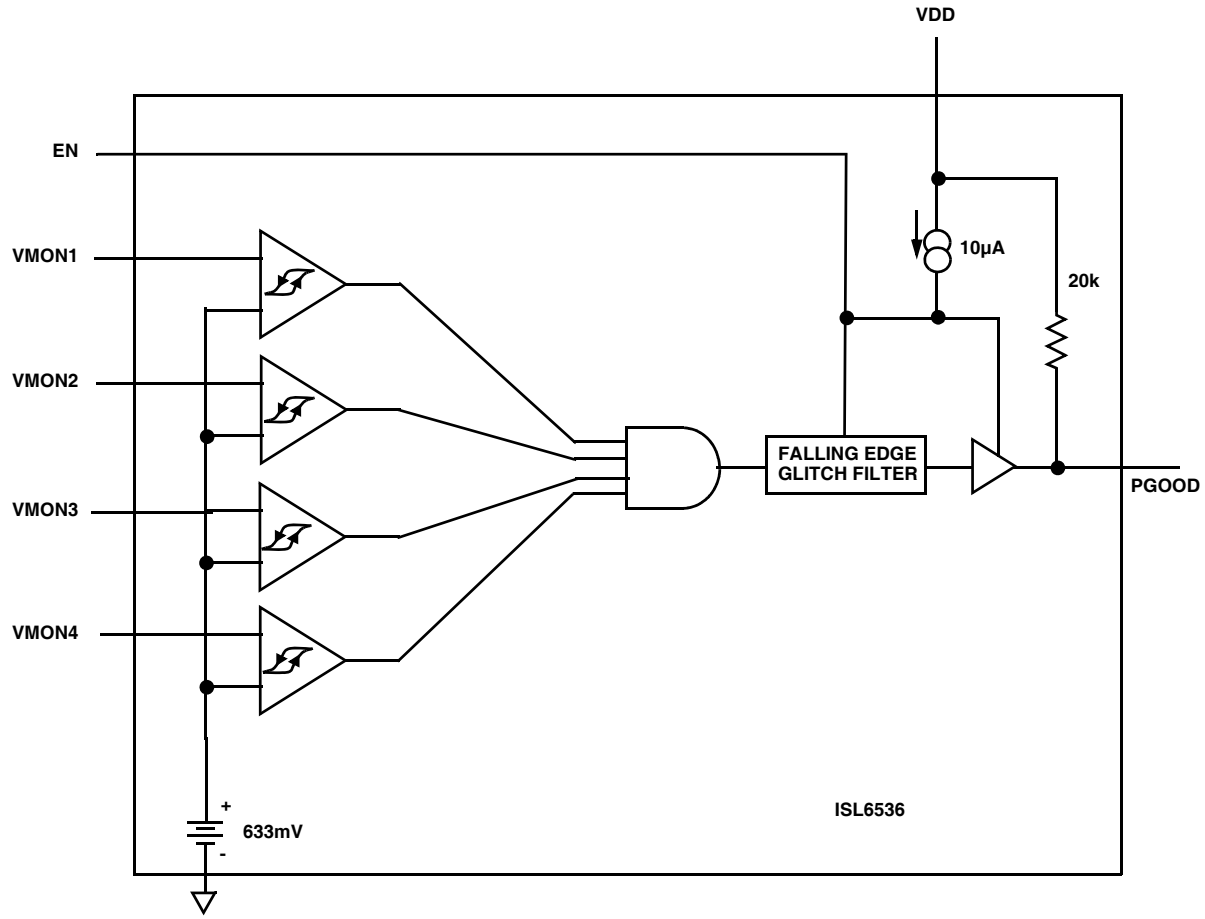
PART NUMBER (Note 2)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL6536IBZ	6536 IBZ	-40 to +85	8 Ld SOIC	M8.15

NOTES:

1. Add "-T*" suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

ISL6536	PIN NAME	FUNCTION DESCRIPTION
1	VDD	Bias IC from nominal 2.7V to 4V
2	PGOOD	PGOOD is the boolean AND function of all the UV inputs being satisfied. This is an open drain output and can be pulled high to the appropriate level with an external resistor. Additionally a 20kΩ pull up to VDD is provided internally.
3	ENABLE	Enabling input for supervisory function. Has a 10µA pull-up to VDD
4	GND	IC ground
5-8	VMON1 VMON2 VMON3 VMON4	These inputs provide for a programmable monitored voltage threshold referenced to an internal 0.63V reference. These inputs have a 30µs glitch filter to prevent transient upsets from being recognized by PGOOD.



Absolute Maximum Ratings

VDD . . . . . +5.5V
VMON, PGOOD, ENABLE. . . . . -0.3V to VDD+0.3V
ESD Classification . . . . . 4kV (HBM)

Operating Conditions

VDD Supply Voltage Range. . . . . +2.7V to +4V
Temperature Range (T_A) . . . . . -40°C to 85°C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)
8 Ld SOIC	108

Maximum Junction Temperature . . . . . 150°C
Maximum Storage Temperature Range. . . . . -65°C to 150°C
Pb-Free Reflow Profile. . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board. See Tech Brief TB379 for details.
2. All voltages are relative to GND, unless otherwise specified.

Electrical Specifications

Nominal VDD = 3.3V, $T_A = T_J$ = -40°C - 85°C, Unless Otherwise Specified.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 3)	TYP	MAX (Note 3)	UNIT
BIAS						
IC Supply Current	I_{VDD}	VMON > VMON_L2H		165	1000	µA
VDD Power On	VDD_L2H	VDD low to high		2.6		V
VDD Power On Reset	VDD_POR	VDD high to low		2.4		V
PGOOD						
Pull-Down Current	$_{PG}$pd	VPGOOD = 0.5V		2		mA
Pull-Up Resistance	$_{PG}$pu			20		kΩ
Output Low	V_{PGl}	V_{DD} = 1V		0.05	0.1	V
Delay from VMON Rising	t_{PG}delVMON	Last valid input = Vth to PG release		2		µs
Delay from EN Rising	t_{PG}delENR	EN high to PG release		0.05		µs
Delay from EN Falling	t_{PG}delENF	EN low to PG pulling low		0.015		µs
ENABLE						
Rising Threshold	V_{EN}	ENABLE Low to High Threshold	0.4VDD	0.5VDD	0.6VDD	V
Threshold Hysteresis	V_{EN_HYS}			0.065		V
Pull-up Current	I_{ENpu}	VEN = 0.5V		10		µA
VMON Input						
Falling Threshold	3.3VMON_H2L	T_J = +25°C	0.623	0.633	0.643	V
Falling Threshold Temp Coeff.	3.3VMON_TC			100		uV/°C
Hysteresis	VVMON_HYS		-	10	-	mV
Range	VMON_RNG		-	8	-	mV
Glitch Filter Duration	TFIL	VMON glitch to PGOOD low Filter	-	30	-	µs

NOTE:

3. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

ISL6536 Description and Operation

The ISL6536 is a four channel supervisory IC designed to monitor multiple voltages greater than 0.7V. This IC is suitable for both microprocessors or industrial system applications.

Upon VDD bias power up the PGOOD output is held low with VDD as low as 0V. Once biased to 2.6V and enabled the IC continuously monitors from one to four voltages independently through external resistor dividers comparing each VMON pin voltage to an internal 0.63V reference.

Once all VMON input voltages rise above 0.63V the PGOOD (power good) output signal is released and is pulled high via an external pull resistor to indicate that the power conditions have been met. The PGOOD output is an open-drain to allow ORing of the signals and interfacing to a wide range of logic levels.

Once any VMON input falls below 0.63V the PGOOD output is pulled low, the VMON inputs are designed to reject fast transients (30µs).

If less than four voltages are being monitored, connect the unused VMON pins to VDD.

The PGOOD pin has an internal 20kΩ pull-up to VDD making an external pull-up resistor unnecessary.

Figure 1 illustrates the operational timing diagram.

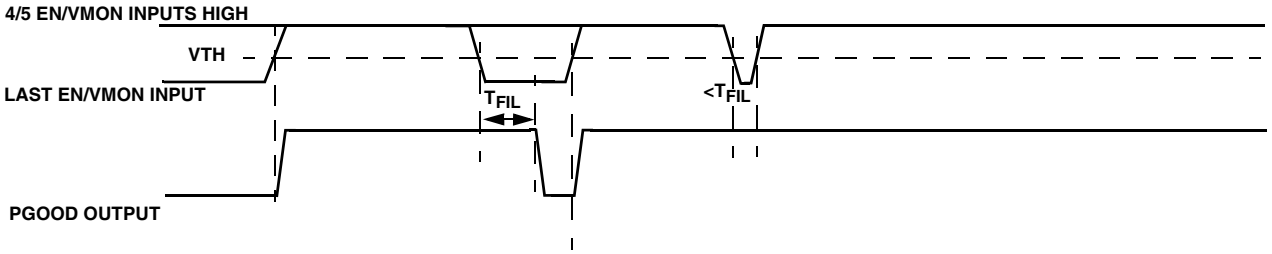


FIGURE 1. ISL6536 OPERATIONAL TIMING DIAGRAM

Typical Performance Curves

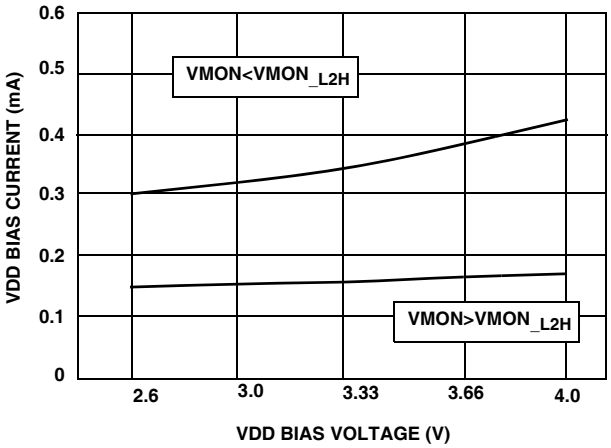


FIGURE 2. VDD CURRENT vs. VDD VOLTAGE

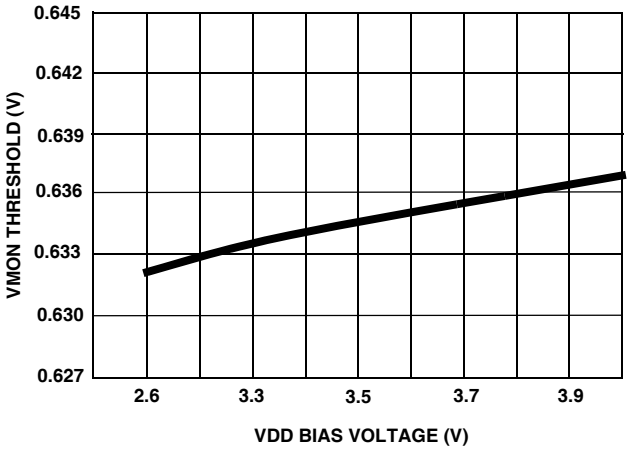


FIGURE 3. VMON THRESHOLD vs. VDD VOLTAGE

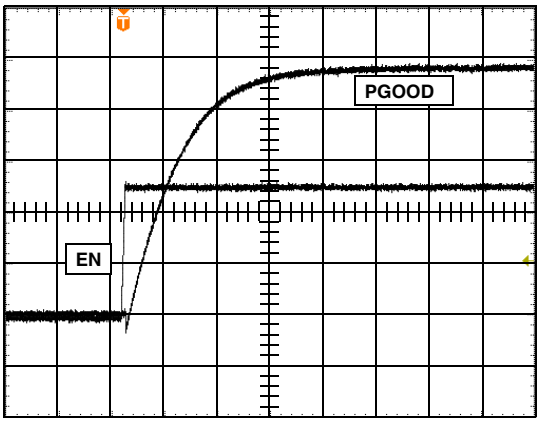


FIGURE 4. EN HIGH to PGOOD

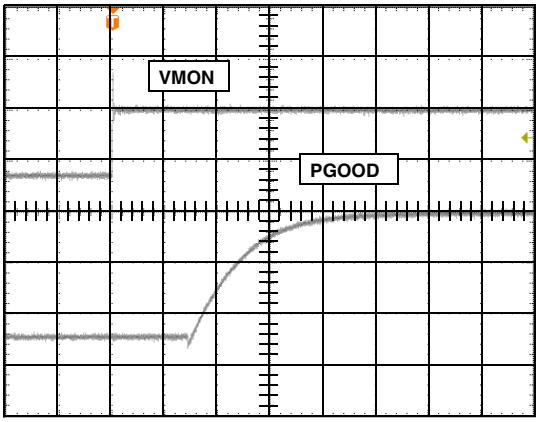


FIGURE 5. VMON HIGH to PGOOD

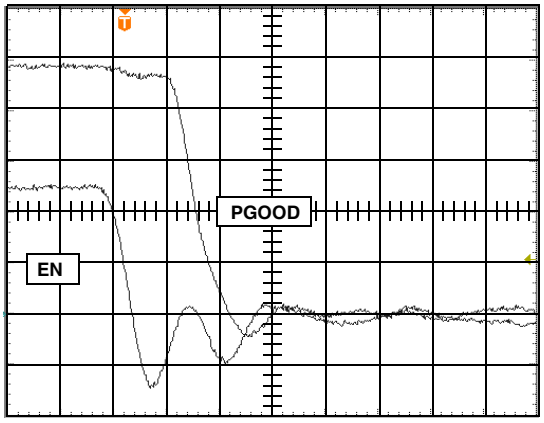


FIGURE 6. EN LOW to PGOOD

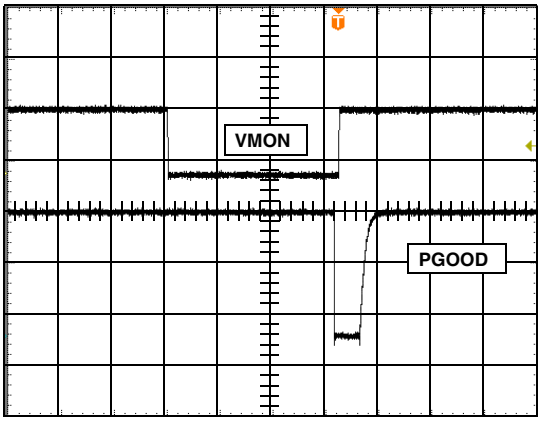
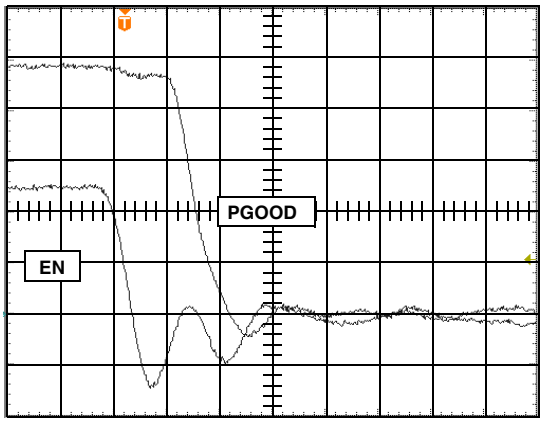


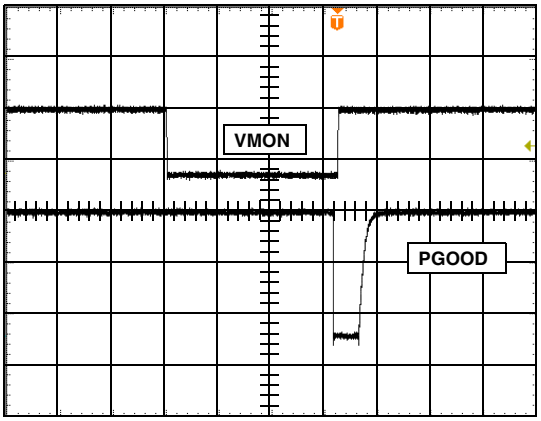
FIGURE 7. VMON LOW to PGOOD

Typical Performance Curves (Continued)



EN = 1V/DIV
PG = 1V/DIV
10nS/DIV

FIGURE 8. EN LOW to PGOOD



PGOOD = 2V/DIV
VMON = 1V/DIV
10µs/DIV

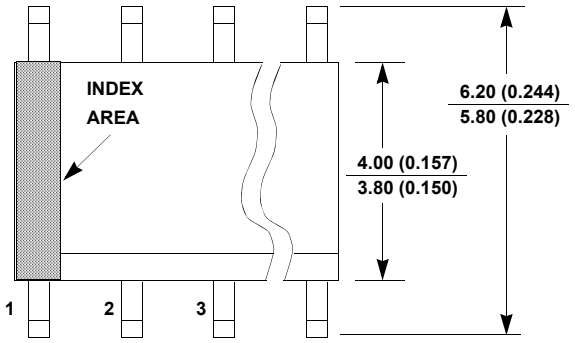
FIGURE 9. VMON LOW to PGOOD

Package Outline Drawing

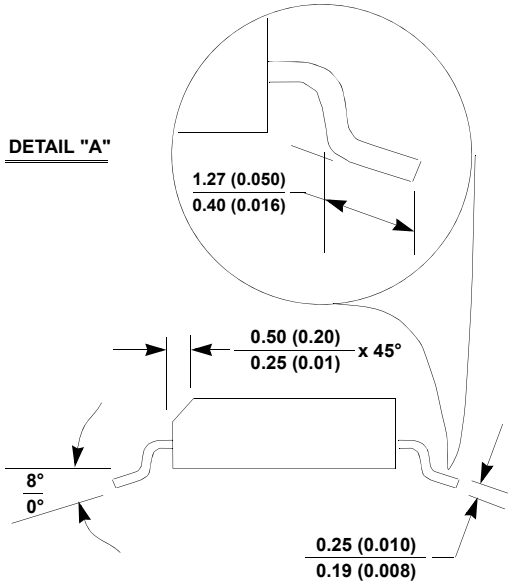
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

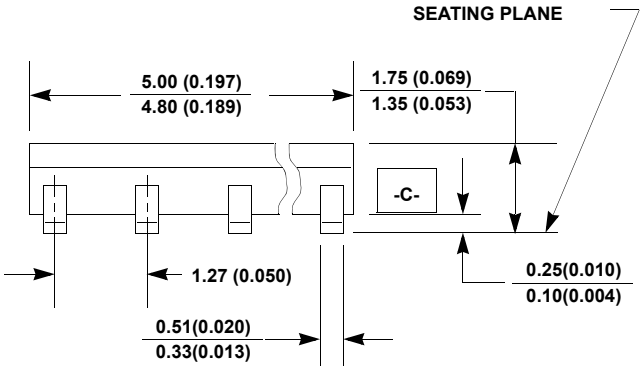
Rev 2, 11/10



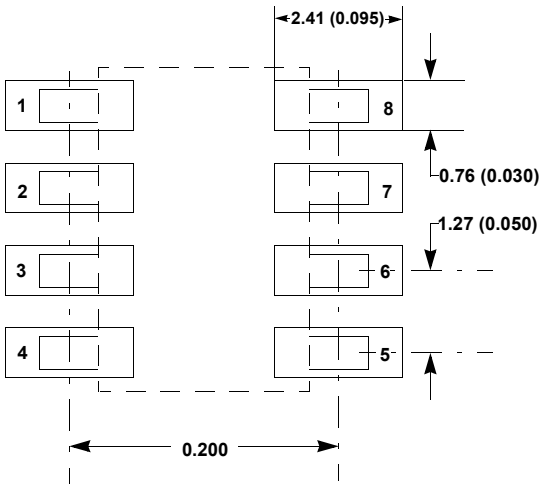
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.