Data Sheet | May 30, 2006 | FN8125.1

CPU Supervisor

FEATURES

- **200ms power-on reset delay**
- **Low V_{CC} detection and reset assertion**
  - **—Five standard reset threshold voltages**
  - **—Adjust low V_{CC} reset threshold voltage using special programming sequence**
  - **—Reset signal valid to V_{CC} = 1V**
- **Selectable nonvolatile watchdog timer**
  - **—0.2, 0.6, 1.4 seconds**
  - **—Off selection**
  - **—Select settings through software**
- **Long battery life with low power consumption**
  - **—<50µA max standby current, watchdog on**
  - **—<1µA max standby current, watchdog off**
- **2.7V to 5.5V operation**
- **SPI mode 0 interface**
- **Built-in inadvertent write protection**
  - **—Power-up/power-down protection circuitry**
  - **—Watchdog change latch**
- **High reliability**
- **Available packages**
  - **—8 Ld TSSOP**
  - **—8 Ld SOIC**
  - **—8 Ld PDIP**
- **Pb-free plus anneal available (RoHS compliant)**

DESCRIPTION

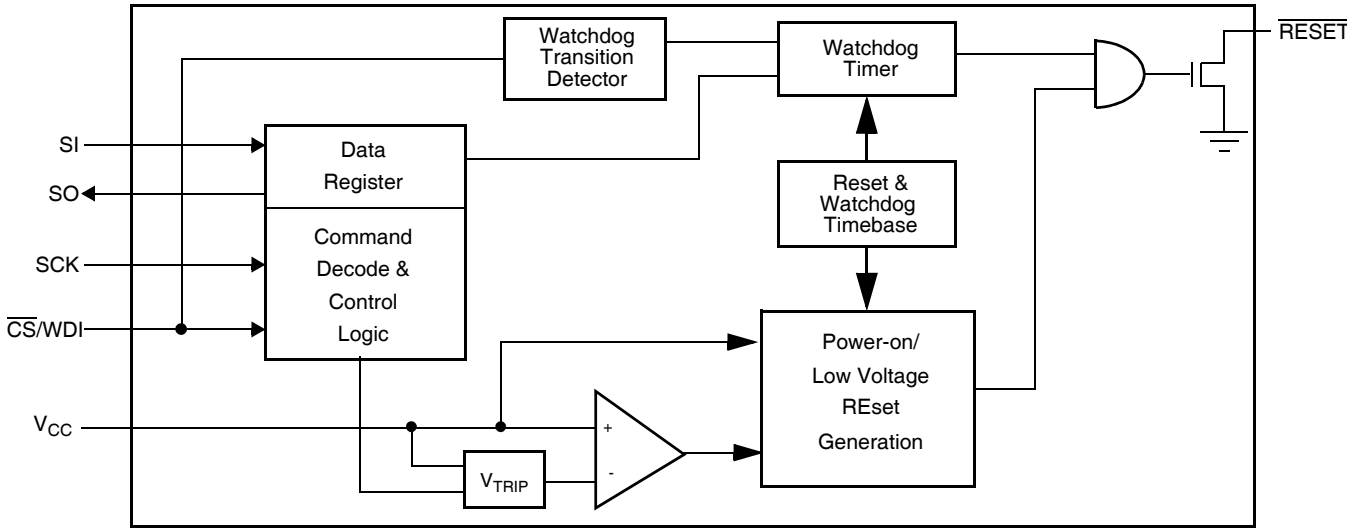
This device combines three popular functions, Power-on Reset, Watchdog Timer, and Supply Voltage Supervision in one package. This combination lowers system cost, reduces board space requirements, and increases reliability.

The watchdog timer provides an independent protection mechanism for microcontrollers. During a system failure, the device will respond with a $\overline{RESET}$ signal after a selectable time out interval. The user selects the interval from three preset values. Once selected, the interval does not change, even after cycling the power.

The user's system is protected from low voltage conditions by the device's low V_{CC} detection circuitry. When V_{CC} falls below the minimum V_{CC} trip point, the system is reset. $\overline{RESET}$ is asserted until V_{CC} returns to proper operating levels and stabilizes. Five industry standard V_{TRIP} thresholds are available, however, Intersil's unique circuits allow the threshold to be reprogrammed to meet custom requirements or to fine-tune the threshold for applications requiring higher precision.

The device utilizes Intersil's proprietary Direct Write™ cell for the watchdog timer control bits and the V_{TRIP} storage element, providing a minimum endurance of 100,000 write cycles and a minimum data retention of 100 years.

BLOCK DIAGRAM



Ordering Information

PART NUMBER	PART MARKING	V_{CC} RANGE (V)	V_{TRIP} RANGE	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
X5001P-2.7	X5001P F	2.7 to 5.5	2.55 to 2.7	0 to 70	8 Ld PDIP	MDP0031
X5001PZ-2.7 (Note)	X5001P ZF			0 to 70	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X5001PI-2.7	X5001P G			-40 to 85	8 Ld PDIP	MDP0031
X5001PIZ-2.7 (Note)	X5001P ZG			-40 to 85	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X5001S8-2.7	X5001 F			0 to 70	8 Ld SOIC (150 mil)	MDP0027
X5001S8Z-2.7 (Note)	X5001 ZF			0 to 70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X5001S8I-2.7	X5001 G			-40 to 85	8 Ld SOIC (150 mil)	MDP0027
X5001S8IZ-2.7 (Note)	X5001 ZG			-40 to 85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X5001V8-2.7	501 F			0 to 70	8 Ld TSSOP (4.4mm)	M8.173
X5001V8Z-2.7 (Note)	5001 FZ			0 to 70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X5001V8I-2.7	501 G			-40 to 85	8 Ld TSSOP (4.4mm)	M8.173
X5001V8IZ-2.7 (Note)	5001 GZ			-40 to 85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X5001P-2.7A	X5001P AN		2.85 to 3.0	0 to 70	8 Ld PDIP	MDP0031
X5001PZ-2.7A (Note)	X5001P ZAN			0 to 70	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X5001PI-2.7A	X5001P AP			-40 to 85	8 Ld PDIP	MDP0031
X5001PIZ-2.7A (Note)	X5001P ZAP			-40 to 85	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X5001S8-2.7A	X5001 AN			0 to 70	8 Ld SOIC (150 mil)	MDP0027
X5001S8Z-2.7A (Note)	X5001 ZAN			0 to 70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X5001S8I-2.7A	X5001 AP			-40 to 85	8 Ld SOIC (150 mil)	MDP0027
X5001S8IZ-2.7A (Note)	X5001 ZAP			-40 to 85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X5001V8-2.7A	501 AN			0 to 70	8 Ld TSSOP (4.4mm)	M8.173
X5001V8Z-2.7A (Note)	5001 ANZ			0 to 70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X5001V8I-2.7A	501 AP			-40 to 85	8 Ld TSSOP (4.4mm)	M8.173
X5001V8IZ-2.7A (Note)	5001 APZ			-40 to 85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X5001PI	X5001P I	4.5 to 5.5	4.25 to 4.5	-40 to 85	8 Ld PDIP	MDP0031
X5001PIZ (Note)	X5001P ZI			-40 to 85	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X5001S8	X5001			0 to 70	8 Ld SOIC (150 mil)	MDP0027
X5001S8Z (Note)	X5001 Z			0 to 70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X5001S8I	X5001 I			-40 to 85	8 Ld SOIC (150 mil)	MDP0027
X5001S8IZ (Note)	X5001 ZI			-40 to 85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027

Ordering Information (Continued)

PART NUMBER	PART MARKING	V_{CC} RANGE (V)	V_{TRIP} RANGE	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
X5001V8	501	4.5 to 5.5	4.25 to 4.5	0 to 70	8 Ld TSSOP (4.4mm)	M8.173
X5001V8Z (Note)	5001 Z			0 to 70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X5001V8I	501 I			-40 to 85	8 Ld TSSOP (4.4mm)	M8.173
X5001V8IZ (Note)	5001 IZ			-40 to 85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X5001PI-4.5A	X5001P AM	4.5 to 5.5	4.5 to 4.75	-40 to 85	8 Ld PDIP	MDP0031
X5001PIZ-4.5A (Note)	X5001P ZAM			-40 to 85	8 Ld PDIP (300 mil) (Pb-free)	MDP0031
X5001S8-4.5A	X5001 AL			0 to 70	8 Ld SOIC (150 mil)	MDP0027
X5001S8Z-4.5A (Note)	X5001 ZAL			0 to 70	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X5001S8I-4.5A	X5001 AM			-40 to 85	8 Ld SOIC (150 mil)	MDP0027
X5001S8IZ-4.5A (Note)	X5001 ZAM			-40 to 85	8 Ld SOIC (150 mil) (Pb-free)	MDP0027
X5001V8-4.5A	501 AL			0 to 70	8 Ld TSSOP (4.4mm)	M8.173
X5001V8Z-4.5A (Note)	5001 ALZ			0 to 70	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173
X5001V8I-4.5A	501 AM			-40 to 85	8 Ld TSSOP (4.4mm)	M8.173
X5001V8IZ-4.5A (Note)	5001 AMZ			-40 to 85	8 Ld TSSOP (4.4mm) (Pb-free)	M8.173

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

PIN CONFIGURATION

PIN DESCRIPTION

Pin (SOIC/PDIP)	Pin TSSOP	Name	Function
1	1	$\overline{CS}/\overline{WDI}$	**Chip Select Input.** $\overline{CS}$ HIGH, deselects the device and the SO output pin is at a high impedance state. Unless a nonvolatile write cycle is underway, the device will be in the standby power mode. $\overline{CS}$ LOW enables the device, placing it in the active power mode. Prior to the start of any operation after power-up, a HIGH to LOW transition on $\overline{CS}$ is required. **Watchdog Input.** A HIGH to LOW transition on the WDI pin restarts the Watchdog timer. The absence of a HIGH to LOW transition within the watchdog time out period results in $\overline{RESET}$/RESET going active.
2	2	SO	**Serial Output.** SO is a push/pull serial data output pin. A read cycle shifts data out on this pin. The falling edge of the serial clock (SCK) clocks the data out.
5	8	SI	**Serial Input.** SI is a serial data input pin. Input all opcodes, byte addresses, and memory data on this pin. The rising edge of the serial clock (SCK) latches the input data. Send all opcodes (Table 1), addresses and data MSB first.
6	9	SCK	**Serial Clock.** The Serial Clock controls the serial bus timing for data input and output. The rising edge of SCK latches in the opcode, address, or watchdog bits present on the SI pin. The falling edge of SCK changes the data output on the SO pin.
3	6	V_{PE}	**V_{TRIP} Program Enable.** When V_{PE} is LOW, the V_{TRIP} point is fixed at the last valid programmed level. To readjust the V_{TRIP} level, requires that the V_{PE} pin be pulled to a high voltage (15-18V).
4	7	V_{SS}	**Ground**
8	14	V_{CC}	**Supply Voltage**
7	13	$\overline{RESET}$	**Reset Output**. $\overline{RESET}$ is an active LOW, open drain output which goes active whenever V_{CC} falls below the minimum V_{CC} sense level. It will remain active until V_{CC} rises above the minimum V_{CC} sense level for 200ms. $\overline{RESET}$ goes active if the watchdog timer is enabled and $\overline{CS}$/WDI remains either HIGH or LOW longer than the selectable watchdog time out period. A falling edge of $\overline{CS}$/WDI will reset the watchdog timer. $\overline{RESET}$ goes active on power-up at 1V and remains active for 200ms after the power supply stabilizes.
	3-5,10-12	NC	No internal connections

PRINCIPLES OF OPERATION

Power-on Reset

Application of power to the X5001 activates a power-on reset circuit. This circuit goes active at 1V and pulls the $\overline{RESET}$/RESET pin active. This signal prevents the system microprocessor from starting to operate with insufficient voltage or prior to stabilization of the oscillator. When V_{CC} exceeds the device V_{TRIP} value for 200ms (nominal) the circuit releases $\overline{RESET}$, allowing the processor to begin executing code.

Low Voltage Monitoring

During operation, the X5001 monitors the V_{CC} level and asserts $\overline{RESET}$ if supply voltage falls below a preset minimum V_{TRIP}. The $\overline{RESET}$ signal prevents the microprocessor from operating in a power fail or brownout condition. The $\overline{RESET}$ signal remains active until the voltage drops below 1V. It also remains active until V_{CC} returns and exceeds V_{TRIP} for 200ms.

Watchdog Timer

The watchdog timer circuit monitors the microprocessor activity by monitoring the WDI input. The microprocessor must toggle the $\overline{CS}$/WDI pin periodically to prevent a $\overline{RESET}$ signal. The $\overline{CS}$/WDI pin must be toggled from HIGH to LOW prior to the expiration of the watchdog time out period. The state of two nonvolatile control bits in the watchdog register determine the watchdog timer period.

Vcc Threshold Reset Procedure

The X5001 is shipped with a standard V_{CC} threshold (V_{TRIP}) voltage. This value will not change over normal operating and storage conditions. However, in applications where the standard V_{TRIP} is not exactly right, or if higher precision is needed in the V_{TRIP} value, the X5001 threshold may be adjusted. The procedure is described in the following sections, and requires the application of a high voltage control signal.

Setting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a higher voltage value. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} is 4.6V, this procedure will directly make the change. If the new setting is to be lower than the current setting, then it is necessary to reset the trip point before setting the new value.

To set the new V_{TRIP} voltage, apply the desired V_{TRIP} threshold voltage to the V_{CC} pin and tie the W_{PE} pin to the programming voltage V_P. Then a V_{TRIP} programming command sequence is sent to the device over the SPI interface. This V_{TRIP} programming sequence consists of pulling $\overline{CS}$ LOW, then clocking in data 03h, 00h and 01h. This is followed by bringing $\overline{CS}$ HIGH then LOW and clocking in data 02h, 00h, and 01h (in order) and bringing $\overline{CS}$ HIGH. This initiates the V_{TRIP} programming sequence. V_P is brought LOW to end the operation.

Resetting the V_{TRIP} Voltage

This procedure is used to set the V_{TRIP} to a “native” voltage level. For example, if the current V_{TRIP} is 4.4V and the new V_{TRIP} must be 4.0V, then the V_{TRIP} must be reset. When V_{TRIP} is reset, the new V_{TRIP} is something less than 1.7V. This procedure must be used to set the voltage to a lower value.

To reset the V_{TRIP} voltage, apply greater than 3V to the V_{CC} pin and tie the W_{PE} pin to the programming voltage V_P. Then a V_{TRIP} command sequence is sent to the device over the SPI interface. This V_{TRIP} programming sequence consists of pulling $\overline{CS}$ LOW, then clocking in data 03h, 00h and 01h. This is followed by bringing $\overline{CS}$ HIGH then LOW and clocking in data 02h, 00h, and 03h (in order) and bringing $\overline{CS}$ HIGH. This initiates the V_{TRIP} programming sequence. V_P is brought LOW to end the operation.

Figure 1. Sample V_{TRIP} Reset Circuit

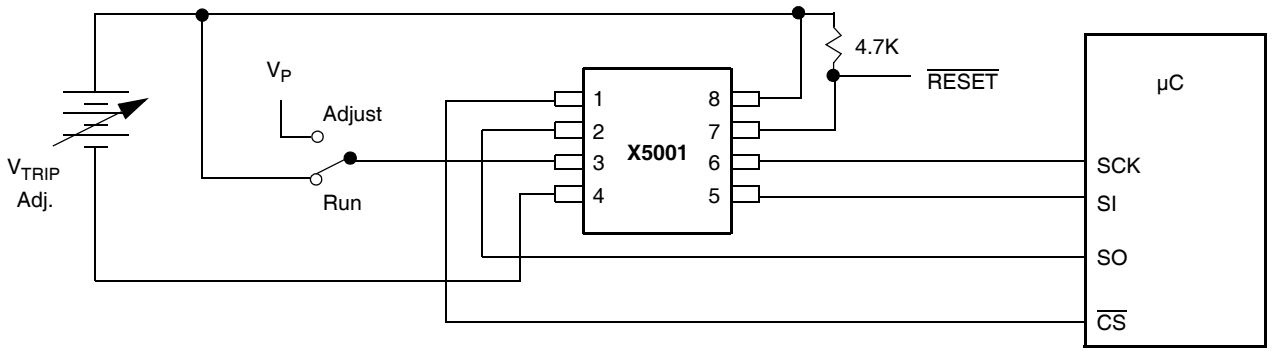


Figure 2. Set V_{TRIP} Level Sequence (V_{CC} = desired V_{TRIP} value)

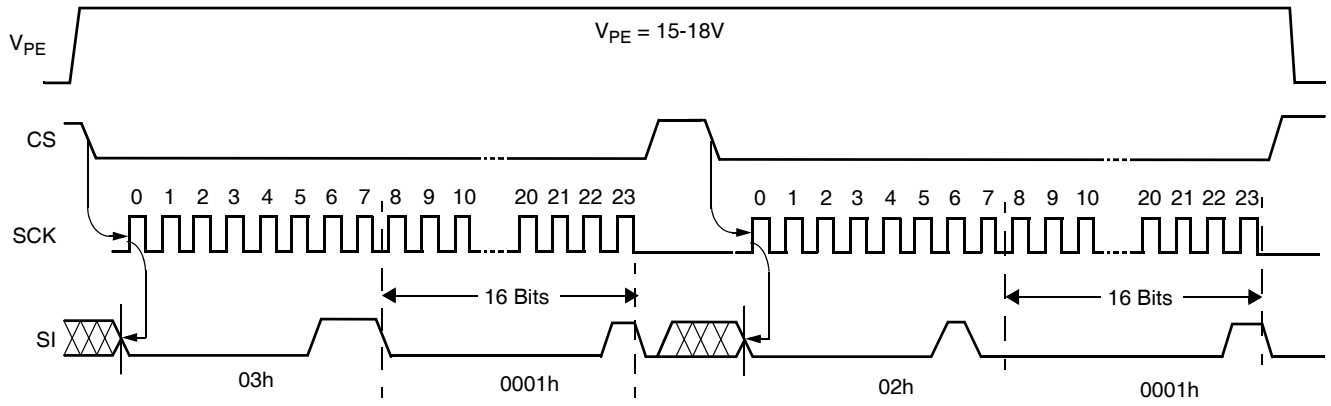


Figure 3. Reset V_{TRIP} Level Sequence (V_{CC} > 3V)

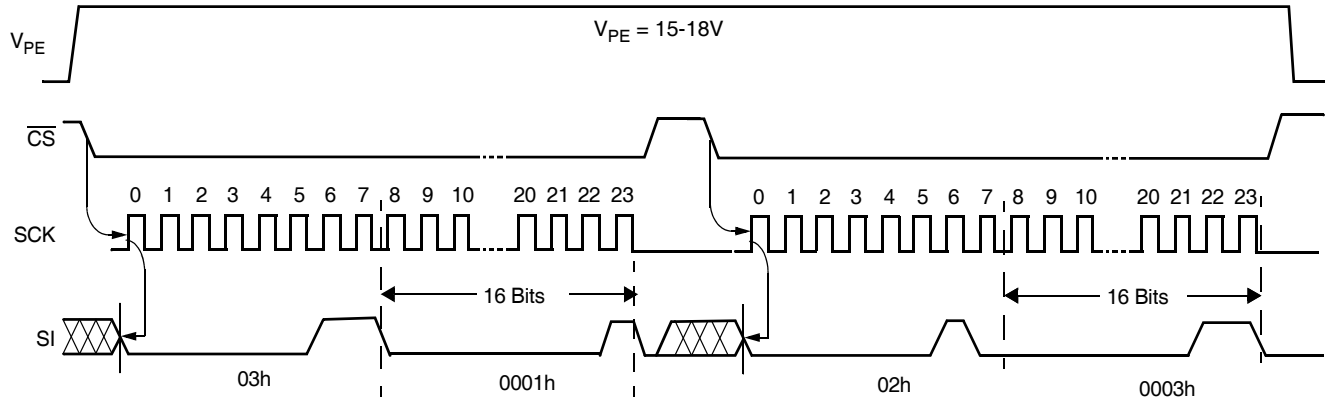
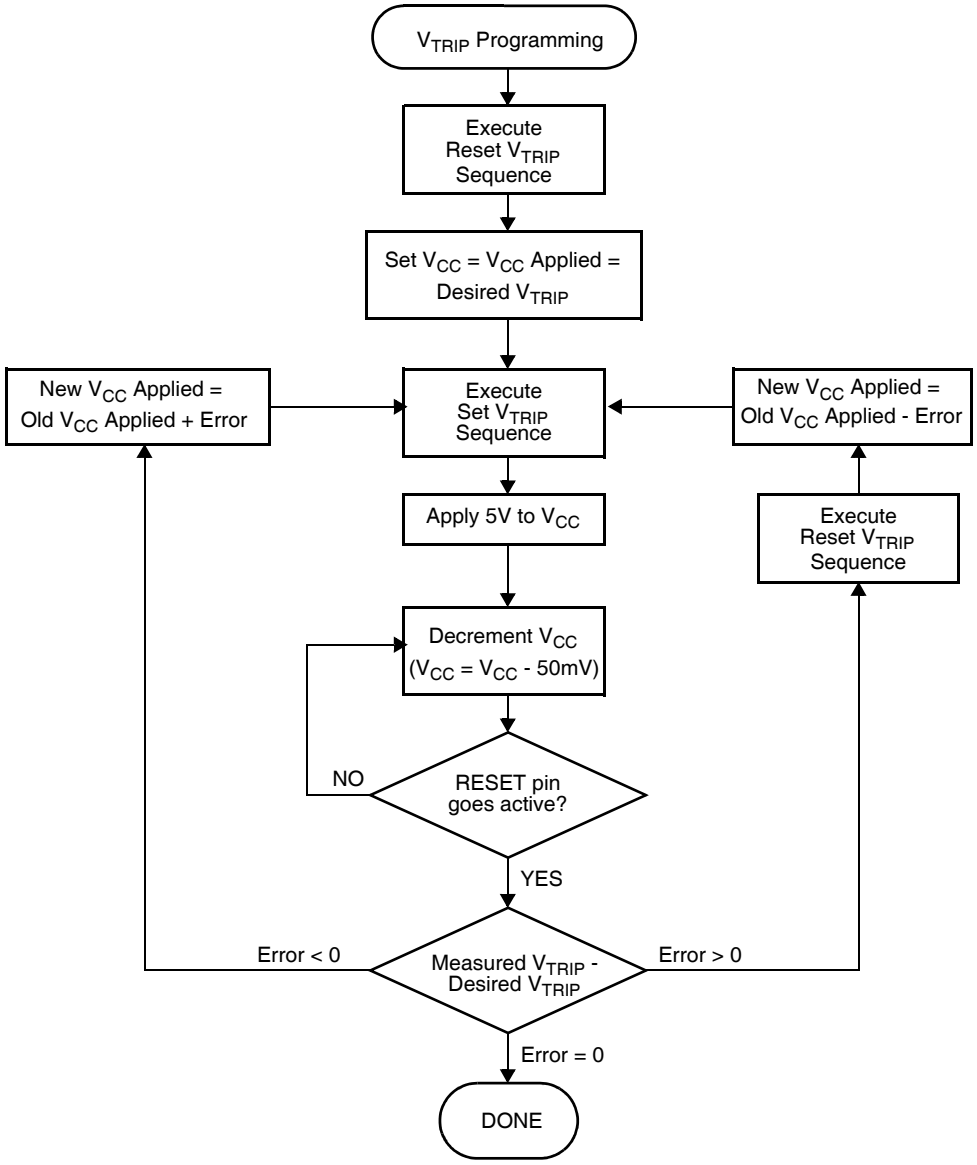


Figure 4. V_{TRIP} Programming Sequence



SPI INTERFACE

The device is designed to interface directly with the synchronous Serial Peripheral Interface (SPI) of many popular microcontroller families.

The device monitors the $\overline{CS}$/WDI line and asserts $\overline{RESET}$ output if there is no activity within user selectable timeout period. The device also monitors the V_{CC} supply and asserts the $\overline{RESET}$ if V_{CC} falls below a preset minimum (V_{TRIP}). The device contains an 8-bit watchdog timer register to control the watchdog time out period. The current settings are accessed via the SI and SO pins.

All instructions (Table 1) and data are transferred MSB first. Data input on the SI line is latched on the first rising edge of SCK after $\overline{CS}$ goes LOW. Data is output on the SO line by the falling edge of SCK. SCK is static, allowing the user to stop the clock and then start it again to resume operations where left off.

Watchdog Timer Register

7	6	5	4	3	2	1	0
0	0	0	WD_1	WD_0	0	0	0

Watchdog Timer Control Bits

The watchdog timer control bits, WD_0 and WD_1, select the watchdog time out period. These nonvolatile bits are programmed with the set watchdog timer (SWDT) instruction.

Watchdog Control Bits		Watchdog Time Out (Typical)
WD1	WD0	
0	0	1.4 seconds
0	1	600 milliseconds
1	0	200 milliseconds
1	1	disabled

Write Watchdog Register Operation

Changing the watchdog timer register is a two step process. First, the change must be enabled by setting the watchdog change latch (see below). This instruction is followed by the set watchdog timer (SWDT) instruction, which includes the data to be written (Figure 5). Data bits 3 and 4 contain the watchdog settings and data bits 0, 1, 2, 5, 6 and 7 must be “0”.

Watchdog Change Latch

The watchdog change latch must be SET before a Write watchdog timer operation is initiated. The Enable Watchdog Change (EWDC) instruction will set the latch and the Disable Watchdog Change (DWDC) instruction will reset the latch (Figure 6). This latch is automatically reset upon a power-up condition and after the completion of a valid nonvolatile write cycle.

Read Watchdog Timer Register Operation

If there is not a nonvolatile write in progress, the read watchdog timer instruction returns the setting of the watchdog timer control bits. The other bits are reserved and will return’0’ when read. See Figure 3.

If a nonvolatile write is in progress, the read watchdog timer register Instruction returns a HIGH on SO. When the nonvolatile write cycle is completed, a separate read watchdog timer instruction should be used to determine the current status of the watchdog control bits.

$\overline{\text{RESET}}$ Operation

The $\overline{\text{RESET}}$ (X5001) output is designed to go LOW whenever V_{CC} has dropped below the minimum trip point and/or the watchdog timer has reached its programmable time out limit.

The $\overline{\text{RESET}}$ output is an open drain output and requires a pull-up resistor.

Operational Notes

The device powers-up in the following state:

– The device is in the low power standby state.
– A HIGH to LOW transition on $\overline{\text{CS}}$ is required to enter an active state and receive an instruction.
– SO pin is high impedance.
– The watchdog change latch is reset.
– The $\overline{\text{RESET}}$ signal is active for t_{PURST}.

Data Protection

The following circuitry has been included to prevent inadvertent writes:

– A EWDC instruction must be issued to enable a change to the watchdog timeout setting.
– $\overline{\text{CS}}$ must come HIGH at the proper clock count in order to implement the requested changes to the watchdog timeout setting.

Table 1. Instruction Set Definition

Instruction Format	Instruction Name and Operation
0000 0110	**EWDC: Enable Watchdog Change Operation**
0000 0100	**DWDC: Disable Watchdog Change Operation**
0000 0001	**SWDT: Set Watchdog Timer control bits:** Instruction followed by contents of register: 000(WD_1) (WD_0)000 See Watchdog Timer Settings and Figure 7.
0000 0101	**RWDT: Read Watchdog Timer Control Bits**

Note: Instructions are shown with MSB in leftmost position. Instructions are transferred MSB first.

Figure 5. Read Watchdog Timer Setting

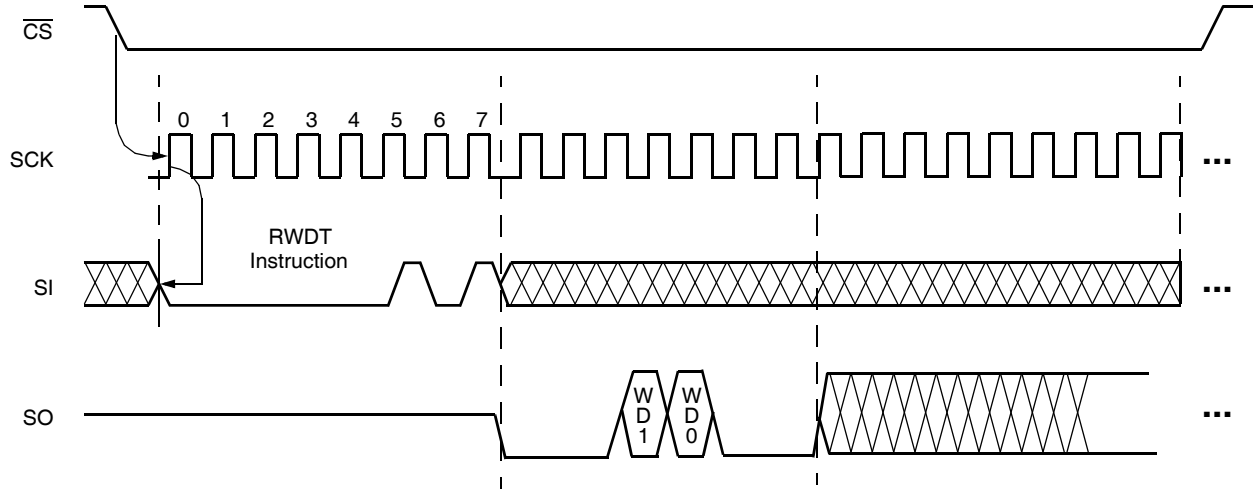


Figure 6. Enable Watchdog Change/Disable Watchdog Change Sequence

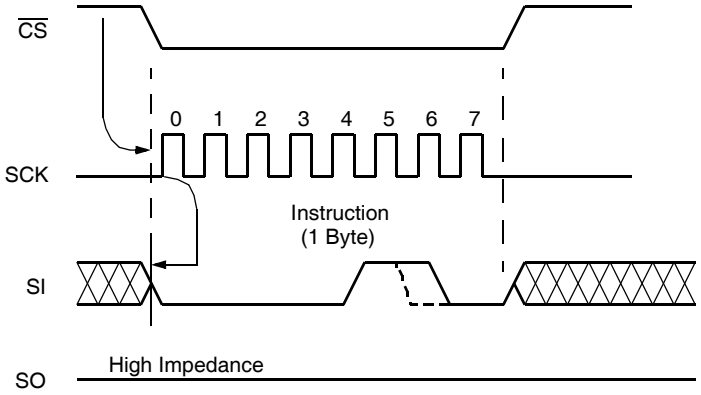


Figure 7. Write Watchdog Timer Sequence

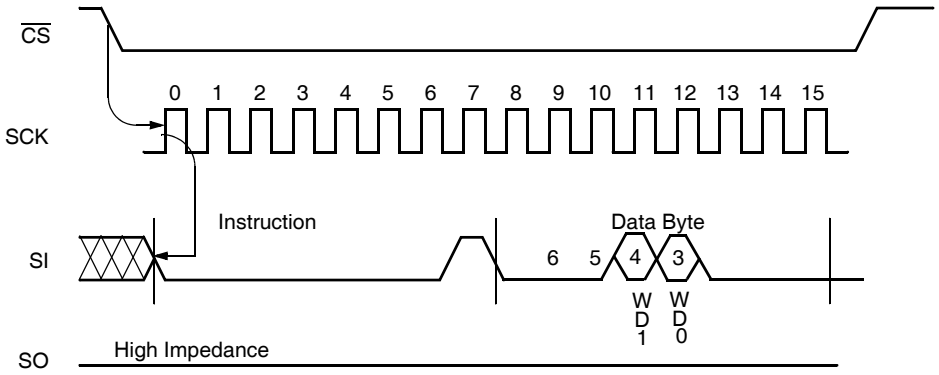


Figure 8. Read Nonvolatile Status (Option 1) (Used to determine end of Watchdog Timer store operation)

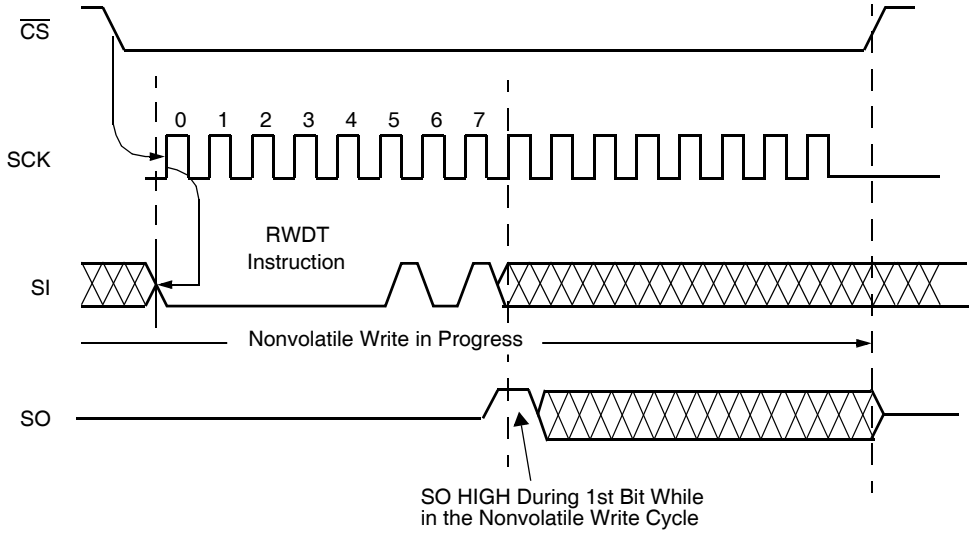
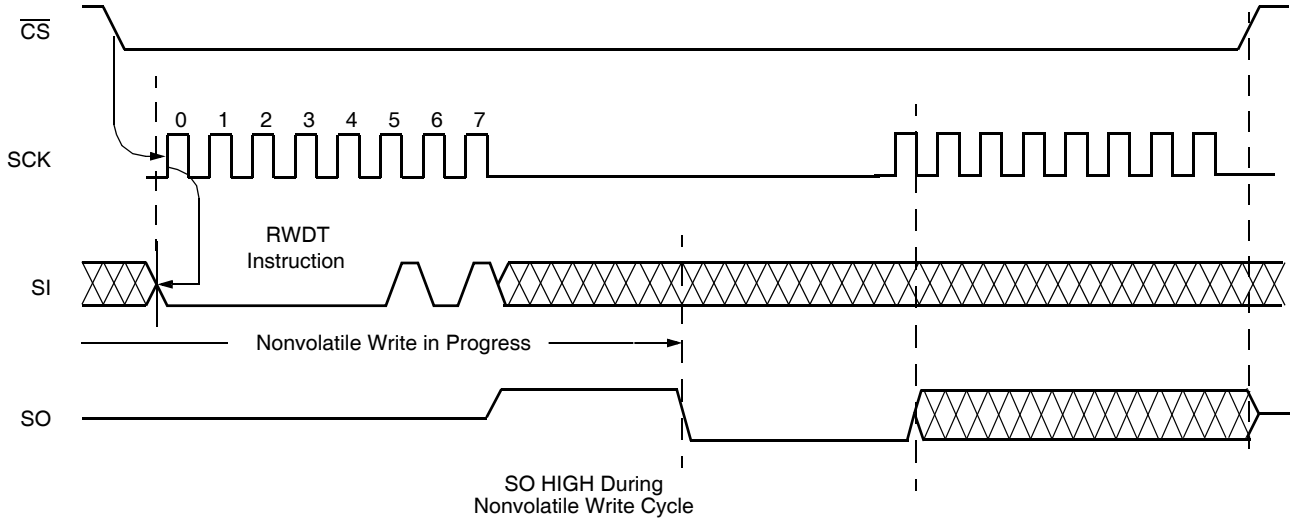


Figure 9. Read Nonvolatile Status (Option 2) (Used to determine end of Watchdog Timer store operation)



ABSOLUTE MAXIMUM RATINGS

Temperature under bias ..... -65°C to +135°C
Storage temperature ..... -65°C to +150°C
Voltage on any pin with
respect to V_{SS} ..... -1.0V to +7V
D.C. output current 5mA
Lead temperature (soldering, 10s) ..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; the functional operation of the device (at these or any other conditions above those listed in the operational sections of this datasheet) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Temperature	Min.	Max.
Commercial	0°C	+70°C

Voltage Option	Supply Voltage Limits
-1.8	1.8V to 3.6V
-2.7 or -2.7A	2.7V to 5.5V
-4.5 or -4.5A	4.5V to 5.5V

Note: PT= Package, Temperature

D.C. OPERATING CHARACTERISTICS (Over the recommended operating conditions unless otherwise specified)

Symbol	Parameter	Limits			Unit	Test Conditions
		Min.	Typ	Max.		
I_{CC1}	V_{CC} write current (Active)			5	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 5MHz, SO = Open
I_{CC2}	V_{CC} read current (Active)			0.4	mA	SCK = V_{CC} x 0.1/V_{CC} x 0.9 @ 5MHz, SO = Open
I_{SB1}	V_{CC} standby current WDT=OFF			1	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V
I_{SB2}	V_{CC} standby current WDT=ON			50	µA	$\overline{CS}$ = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 5.5V
I_{SB3}	V_{CC} standby current WDT=ON			20	µA	CS = V_{CC}, V_{IN} = V_{SS} or V_{CC}, V_{CC} = 3.6V
I_{LI}	Input leakage current		0.1	10	µA	V_{IN} = V_{SS} to V_{CC}
I_{LO}	Output leakage current		0.1	10	µA	V_{OUT} = V_{SS} to V_{CC}
V_{IL}(1)	Input LOW voltage	-0.5		V_{CC} x 0.3	V	
V_{IH}(1)	Input HIGH voltage	V_{CC} x 0.7		V_{CC} + 0.5	V	
V_{OL1}	Output LOW voltage			0.4	V	V_{CC} > 3.3V, I_{OL} = 2.1mA
V_{OL2}	Output LOW voltage			0.4	V	2V < V_{CC} < 3.3V, I_{OL} = 1mA
V_{OL3}	Output LOW voltage			0.4	V	$V_{CC} \leq$ 2V, I_{OL} = 0.5mA
V_{OH1}	Output HIGH voltage	V_{CC}-0.8			V	V_{CC} > 3.3V, I_{OH} = -1.0mA
V_{OH2}	Output HIGH voltage	V_{CC}-0.4			V	2V < $V_{CC} \leq$ 3.3V, I_{OH} = -0.4mA
V_{OH3}	Output HIGH voltage	V_{CC}-0.2			V	$V_{CC} \leq$ 2V, I_{OH} = -0.25mA
V_{OLRS}	Reset output LOW voltage			0.4	V	I_{OL} = 1mA

POWER-UP TIMING

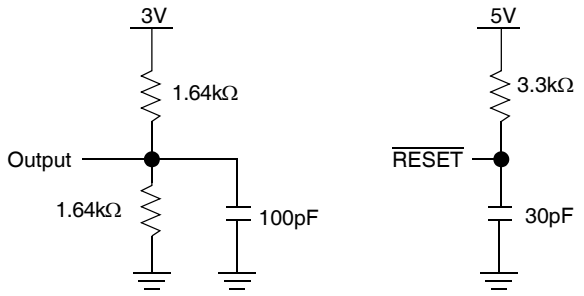
Symbol	Parameter	Min.	Max.	Unit
t_{PUR}(2)	Power-up to read operation		1	ms
t_{PUW}(2)	Power-up to write operation		5	ms

CAPACITANCE (T_A = +25°C, f = 1MHz, V_{CC} = 5V)

Symbol	Test	Max.	Unit	Conditions
C_{OUT}(2)	Output capacitance (SO, $\overline{RESET}$)	8	pF	V_{OUT} = 0V
C_{IN}(2)	Input capacitance (SCK, SI, $\overline{CS}$)	6	pF	V_{IN} = 0V

Notes: (1) V_{IL} min. and V_{IH} max. are for reference only and are not tested.
(2) This parameter is periodically sampled and not 100% tested.

EQUIVALENT A.C. LOAD CIRCUIT



A.C. TEST CONDITIONS

Input pulse levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x0.5

A.C. CHARACTERISTICS (Over recommended operating conditions, unless otherwise specified)

Data Input Timing

SymboL	Parameter	1.8V-3.6V		2.7V-5.5V		Unit
		Min.	Max.	Min.	Max.	
f_{SCK}	Clock frequency	0	1	0	2	MHz
t_{CYC}	Cycle time	1000		500		ns
t_{LEAD}	$\overline{CS}$ lead time	400		200		ns
t_{LAG}	$\overline{CS}$ lag time	400		200		ns
t_{WH}	Clock HIGH time	400		200		ns
t_{WL}	Clock LOW time	400		200		ns
t_{SU}	Data setup time	100		50		ns
t_H	Data hold time	100		50		ns
t_{RI}(3)	Input rise time		2		2	µs
t_{FI}(3)	Input fall time		2		2	µs
t_{CS}	$\overline{CS}$ deselect time	250		150		ns
t_{WC}(4)	Write cycle time		10		10	ms

Data Output Timing

Symbol	Parameter	1.8V-3.6V		2.7V-5.5V		Unit
		Min.	Max.	Min.	Max.	
f_{SCK}	Clock frequency	0	1	0	2	MHz
t_{DIS}	Output disable time		400		200	ns
t_V	Output valid from clock low		400		200	ns
t_{HO}	Output hold time	0		0		ns
t_{RO}(3)	Output rise time		300		150	ns
t_{FO}(3)	Output fall time		300		150	ns

Notes: (3) This parameter is periodically sampled and not 100% tested.
(4) t_{WC} is the time from the rising edge of $\overline{CS}$ after a valid write sequence has been sent to the end of the self-timed internal nonvolatile write cycle.

Figure 10. Data Output Timing

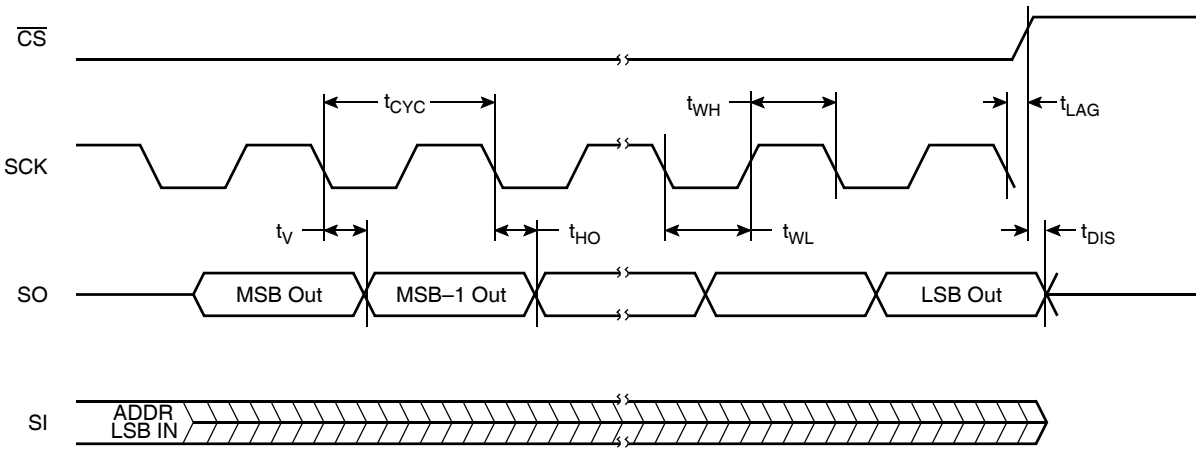
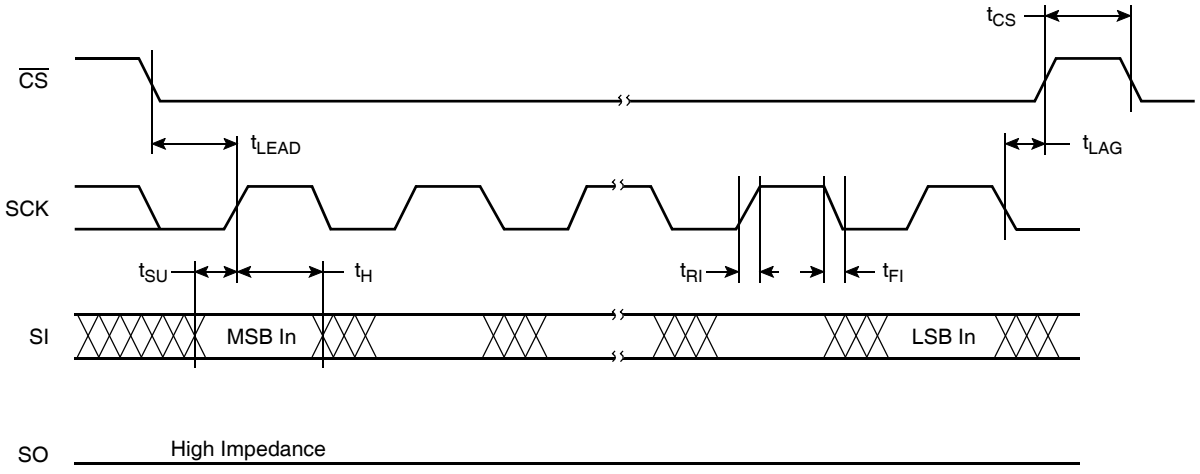


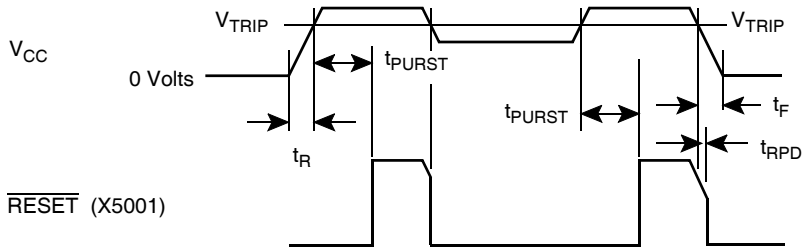
Figure 11. Data Input Timing



SYMBOL TABLE

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Figure 12. Power-Up and Power-Down Timing

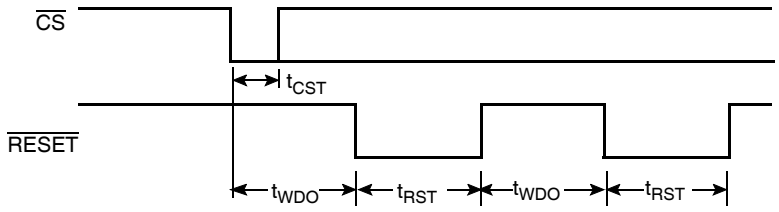


$\overline{RESET}$ Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{TRIP}	Reset trip point voltage, X5001PT-4.5A	4.50	4.63	4.75	V
	Reset trip point voltage, X5001PT-4.5	4.25	4.38	4.50	
	Reset trip point voltage, X5001PT-2.7A	2.85	2.92	3.00	
	Reset trip point voltage, X5001PT-2.7	2.55	2.63	2.70	
	Reset trip point voltage, X5001PT-1.8	1.70	1.75	1.80	
t_{PURST}	Power-up reset timeout	100	200	280	ms
t_{RPD}(5)	V_{CC} detect to reset/output			500	ns
t_F(5)	V_{CC} fall time	0.1			ns
t_R(5)	V_{CC} rise time	0.1			ns
V_{RVALID}	Reset valid V_{CC}	1			V

Note: (5) This parameter is periodically sampled and not 100% tested.
PT = Package, Temperature

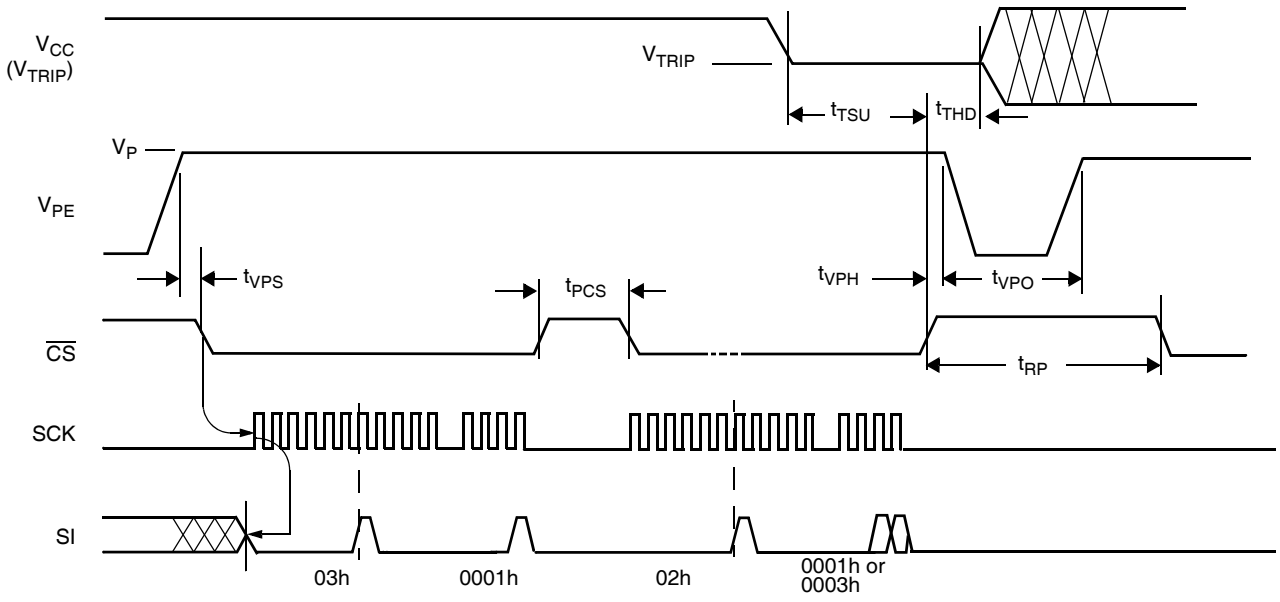
Figure 13. $\overline{CS}$ vs. $\overline{RESET}$ Timing



$\overline{RESET}$ Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Unit
t_{WDO}	Watchdog timeout period,				
	$WD_1 = 1$, $WD_0 = 0$	100	200	300	ms
	$WD_1 = 0$, $WD_0 = 1$	450	600	800	ms
	$WD_1 = 0$, $WD_0 = 0$	1	1.4	2	sec
t_{CST}	$\overline{CS}$ pulse width to reset the watchdog	400			ns
t_{RST}	Reset Timeout	100	200	300	ms

V_{TRIP} Programming Timing Diagram

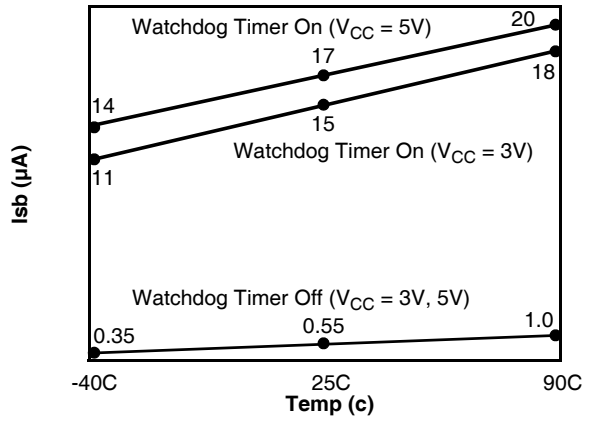


V_{TRIP} Programming Parameters

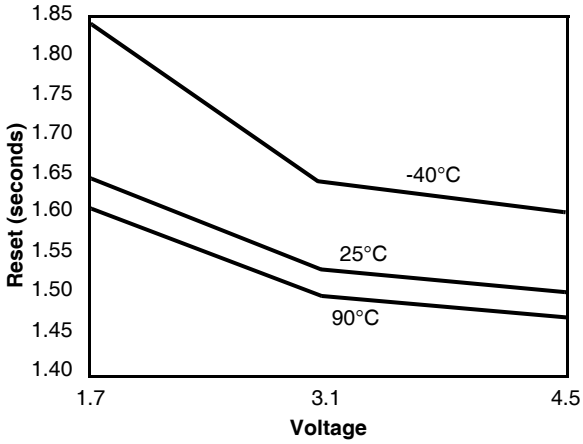
Parameter	Description	Min.	Max.	Unit
t_{VPS}	V_{TRIP} program enable voltage setup time	1		µs
t_{VPH}	V_{TRIP} program enable voltage hold time	1		µs
t_{PCS}	V_{TRIP} programming $\overline{CS}$ inactive time	1		µs
t_{TSU}	V_{TRIP} setup time	1		µs
t_{THD}	V_{TRIP} hold (stable) time	10		ms
t_{WC}	V_{TRIP} write cycle time		10	ms
t_{VPO}	V_{TRIP} program enable voltage Off time (between successive adjustments)	0		µs
t_{RP}	V_{TRIP} program recovery period (between successive adjustments)	10		ms
V_P	Programming voltage	15	18	V
V_{TRAN}	V_{TRIP} programmed voltage range	1.7	5.0	V
V_{ta1}	Initial V_{TRIP} program voltage accuracy (V_{CC} applied-V_{TRIP}) (programmed at 25°C)	-0.1	+0.4	V
V_{ta2}	Subsequent V_{TRIP} program voltage accuracy [(V_{CC} applied-V_{ta1})-V_{TRIP}. Programmed at 25°C.]	-25	+25	mV
V_{tr}	V_{TRIP} program voltage repeatability (Successive program operations. Programmed at 25°C.)	-25	+25	mV
V_{tv}	V_{TRIP} program variation after programming (0-75°C). (programmed at 25°C)	-25	+25	mV

V_{TRIP} programming parameters are periodically sampled and are not 100% tested.

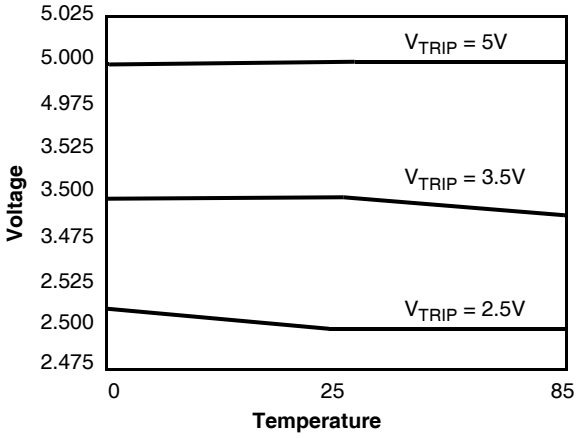
V_{CC} Supply Current vs. Temperature (I_{SB})



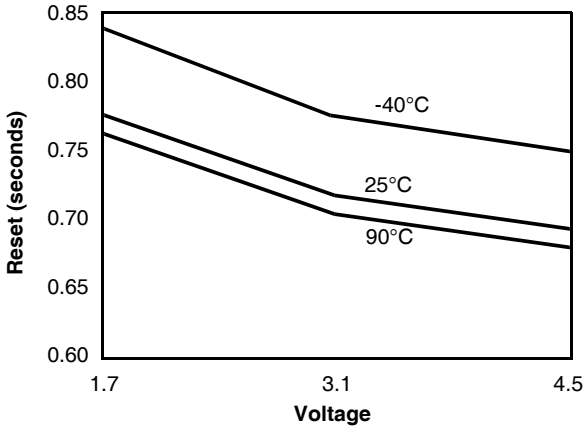
t_{WDO} vs. Voltage/Temperature (WD1, 0 = 1, 1)



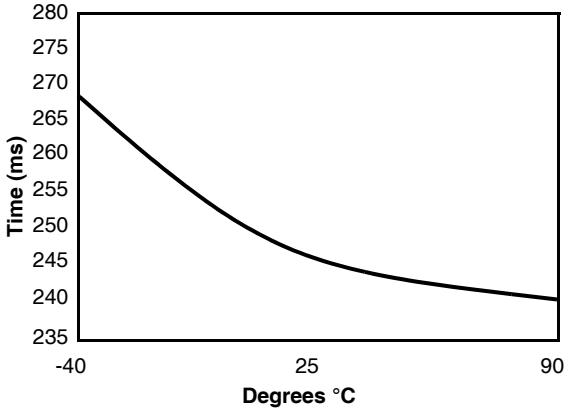
V_{TRIP} vs. Temperature (programmed at 25°C)



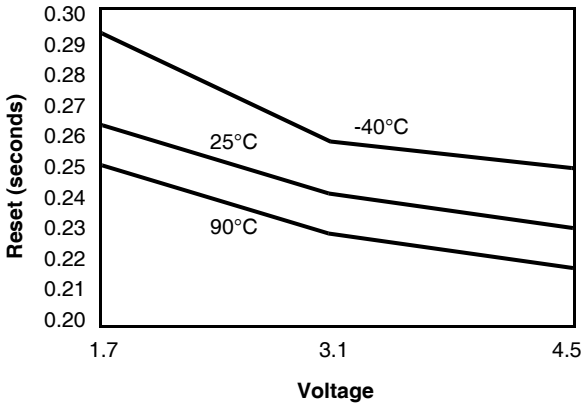
t_{WDO} vs. Voltage/Temperature (WD1, 0 = 1, 0)



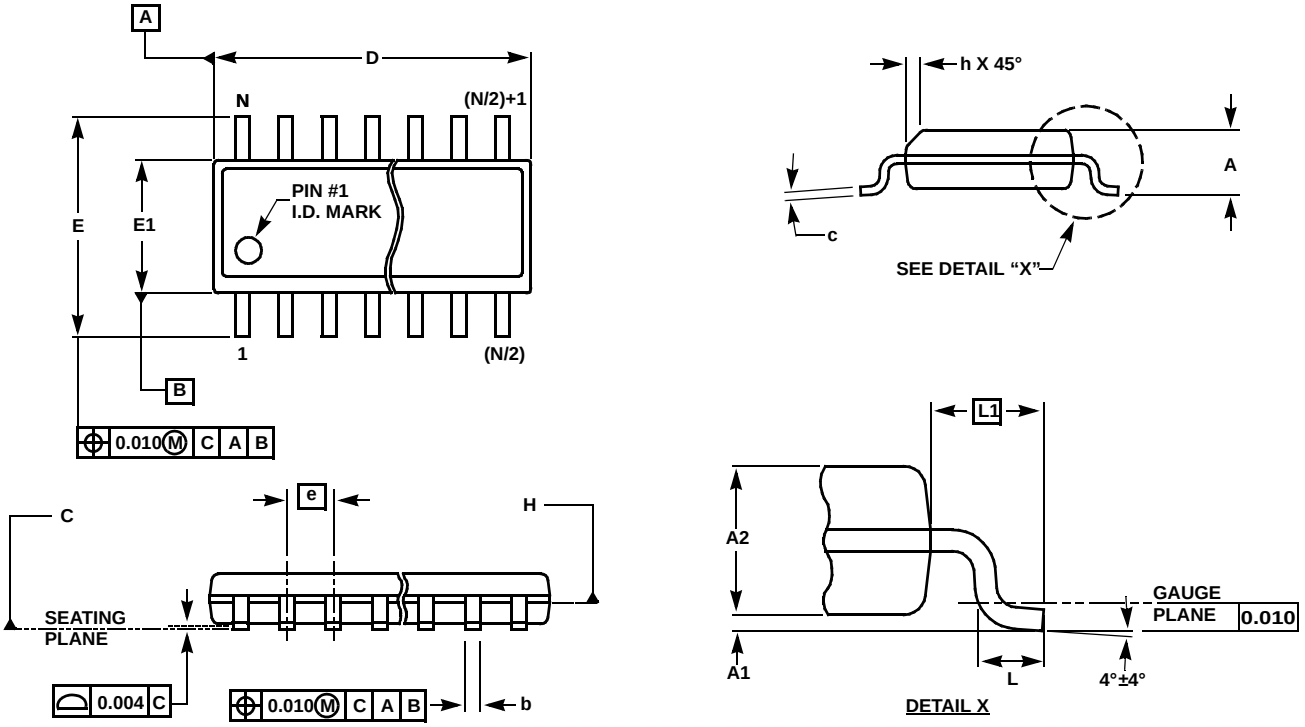
t_{PURST} vs. Temperature



t_{WDO} vs. Voltage/Temperature (WD1, 0 0 = 0, 1)



Small Outline Package Family (SO)



MDP0027

SMALL OUTLINE PACKAGE FAMILY (SO)

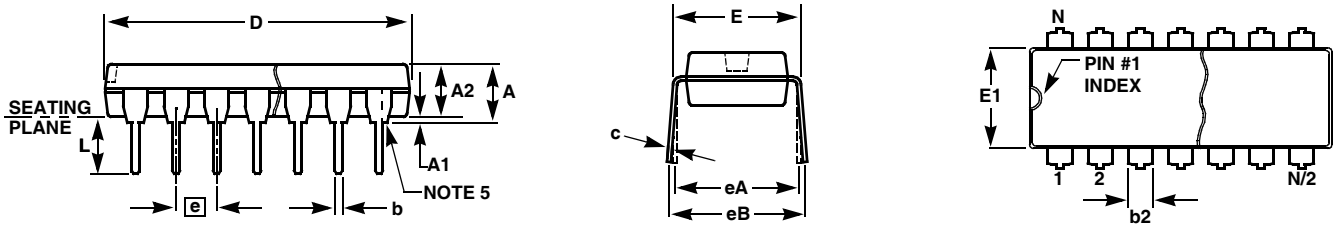
SYMBOL	SO-8	SO-14	SO16 (0.150")	SO16 (0.300") (SOL-16)	SO20 (SOL-20)	SO24 (SOL-24)	SO28 (SOL-28)	TOLERANCE	NOTES
A	0.068	0.068	0.068	0.104	0.104	0.104	0.104	MAX	-
A1	0.006	0.006	0.006	0.007	0.007	0.007	0.007	±0.003	-
A2	0.057	0.057	0.057	0.092	0.092	0.092	0.092	±0.002	-
b	0.017	0.017	0.017	0.017	0.017	0.017	0.017	±0.003	-
c	0.009	0.009	0.009	0.011	0.011	0.011	0.011	±0.001	-
D	0.193	0.341	0.390	0.406	0.504	0.606	0.704	±0.004	1, 3
E	0.236	0.236	0.236	0.406	0.406	0.406	0.406	±0.008	-
E1	0.154	0.154	0.154	0.295	0.295	0.295	0.295	±0.004	2, 3
e	0.050	0.050	0.050	0.050	0.050	0.050	0.050	Basic	-
L	0.025	0.025	0.025	0.030	0.030	0.030	0.030	±0.009	-
L1	0.041	0.041	0.041	0.056	0.056	0.056	0.056	Basic	-
h	0.013	0.013	0.013	0.020	0.020	0.020	0.020	Reference	-
N	8	14	16	16	20	24	28	Reference	-

Rev. L 2/01

NOTES:

1. Plastic or metal protrusions of 0.006" maximum per side are not included.
2. Plastic interlead protrusions of 0.010" maximum per side are not included.
3. Dimensions "D" and "E1" are measured at Datum Plane "H".
4. Dimensioning and tolerancing per ASME Y14.5M-1994

Plastic Dual-In-Line Packages (PDIP)



MDP0031
PLASTIC DUAL-IN-LINE PACKAGE

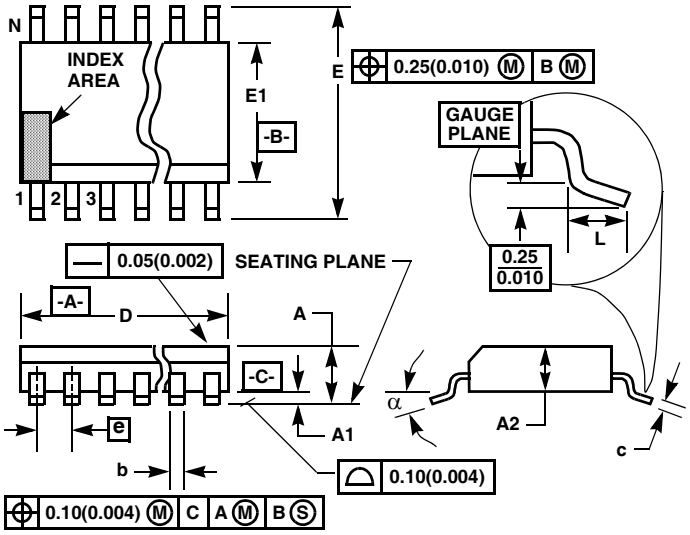
SYMBOL	PDIP8	PDIP14	PDIP16	PDIP18	PDIP20	TOLERANCE	NOTES
A	0.210	0.210	0.210	0.210	0.210	MAX	
A1	0.015	0.015	0.015	0.015	0.015	MIN	
A2	0.130	0.130	0.130	0.130	0.130	±0.005	
b	0.018	0.018	0.018	0.018	0.018	±0.002	
b2	0.060	0.060	0.060	0.060	0.060	+0.010/-0.015	
c	0.010	0.010	0.010	0.010	0.010	+0.004/-0.002	
D	0.375	0.750	0.750	0.890	1.020	±0.010	1
E	0.310	0.310	0.310	0.310	0.310	+0.015/-0.010	
E1	0.250	0.250	0.250	0.250	0.250	±0.005	2
e	0.100	0.100	0.100	0.100	0.100	Basic	
eA	0.300	0.300	0.300	0.300	0.300	Basic	
eB	0.345	0.345	0.345	0.345	0.345	±0.025	
L	0.125	0.125	0.125	0.125	0.125	±0.010	
N	8	14	16	18	20	Reference	

Rev. B 2/99

NOTES:

1. Plastic or metal protrusions of 0.010” maximum per side are not included.
2. Plastic interlead protrusions of 0.010” maximum per side are not included.
3. Dimensions E and eA are measured with the leads constrained perpendicular to the seating plane.
4. Dimension eB is measured with the lead tips unconstrained.
5. 8 and 16 lead packages have half end-leads as shown.

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AC, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M8.173

8 LEAD THIN SHRINK NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.116	0.120	2.95	3.05	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	8		8		7
α	0°	8°	0°	8°	-

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