High-Efficiency, Quad or Triple-Output System Power Supply Controller for Notebook Computers

The ISL62381, ISL62382, ISL62383, ISL62381C, ISL62382C and ISL62383C family of controllers generate supply voltages for battery-powered systems. These controllers include two pulse-width modulation (PWM) controllers, adjustable from 0.6V to 5.5V, and two linear regulators, LDO5 and LDO3, that generate a fixed 5V and an adjustable output respectively, and each can deliver up to 100mA. The ISL62383 and ISL62383C have the same outputs as the ISL62381, ISL62382, ISL62381C and ISL62382C but without LDO3 linear regulator. The channel 2 switching regulator will automatically take over the LDO5 load when programmed to 5V output. This provides a large power savings and boosts efficiency. These controllers include on-board power-up sequencing, two power-good (PGOOD) outputs, digital soft-start, and internal soft-stop output discharge that prevent negative voltages on shutdown.

The patented R^3 PWM control scheme provides a low jitter system with fast response to load transients. Light-load efficiency is improved with period-stretching discontinuous conduction mode (DCM) operation. To eliminate noise in audio frequency applications, an ultrasonic DCM mode is included, which limits the minimum switching frequency to approximately 28kHz.

The ISL62381, ISL62382, ISL62381C and ISL62382C are available in a 32 Ld 5x5 TQFN package, and the ISL62383 and ISL62383C are available in a 28 Ld 4x4 TQFN package. This family of controllers can operate over the extended temperature range (-10°C to +100°C).

Features

- High Performance R^3 Technology
- Fast Transient Response
- ±1% Output Voltage Accuracy: -10°C to +100°C
- Two Fully Programmable Switch-Mode Power Supplies with Independent Operation
- Programmable Switching Frequency
- Integrated MOSFET Drivers and Bootstrap Diode
- Adjustable (+1.2V to +5V) LDO Output
- Fixed +5V LDO Output with Automatic Switchover to SMPS2
- Internal Soft-Start and Soft-Stop Output Discharge
- Wide Input Voltage Range: +5.5V to +25V
- Full and Ultrasonic Pulse-Skipping Mode
- Power-Good Indicator
- Overvoltage, Undervoltage and Overcurrent Protection
- Fault Identification by PGOOD Pull-Down Resistance
- Thermal Monitor and Protection
- Pb-Free (RoHS Compliant)

Applications

- Notebook and Sub-Notebook Computers
- PDAs and Mobile Communication Devices
- 3-Cell and 4-Cell Li+ Battery-Powered Devices
- General Purpose Switching Buck Regulators

Ordering Information

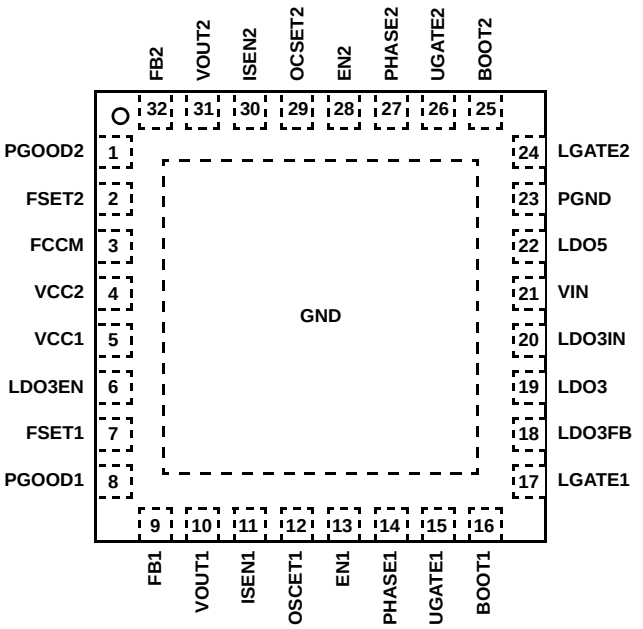
PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL62381HRTZ	62381 HRTZ	-10 to +100	32 Ld 5x5 TQFN	L32.5x5A
ISL62382HRTZ	62382 HRTZ	-10 to +100	32 Ld 5x5 TQFN	L32.5x5A
ISL62383HRTZ	623 83HRTZ	-10 to +100	28 Ld 4x4 TQFN	L28.4x4
ISL62381CHRTZ	62381 CHRTZ	-10 to +100	32 Ld 5x5 TQFN	L32.5x5A
ISL62382CHRTZ	62382 CHRTZ	-10 to +100	32 Ld 5x5 TQFN	L32.5x5A
ISL62383CHRTZ	62383 CHRTZ	-10 to +100	28 Ld 4x4 TQFN	L28.4x4

NOTES:

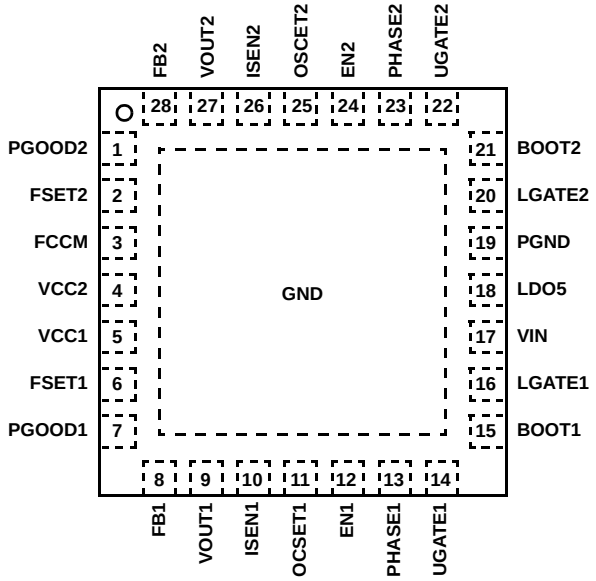
1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL62381, ISL62382, ISL62383, ISL62381C, ISL62382C, ISL62383C. For more information on MSL please see techbrief TB363.

Pinouts

ISL62381, ISL62382, ISL62381C, ISL62382C
(32 LD TQFN)
TOP VIEW



ISL62383, ISL62383C
(28 LD TQFN)
TOP VIEW



Absolute Maximum Ratings

VIN to GND . . . . . -0.3V to +28V
$VCC_{1,2}$, $PGOOD_{1,2}$, LDO5 to GND. . . . . -0.3V to +7.0V
$EN_{1,2}$, LDO3EN. . . . . -0.3V to GND, VCC1 + 0.3V
$VOUT_{1,2}$, $FB_{1,2}$, LDO3FB, $FSET_{1,2}$ . . -0.3V to GND, VCC1 + 0.3V
$PHASE_{1,2}$ to GND . . . . . (DC) -0.3V to +28V
(<100ns Pulse Width, 10µJ). . . . . -5.0V
$BOOT_{1,2}$ to GND . . . . . -0.3V to +33V
$BOOT_{1,2}$ to $PHASE_{1,2}$ . . . . . -0.3V to +7V
$UGATE_{1,2}$ . . . . . (DC) -0.3V to $PHASE_{1,2}$, $BOOT_{1,2}$ + 0.3V
(<200ns Pulse Width, 20µJ) . . . . . -4.0V
$LGATE_{1,2}$. . . . . (DC) -0.3V to GND, VCC1 + 0.3V
(<100ns Pulse Width, 4µJ). . . . . -2.0V
LDO3, LDO5 Output Continuous Current . . . . . +100mA

Thermal Information

Thermal Resistance (Typical, Notes 4, 5)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
32 Ld TQFN Package	30	1.75
28 Ld TQFN Package	37	3

Junction Temperature Range. . . . . -55°C to +150°C
Operating Temperature Range . . . . . -10°C to +100°C
Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Ambient Temperature Range. . . . . -10°C to +100°C
Supply Voltage (VIN to GND) . . . . . 5.5V to 25V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379
5. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

These specifications apply for T_A = -10°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C, VIN = 12V. **Boldface limits apply over the operating temperature range, -10°C to +100°C.**

PARAMETER	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
VIN					
VIN Power-on Reset (POR)	Rising Threshold	**5.3**	5.4	**5.5**	V
	Hysteresis	**20**	80	**150**	mV
VIN Shutdown Supply Current	EN1 = EN2 = GND or Floating, LDO3EN = GND	-	6	**15**	µA
VIN Standby Supply Current	EN1 = EN2 = GND or Floating, LDO3EN = VCC1	-	150	**250**	µA
LINEAR REGULATOR					
LDO5 Output Voltage	$I_{\_LDO5}$ = 0	**4.9**	5.0	**5.1**	V
	$I_{\_LDO5}$ = 100mA (Note 6)	**4.9**	5.0	**5.1**	V
LDO5 Short-Circuit Current (Note 6)	LDO5 = GND	-	190	-	mA
LDO5 UVLO Threshold Voltage (Note 6)	Rising edge of LDO5	-	4.35	-	V
	Falling edge of LDO5	-	4.15	-	V
SMPS2 to LDO5 Switchover Threshold		**4.63**	4.80	**4.93**	V
SMPS2 to LDO5 Switchover Resistance (Note 6)	VOUT2 to LDO5, VOUT2 = 5V	-	2.5	**3.2**	Ω
LDO3 Reference Voltage (Note 6)		-	1.2	-	V
LDO3 Voltage Regulation Range	LDO3IN > V_{LDO3}+dropout	**1.2**	-	**5**	V
LDO3 Short-Circuit Current (Note 6)	LDO3 = GND	-	180	-	mA
LDO3EN Input Voltage	Rising edge	**1.1**	-	**2.5**	V
	Falling edge	**0.94**	-	**1.06**	V
LDO3EN Input Leakage Current	LDO3EN = GND or VCC1	**-1**		**1**	µA
LDO3 Discharge ON-Resistance	LDO3EN = GND	-	36	**60**	Ω
VCC					
VCC Input Bias Current (Note 6)	EN1 = EN2 = VCC1, FB1 = FB2 = 0.65V	-	2	-	mA
VCC1 Start-up Voltage	EN1 = EN2 = LDO3EN = GND	**3.45**	3.6	**3.75**	V

Electrical Specifications These specifications apply for T_A = -10°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C, VIN = 12V. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
VCC2 POR Threshold	Rising edge	**4.35**	4.45	**4.55**	V
	Falling edge	**4.10**	4.20	**4.30**	V
PWM					
Reference Voltage (Note 6)		-	0.6	-	V
Regulation Accuracy	VOUT regulated to 0.6V	**-1**	-	**1**	%
FB Input Bias Current	FB = 0.6V	**-10**	-	**30**	nA
Frequency Range		**200**	-	**600**	kHz
Frequency Set Accuracy (Note 7)	F_{SW} = 300kHz	**-12**	-	**12**	%
VOUT Voltage Regulation Range	VIN > 6V for VOUT = 5.5V	**0.6**	-	**5.5**	V
VOUT Soft-Discharge Resistance		-	14	**50**	Ω
POWER-GOOD					
PGOOD Pull-Down Impedance	Soft-start, $I_{\_PGOOD}$ = 5mA sinking	-	32	**100**	Ω
	UVP, $I_{\_PGOOD}$ = 5mA sinking	-	95	**200**	Ω
	OVP, $I_{\_PGOOD}$ = 5mA sinking	-	63	**150**	Ω
	OCP, $I_{\_PGOOD}$ = 5mA sinking	-	32	**100**	Ω
PGOOD Leakage Current	PGOOD = VCC1	-	0	**1**	µA
Maximum PGOOD Sink Current (Note 6)		-	5	-	mA
PGOOD Soft-start Delay	From EN high to PGOOD high (for one SMPS channel)	**2.20**	2.75	**3.70**	ms
	EN2(1) = Floating, from EN1(2) high to PGOOD2(1) high	**4.50**	5.60	**7.50**	ms
GATE DRIVER					
UGATE Pull-Up ON-Resistance (Note 6)	200mA source current	-	1.0	**1.5**	Ω
UGATE Source Current (Note 6)	UGATE-PHASE = 2.5V	-	2.0	-	A
UGATE Pull-Down ON-Resistance (Note 6)	250mA source current	-	1.0	**1.5**	Ω
UGATE Sink Current (Note 6)	UGATE-PHASE = 2.5V	-	2.0	-	A
LGATE Pull-Up ON-Resistance (Note6)	250mA source current	-	1.0	**1.5**	Ω
LGATE Source Current (Note 6)	LGATE-PGND = 2.5V	-	2.0	-	A
LGATE Pull-Down ON-Resistance (Note 6)	250mA source current	-	0.5	**0.9**	Ω
LGATE Sink Current (Note 6)	LGATE-PGND = 2.5V	-	4.0	-	A
UGATE to LGATE Deadtime (Note 6)	UG falling to LG rising, no load	-	21	-	ns
LGATE to UGATE Deadtime (Note 6)	LG falling to UG rising, no load	-	21	-	ns
Bootstrap Diode Forward Voltage (Note 6)	2mA forward diode current	-	0.58	-	V
Bootstrap Diode Reverse Leakage Current	V_R = 25V	-	0.2	**1**	µA
CONTROL					
FCCM Input Voltage	Low level (DCM enabled)	-	-	**0.8**	V
	Float level (DCM with audio filter)	**1.9**	-	**2.1**	V
	High level (Forced CCM)	**2.4**	-	-	V
FCCM Input Leakage Current	FCCM = GND or VCC1	**-2**	-	**2**	µA

Electrical Specifications These specifications apply for T_A = -10°C to +100°C, unless otherwise noted. Typical values are at T_A = +25°C, VIN = 12V. **Boldface limits apply over the operating temperature range, -10°C to +100°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
Audio Filter Switching Frequency (Note 6)	FCCM floating	-	28	-	kHz
EN Input Voltage	Clear fault level/SMPS OFF level	-	-	**0.8**	V
	Delay start level	**1.9**	-	**2.1**	V
	SMPS ON level	**2.4**	-	-	V
EN Input Leakage Current	EN = GND or VCC1	**-3.5**	-	**3.5**	µA
ISEN Input Impedance (Note 6)	EN = VCC1	-	600	-	kΩ
ISEN Input Leakage Current (Note 6)	EN = GND	-	0.1	-	µA
PROTECTION					
OCSET Input Impedance (Note 6)	EN = VCC1	-	600	-	kΩ
OCSET Input Leakage Current (Note 6)	EN = GND	-	0.1	-	µA
OCSET Current Source	EN = VCC1	**9**	10.0	**10.5**	µA
OCP (V_{OCSET}-V_{ISEN}) Threshold		**-1.75**	0.0	**1.75**	mV
UVP Threshold	Falling edge, referenced to FB	**81**	84	**87**	%
OVP Threshold	Rising edge, referenced to FB	**113**	116	**120**	%
	Falling edge, referenced to FB	**99.5**	103	**106**	%
OTP Threshold (Note 6)	Rising edge	-	150	-	°C
	Falling edge	-	135	-	°C

NOTES:

6. Limits established by characterization and are not production tested.
7. F_{SW} accuracy reflects IC tolerance only; it does not include frequency variation due to V_{IN}, V_{OUT}, L_{OUT}, ESR_{COUT}, or other application specific parameters.
8. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Application Circuits

The below typical application circuits generate the 5V/8A and 3.3V/8A main supplies in a notebook computer. The input supply (VBAT) range is 5.5V to 25V

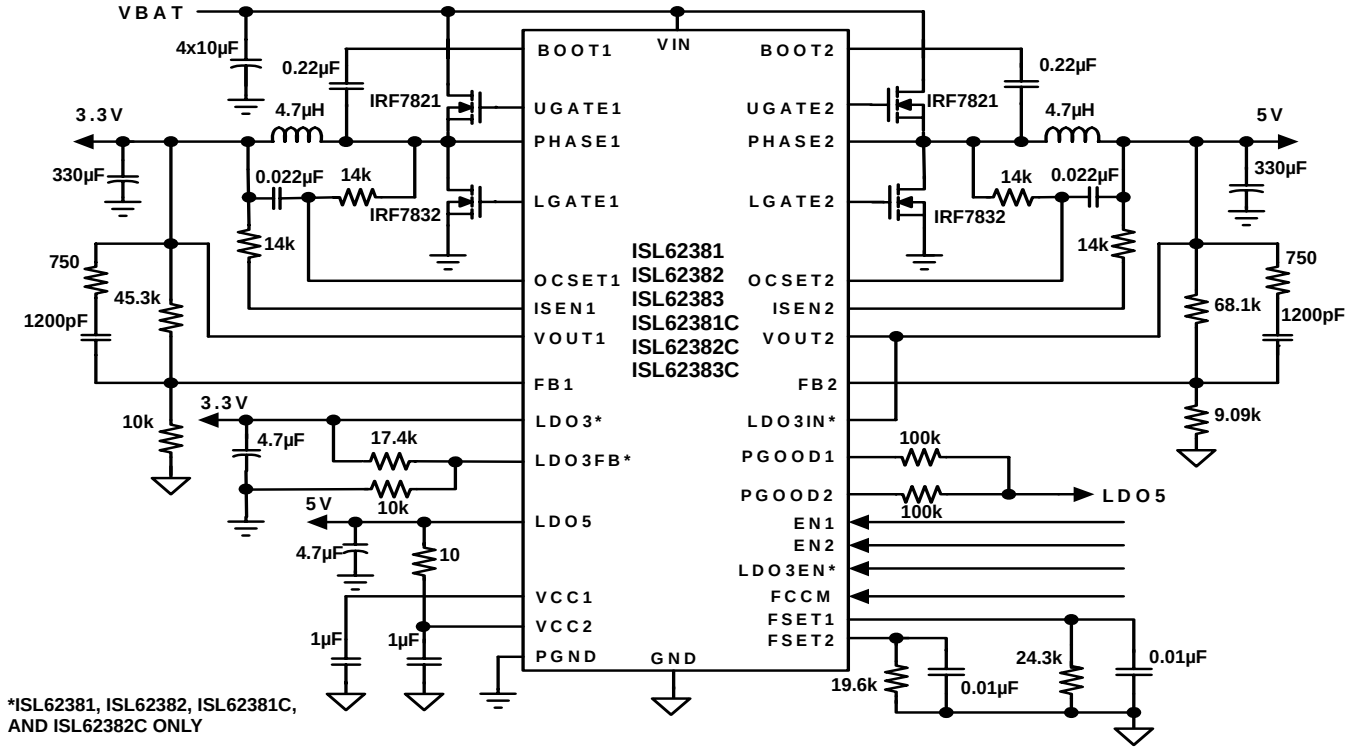


FIGURE 1. TYPICAL APPLICATION CIRCUIT WITH INDUCTOR DCR CURRENT SENSE

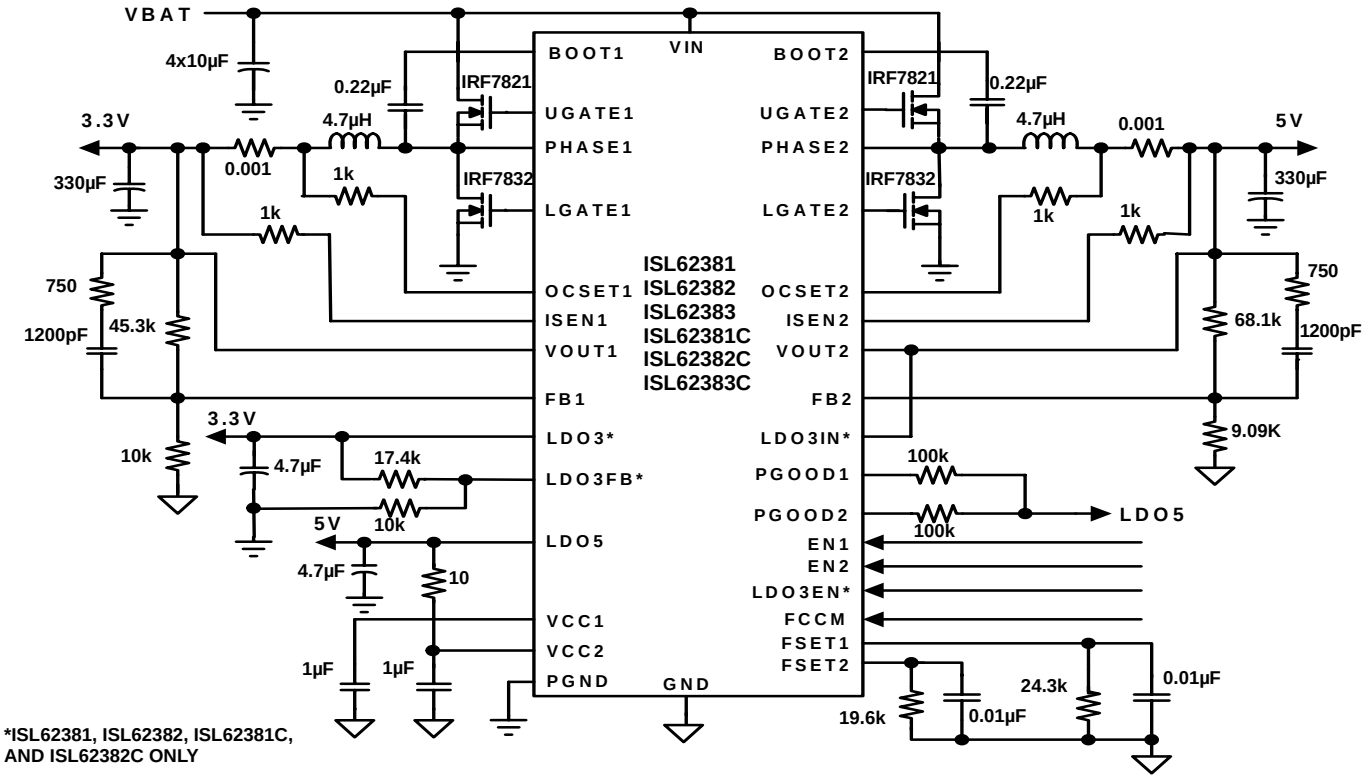


FIGURE 2. TYPICAL APPLICATION CIRCUIT WITH RESISTOR CURRENT SENSE

Typical Application Circuits

The below typical application circuits generate the 1.05V/15A and 1.5V/15A main supplies in a notebook computer. The input supply (VBAT) range is 5.5V to 25V

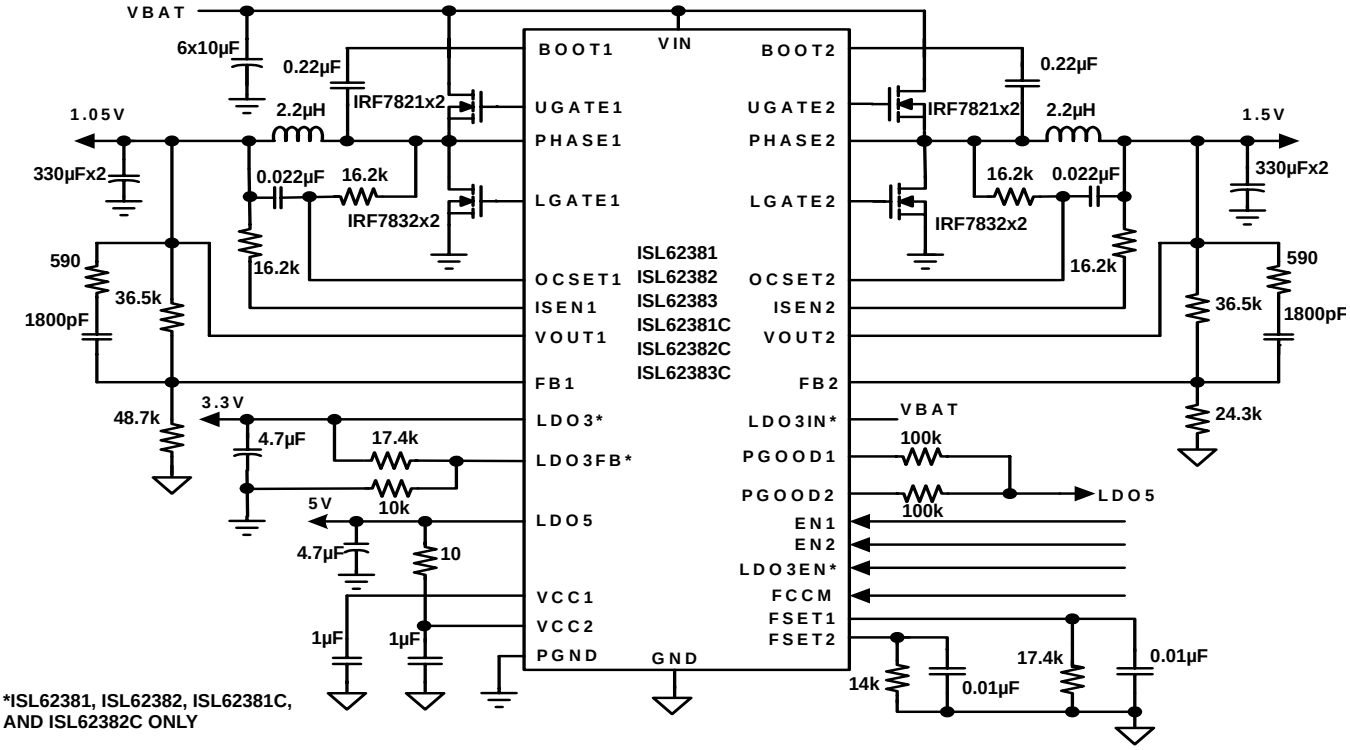


FIGURE 3. TYPICAL APPLICATION CIRCUIT WITH INDUCTOR DCR CURRENT SENSE

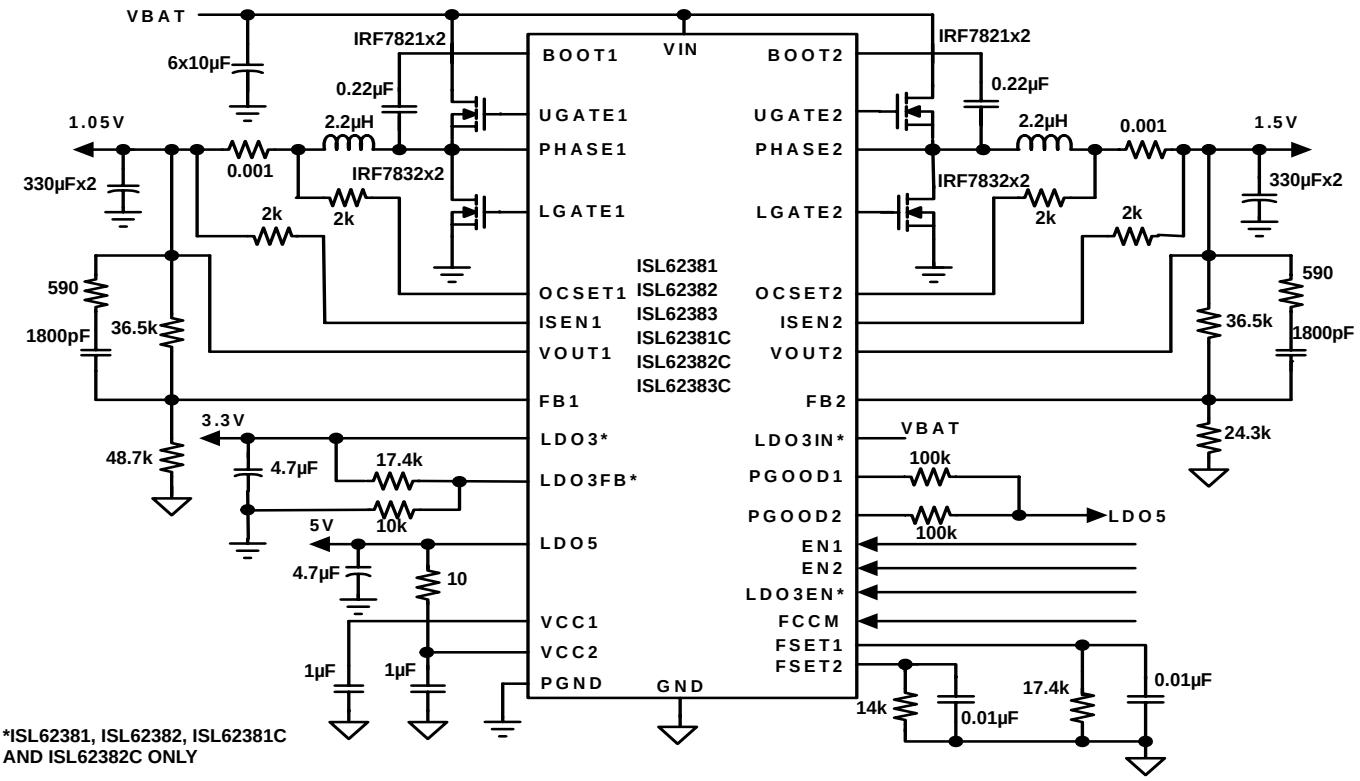


FIGURE 4. TYPICAL APPLICATION CIRCUIT WITH RESISTOR CURRENT SENSE

Pin Descriptions

PIN NUMBER			
28 LD	32 LD	NAME	FUNCTION
1	1	PGOOD2	SMPS2 open-drain power-good status output. Connect to LDO5 through a 100kΩ resistor. Output will be high when the SMPS2 output is within the regulation window with no faults detected.
2	2	FSET2	Frequency control input for SMPS2. Connect a resistor to ground to program the switching frequency. A small ceramic capacitor such as 10nF is necessary to parallel with this resistor to smooth the voltage.
3	3	FCCM	Logic input to control efficiency mode. Logic high forces continuous conduction mode (CCM). Logic low allows full discontinuous conduction mode (DCM). Float this pin for ultrasonic DCM operation.
4	4	VCC2	SMPS2 analog power supply input for reference voltages and currents. Connect to VCC1 with a 10Ω resistor. Bypass to ground with a 1µF ceramic capacitor near the IC.
5	5	VCC1	SMPS1 analog power supply input for reference voltages and currents. It is internally connected to the LDO5 output. Bypass to ground with a 1µF ceramic capacitor near the IC.
-	6	LDO3EN	Logic input for enabling and disabling the LDO3 linear regulator. Positive logic input.
6	7	FSET1	Frequency control input for SMPS1. Connect a resistor to ground to program the switching frequency. A small ceramic capacitor such as 10nF is necessary to parallel with this resistor to smooth the voltage.
7	8	PGOOD1	SMPS1 open-drain power-good status output. Connect to LDO5 through a 100kΩ resistor. Output will be high when the SMPS1 output is within the regulation window with no faults detected.
8	9	FB1	SMPS1 feedback input used for output voltage programming and regulation.
9	10	VOUT1	SMPS1 output voltage sense input. Used for soft-discharge.
10	11	ISEN1	SMPS1 current sense input. Used for overcurrent protection and R^3 regulation.
11	12	OCSET1	Input from current-sensing network used to program the overcurrent shutdown threshold for SMPS1.
12	13	EN1	Logic input to enable and disable SMPS1. A logic high will enable SMPS1 immediately. A logic low will disable SMPS1. Floating this input will delay SMPS1 start-up until after SMPS2 achieves regulation.
13	14	PHASE1	SMPS1 switching node for high-side gate drive return and synthetic ripple modulation. Connect to the switching NMOS source, the synchronous NMOS drain, and the output inductor for SMPS1.
14	15	UGATE1	High-side NMOS gate drive output for SMPS1. Connect to the gate of the SMPS1 switching FET.
15	16	BOOT1	SMPS1 bootstrap input for the switching NMOS gate drivers. Connect to PHASE1 with a 0.22µF ceramic capacitor.
16	17	LGATE1	Low-side NMOS gate drive output for SMPS1. Connect to the gate of the SMPS1 synchronous FET.
-	18	LDO3FB	LDO3 linear regulator feedback input used for output voltage programming and regulation.
-	19	LDO3	LDO3 linear regulator output, providing up to 100mA. Bypass to ground with a 4.7µF ceramic capacitor.
-	20	LDO3IN	Power input for LDO3. Must be connected to a voltage greater than the LDO3 set point plus the dropout voltage.
17	21	VIN	Feed-forward input for line voltage transient compensation. Connect to the power train input voltage.
18	22	LDO5	5V linear regulator output, providing up to 100mA before switchover to SMPS2. Bypass to ground with a 4.7µF ceramic capacitor.
19	23	PGND	Power ground for SMPS1 and SMPS2. This provides a return path for synchronous FET switching currents.
20	24	LGATE2	Low-side NMOS gate drive output for SMPS2. Connect to the gate of the SMPS2 synchronous FET.
21	25	BOOT2	SMPS2 bootstrap input for the switching NMOS gate drivers. Connect to PHASE2 with a 0.22µF ceramic capacitor.
22	26	UGATE2	High-side NMOS gate drive output for SMPS2. Connect to the gate of the SMPS2 switching FET.
23	27	PHASE2	SMPS2 switching node for high-side gate drive return and synthetic ripple modulation. Connect to the switching NMOS source, the synchronous NMOS drain, and the output inductor for SMPS2.
24	28	EN2	Logic input to enable and disable SMPS2. A logic high will enable SMPS2 immediately. A logic low will disable SMPS2. Floating this input will delay SMPS2 start-up until after SMPS1 achieves regulation.
25	29	OCSET2	Input from current-sensing network used to program the over-current shutdown threshold for SMPS2.
26	30	ISEN2	SMPS2 current sense input. Used for overcurrent protection and R^3 regulation.
27	31	VOUT2	SMPS2 output voltage sense input. Used for soft-discharge and switchover to LDO5 output.

Pin Descriptions (Continued)

PIN NUMBER		NAME	FUNCTION
28 LD	32 LD		
28	32	FB2	SMPS2 feedback input used for output voltage programming and regulation.
Bottom Pad	Bottom Pad	GND	Analog ground of the IC. Unless otherwise stated, signals are reference to this GND.

Typical Performance

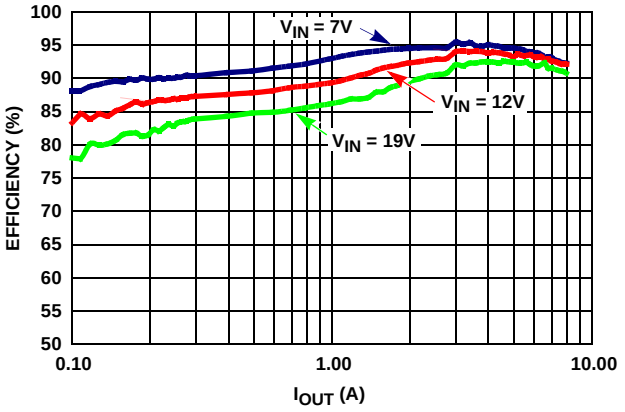


FIGURE 5. CHANNEL 1 EFFICIENCY AT V_O = 3.3V, DEM OPERATION. HIGH-SIDE 1xIRF7821, $r_{DS(ON)}$ = 9.1mΩ; LOW-SIDE 1xIRF7832, $r_{DS(ON)}$ = 4mΩ; L = 4.7µH, DCR = 14.3mΩ; CCM F_{SW} = 270kHz

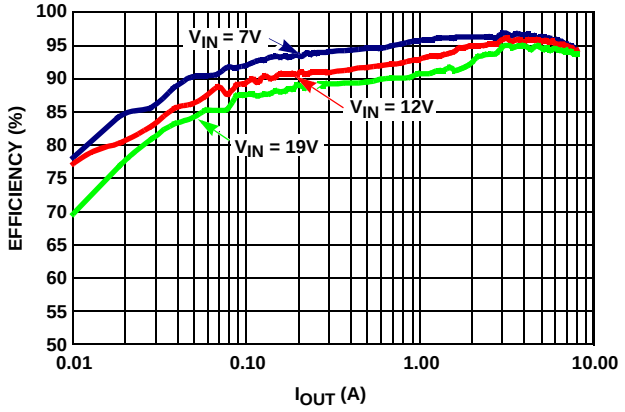


FIGURE 6. CHANNEL 2 EFFICIENCY AT V_O = 5V, DEM OPERATION. HIGH-SIDE 1xIRF7821, $r_{DS(ON)}$ = 9.1mΩ; LOW-SIDE 1xIRF7832, $r_{DS(ON)}$ = 4mΩ; L = 4.7µH, DCR = 14.3mΩ; CCM F_{SW} = 330kHz

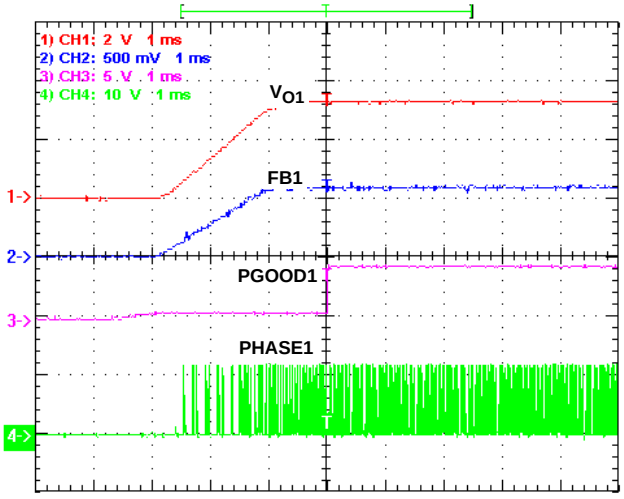


FIGURE 7. POWER-ON, V_{IN} = 12V, LOAD = 5A, V_O = 3.3V

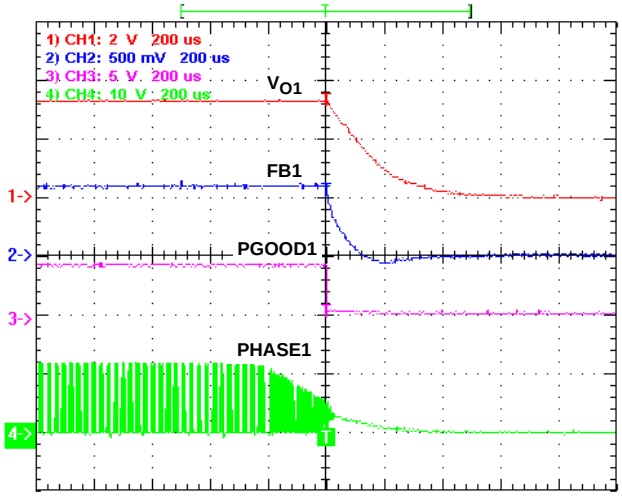


FIGURE 8. POWER-OFF, V_{IN} = 12V, I_O = 5A, V_O = 3.3V

Typical Performance (Continued)

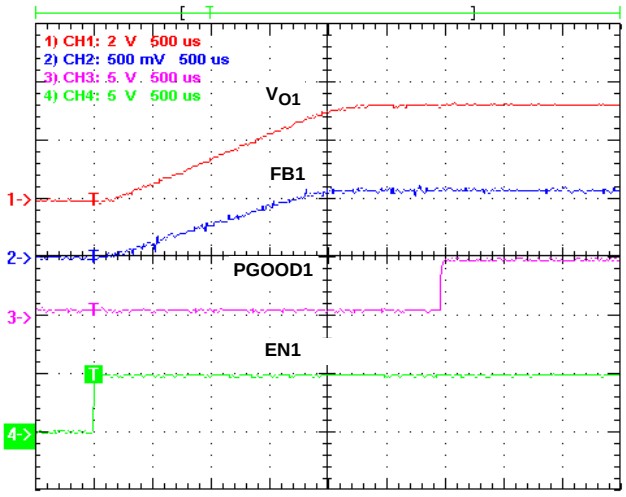


FIGURE 9. ENABLE CONTROL, EN1 = HIGH, V_{IN} = 12V, V_O = 3.3V, I_O = 5A

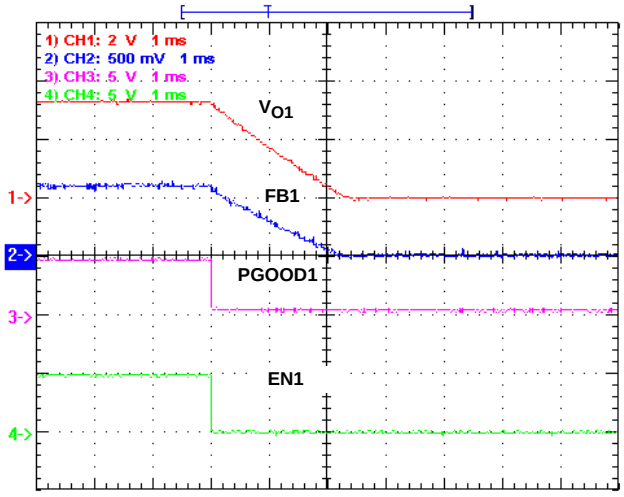


FIGURE 10. ENABLE CONTROL, EN1 = LOW, V_{IN} = 12V, V_O = 3.3V, I_O = 5A

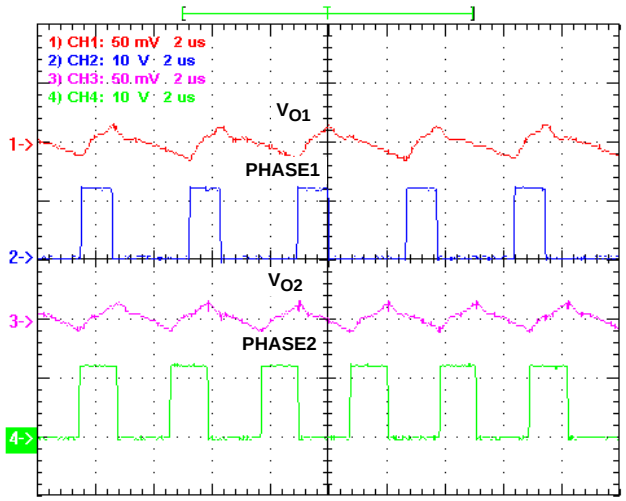


FIGURE 11. CCM STEADY-STATE OPERATION, V_{IN} = 12V, V_{O1} = 3.3V, I_{O1} = 5A, V_{O2} = 5V, I_{O2} = 5A

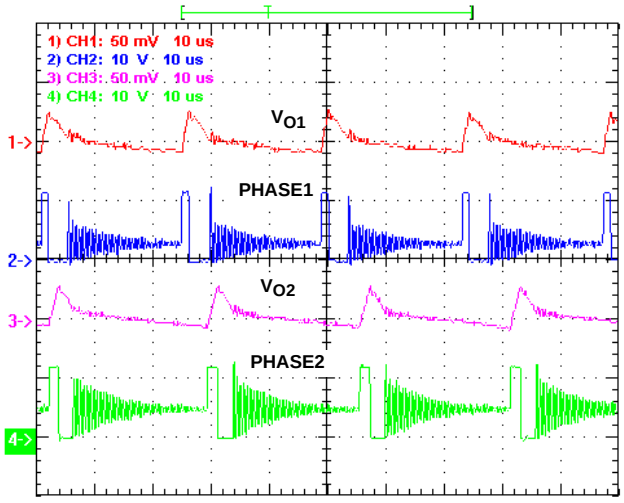


FIGURE 12. DCM STEADY-STATE OPERATION, V_{IN} = 12V, V_{O1} = 3.3V, I_{O1} = 0. 2A, V_{O2} = 5V, I_{O2} = 0. 2A

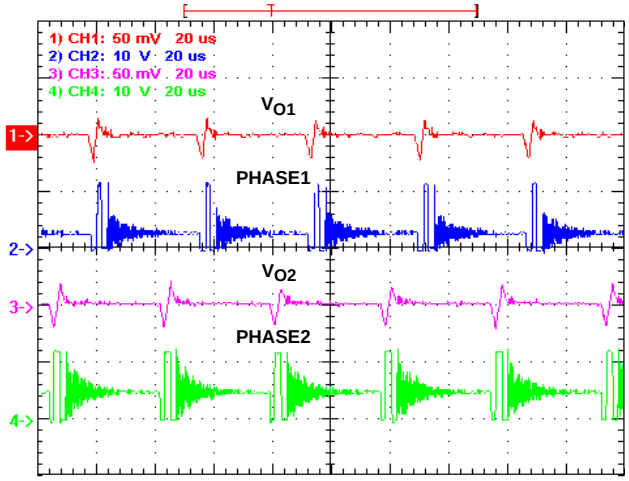


FIGURE 13. AUDIO FILTER OPERATION, V_{IN} = 12V, V_{O1} = 3.3V, V_{O2} = 5V, NO LOAD

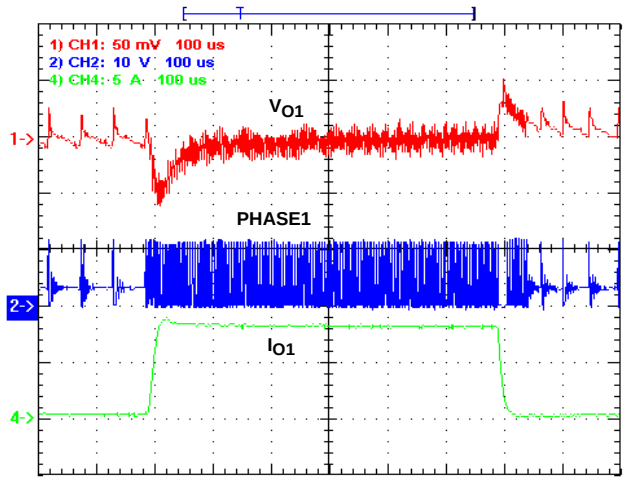


FIGURE 14. TRANSIENT RESPONSE, V_{IN} = 12V, V_O = 3.3V, I_O = 0.1A/8.1A @ 2.5A/µs

Typical Performance (Continued)

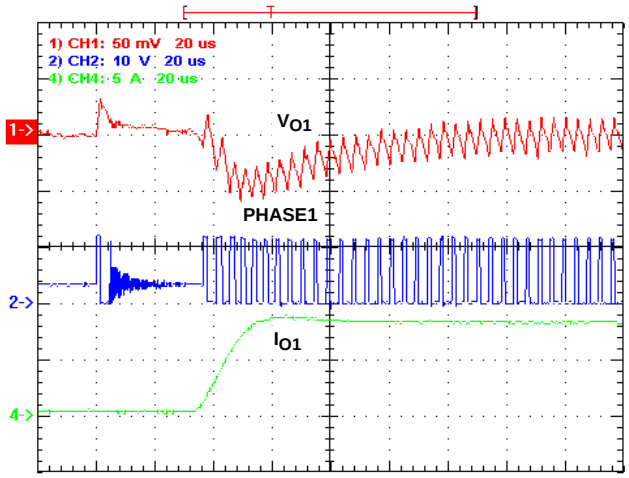


FIGURE 15. LOAD INSERTION RESPONSE, V_{IN} = 12V, V_O = 3.3V, I_O = 0.1A/8.1A @ 2.5A/µs

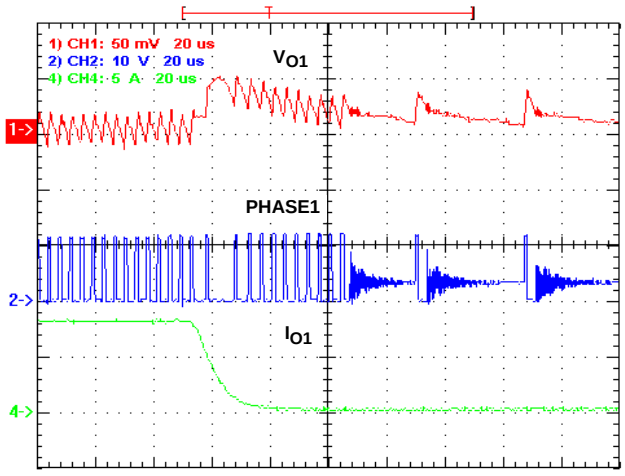


FIGURE 16. LOAD RELEASE RESPONSE, V_{IN} = 12V, V_O = 3.3V, I_O = 0.1A/8.1A @ 2.5A/µs

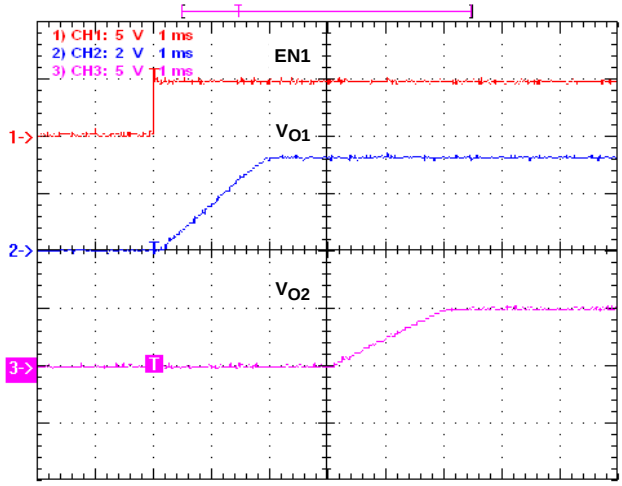


FIGURE 17. DELAYED START, V_{IN} = 12V, V_{O1} = 3.3V, V_{O2} = 5V, EN2 = FLOAT, NO LOAD

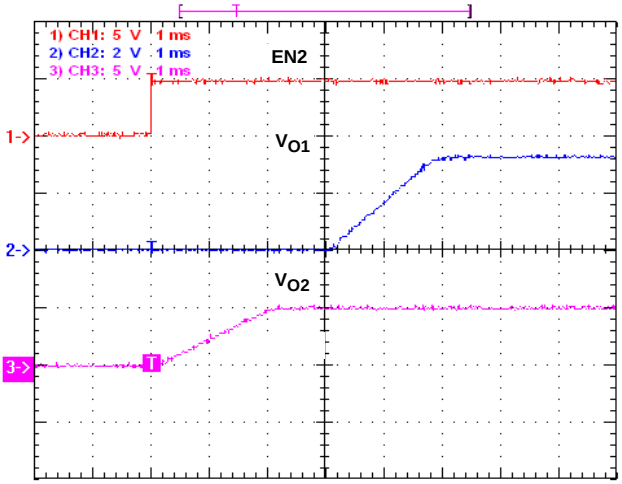


FIGURE 18. DELAYED START, V_{IN} = 12V, V_{O1} = 3.3V, V_{O2} = 5V, EN1 = FLOAT, NO LOAD

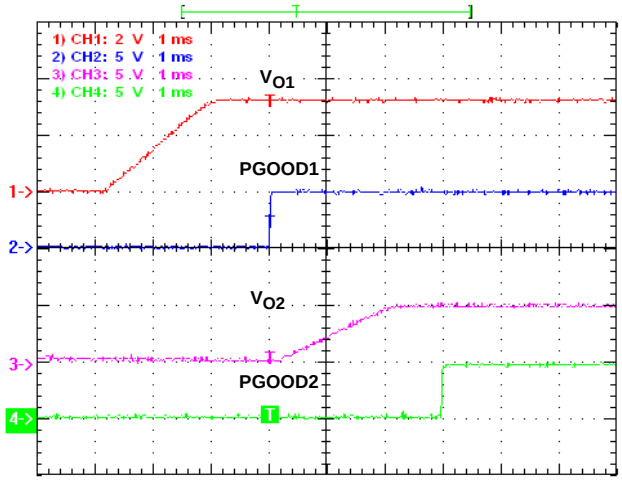


FIGURE 19. DELAYED START, V_{IN} = 12V, V_{O1} = 3.3V, V_{O2} = 5V, EN1 = 1, EN2 = FLOAT, NO LOAD

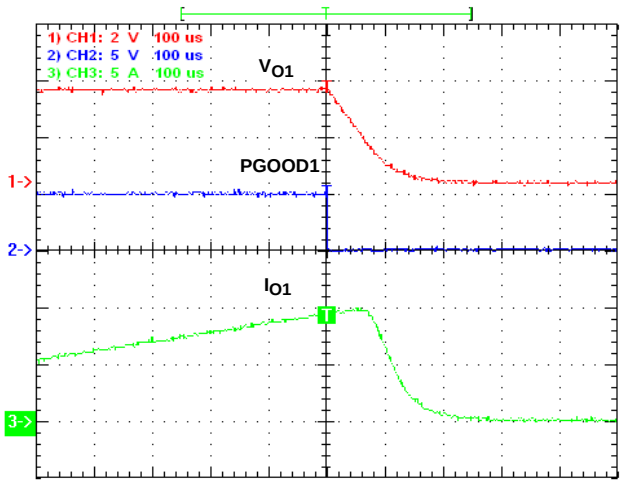


FIGURE 20. OVERCURRENT PROTECTION, V_{IN} = 12V, V_O = 3.3V

Typical Performance (Continued)

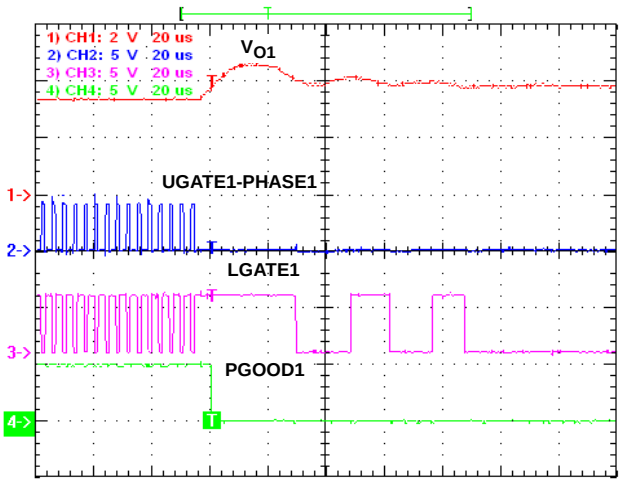


FIGURE 21. CROWBAR OVERVOLTAGE PROTECTION, V_{IN} = 12V, V_O = 3.3V, NO LOAD

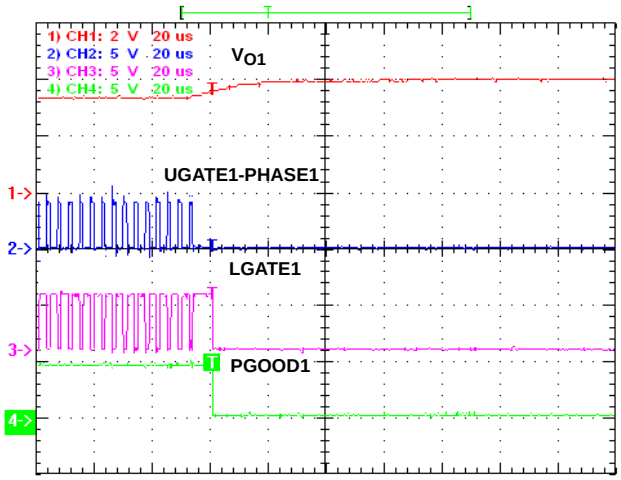
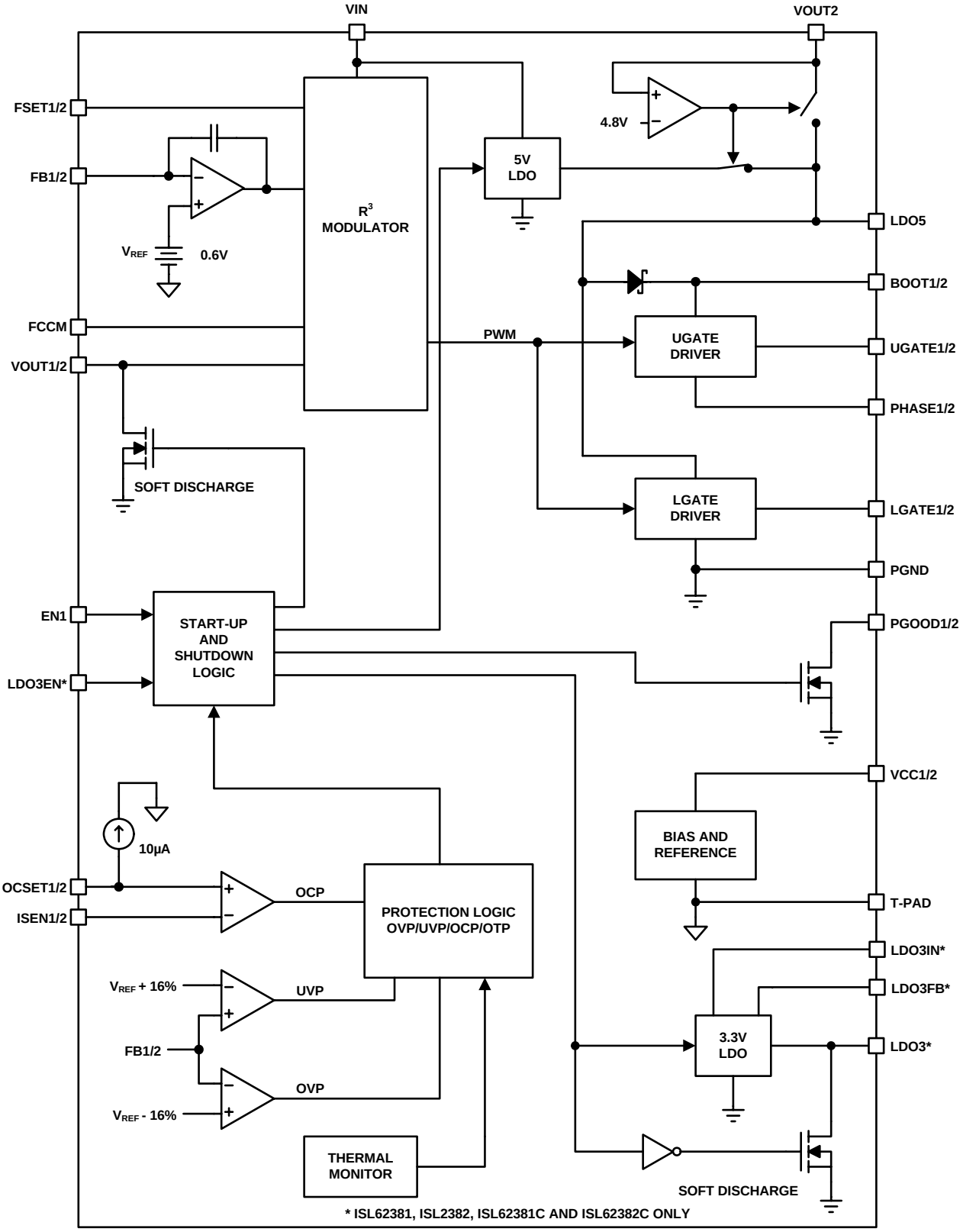


FIGURE 22. TRI-STATE OVERVOLTAGE PROTECTION, V_{IN} = 12V, V_O = 3.3V, NO LOAD

Block Diagram



Theory of Operation

Four Output Controller

The ISL62381, ISL62382, ISL62381C and ISL62382C generate four regulated output voltages, including two PWM controllers and two LDOs. The two PWM channels are identical and almost entirely independent, with the exception of sharing the GND pin. Unless otherwise stated, only one individual channel is discussed, and the conclusion applies to both channels.

PWM Modulator

The ISL62381, ISL62382, ISL62383, ISL62381C, ISL62382C and ISL62383C modulator features Intersil's R^3 technology, a hybrid of fixed frequency PWM control and variable frequency hysteretic control. Intersil's R^3 technology can simultaneously affect the PWM switching frequency and PWM duty cycle in response to input voltage and output load transients. The R^3 modulator synthesizes an AC signal V_R, which is an analog representation of the output inductor ripple current. The duty-cycle of V_R is the result of charge and discharge current through a ripple capacitor C_R. The current through C_R is provided by a transconductance amplifier g_m that measures the VIN and VO pin voltages. The positive slope of V_R can be written as Equation 1:

$$V_{RPOS} = g_m \cdot (V_{IN} - V_{OUT}) / C_R \quad \text{(EQ. 1)}$$

The negative slope of V_R can be written as Equation 2:

$$V_{RNEG} = g_m \cdot V_{OUT} / C_R \quad \text{(EQ. 2)}$$

Where g_m is the gain of the transconductance amplifier.

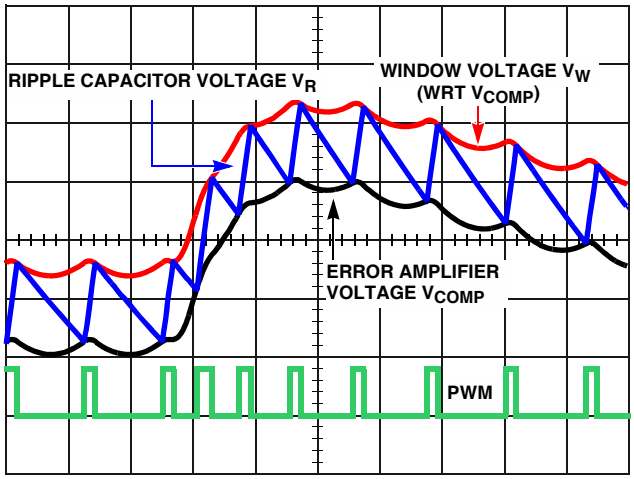


FIGURE 23. MODULATOR WAVEFORMS DURING LOAD TRANSIENT

A window voltage V_W is referenced with respect to the error amplifier output voltage V_{COMP}, creating an envelope into which the ripple voltage V_R is compared. The amplitude of V_W is set by a resistor connected across the FSET and GND pins. The V_R, V_{COMP}, and V_W signals feed into a window comparator in which V_{COMP} is the lower threshold voltage and $V_{COMP} + V_W$ is the higher threshold voltage. Figure 23 shows PWM pulses being generated as V_R traverses the V_{COMP} and $V_{COMP} + V_W$ thresholds. The PWM switching frequency is proportional to the slew rates of the positive and negative slopes of V_R; it is inversely proportional to the voltage between V_W and V_{COMP}. Equation 3 illustrates how to calculate the window size based on output voltage and frequency set resistor R_W.

$$V_W = g_m \cdot V_{OUT} \cdot (1 - D) \cdot R_W \quad \text{(EQ. 3)}$$

Programming the PWM Switching Frequency

These controllers do not use a clock signal to produce PWMs. The PWM switching frequency F_{SW} is programmed by the resistor R_W that is connected from the FSET pin to the GND pin. The approximate PWM switching frequency can be expressed as written in Equation 4:

$$F_{SW} = \frac{1}{10 \cdot C_R \cdot R_W} \quad \text{(EQ. 4)}$$

For a desired F_{SW}, the R_W can be selected by Equation 5.

$$R_W = \frac{1}{10 \cdot C_R \cdot F_{SW}} \quad \text{(EQ. 5)}$$

where C_R = 17pF with ±20% error range. To smooth the FSET pin voltage, a ceramic capacitor such as 10nF is necessary to parallel with R_W.

It is recommended that whenever the control loop compensation network is modified, F_{SW} should be checked for the correct frequency and if necessary, adjust R_W.

Power-On Reset

These controllers are disabled until the voltage at the VIN pin has increased above the rising power-on reset (POR) threshold voltage. The controller will be disabled when the voltage at the VIN pin decreases below the falling POR threshold.

In addition to VIN POR, the LDO5 pin is also monitored. If its voltage falls below 4.2V, the SMPS outputs will be shut down. This ensures that there is sufficient BOOT voltage to enhance the upper MOSFET.

EN, Soft-Start and PGOOD

These controllers use a digital soft-start circuit to ramp the output voltage of each SMPS to the programmed regulation setpoint at a predictable slew rate. The slew rate of the soft-start sequence has been selected to limit the in-rush current through the output capacitors as they charge to the desired regulation voltage. When the EN pins are pulled above their rising thresholds, the PGOOD Soft-Start Delay, t_{SS}, starts and the output voltage begins to rise. The FB pin ramps to 0.6V in approximately 1.5ms and the PGOOD pin goes to high impedance approximately 1.25ms after the FB pin voltage reaches 0.6V.

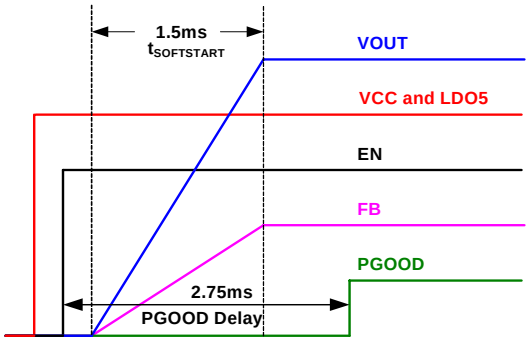


FIGURE 24. SOFT-START SEQUENCE FOR ONE SMPS

The PGOOD pin indicates when the converter is capable of supplying regulated voltage. It is an undefined impedance if V_{IN} is not above the rising POR threshold or below the POR falling threshold. When a fault is detected, these controllers will turn on the open-drain NMOS, which will pull PGOOD low with a nominal impedance of 63Ω or 95Ω. This will flag the system that one of the output voltages is out of regulation.

Separate enable pins allow for full soft-start sequencing. Because low shutdown quiescent current is necessary to prolong battery life in notebook applications, the LDO5 5V LDO is held off until any of the three enable signals (EN1, EN2 or LDO3EN) is pulled high. Soft-start of all outputs will only start until after LDO5 is above the 4.2V POR threshold. In addition to user-programmable sequencing, these controllers include a pre-programmed sequential SMPS soft-start feature. Table 1 shows the SMPS enable truth table.

TABLE 1. SMPS ENABLE SEQUENCE LOGIC

EN1	EN2	START-UP SEQUENCE
0	0	Both SMPS outputs OFF simultaneously
0	Float	Both SMPS outputs OFF simultaneously
Float	0	Both SMPS outputs OFF simultaneously
Float	Float	Both SMPS outputs OFF simultaneously
0	1	SMPS1 OFF, SMPS2 ON
1	0	SMPS1 ON, SMPS2 OFF
1	1	Both SMPS outputs ON simultaneously
Float	1	SMPS1 enables after SMPS2 is in regulation
1	Float	SMPS2 enables after SMPS1 is in regulation

VCC1

The VCC1 nominal operation voltage is 5V. If EN1, EN2 and LDO3EN are all logic low, the VCC1 start-up voltage is 3.6V when VIN is applied on these controllers. LDO5 is held off until any of the three enable signals (EN1, EN2 or LDO3EN) is pulled high. When LDO5 is above the 4.2V VCC1 POR threshold, VCC1 will switchover to LDO5 internally.

After VIN is applied, the VCC1 start-up 3.6V voltage can be used as the logic high signal of any of EN1, EN2 and LDO3EN to enable PVCC if there is no other power supply on the board.

MOSFET Gate-Drive Outputs LGATE and UGATE

These controllers have internal gate-drivers for the high-side and low-side N-Channel MOSFETs. The low-side gate-drivers are optimized for low duty-cycle applications where the low-side MOSFET conduction losses are dominant, requiring a low $r_{DS(ON)}$ MOSFET. The LGATE pull-down resistance is small in order to clamp the gate of the MOSFET below the $V_{GS(th)}$ at turn-off. The current transient through the gate at turn-off can be considerable because the gate charge of a low $r_{DS(ON)}$ MOSFET can be large. Adaptive shoot-through protection prevents a gate-driver output from turning on until the opposite gate-driver output has fallen below approximately 1V. The dead-time shown in Figure 25 is extended by the additional period that the falling gate voltage stays above the 1V threshold. The typical dead-time is 21ns. The high-side gate-driver output voltage is measured across the UGATE and PHASE pins while the low-side gate-driver output voltage is measured across the LGATE and PGND pins. The power for the LGATE gate-driver is sourced directly from the LDO5 pin. The power for the UGATE gate-driver is sourced from a “boot” capacitor connected across the BOOT and PHASE pins. The boot capacitor is charged from the 5V LDO5 supply through a “boot diode” each time the low-side MOSFET turns on, pulling the PHASE pin low. These controllers have integrated boot diodes connected from the LDO5 pins to BOOT pins.

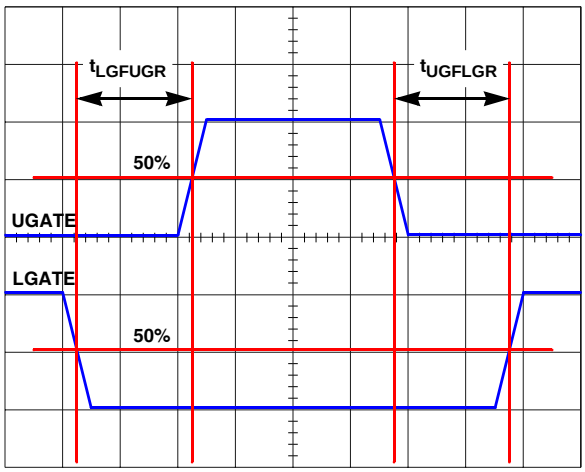


FIGURE 25. LGATE AND UGATE DEAD-TIME

Diode Emulation

FCCM is a logic input that controls the power state of these controllers. If forced high, these controllers will operate in forced continuous-conduction-mode (CCM) over the entire load range. This will produce the best transient response to all load conditions, but will have increased light-load power loss. If FCCM is forced low, these controllers will automatically operate in diode-emulation-mode (DEM) at light load to optimize efficiency in the entire load range. The

transition is automatically achieved by detecting the load current and turning off LGATE when the inductor current reaches 0A.

Positive-going inductor current flows from either the source of the high-side MOSFET, or the drain of the low-side MOSFET. Negative-going inductor current flows into the drain of the low-side MOSFET. When the low-side MOSFET conducts positive inductor current, the phase voltage will be negative with respect to the GND and PGND pins. Conversely, when the low-side MOSFET conducts negative inductor current, the phase voltage will be positive with respect to the GND and PGND pins. These controllers monitor the phase voltage when the low-side MOSFET is conducting inductor current to determine its direction.

When the output load current is greater than or equal to ½ the inductor ripple current, the inductor current is always positive, and the converter is always in CCM. These controllers minimize the conduction loss in this condition by forcing the low-side MOSFET to operate as a synchronous rectifier.

When the output load current is less than ½ the inductor ripple current, negative inductor current occurs. Sinking negative inductor current through the low-side MOSFET lowers efficiency through unnecessary conduction losses. These controllers automatically enter DEM after the PHASE pin has detected positive voltage and LGATE was allowed to go high for eight consecutive PWM switching cycles. These controllers will turn off the low-side MOSFET once the phase voltage turns positive, indicating negative inductor current. These controllers will return to CCM on the following cycle after the PHASE pin detects negative voltage, indicating that the body diode of the low-side MOSFET is conducting positive inductor current.

Efficiency can be further improved with a reduction of unnecessary switching losses by reducing the PWM frequency. It is characteristic of the R^3 architecture for the PWM frequency to decrease while in diode emulation. The extent of the frequency reduction is proportional to the reduction of load current. Upon entering DEM, the PWM frequency makes an initial step-reduction because of a 33% step-increase of the window voltage V_W.

Because the switching frequency in DEM is a function of load current, very light load conditions can produce frequencies well into the audio band. This can be problematic if audible noise is coupled into audio amplifier circuits. To prevent this from occurring, these controllers allow the user to float the FCCM input. This will allow DEM at light loads, but will prevent the switching frequency from going below ~28kHz to prevent noise injection into the audio band. A timer is reset each PWM pulse. If the timer exceeds 30µs, LGATE is turned on, causing the ramp voltage to reduce until another UGATE is commanded by the voltage loop.

Overcurrent Protection

The overcurrent protection (OCP) setpoint is programmed with resistor, R_{OCSET}, that is connected across the OCSET and PHASE pins.

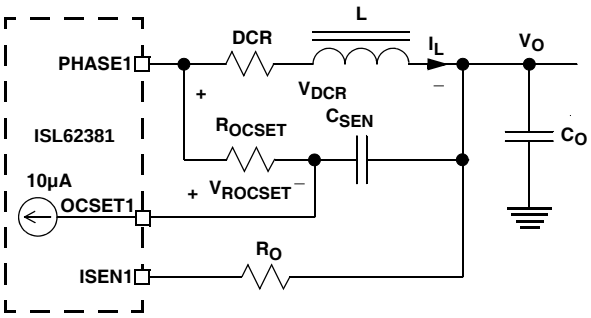


FIGURE 26. OVERCURRENT-SET CIRCUIT

Figure 26 shows the overcurrent-set circuit for SMPS1. The inductor consists of inductance L and the DC resistance (DCR). The inductor DC current I_L creates a voltage drop across DCR, given by Equation 6:

$$V_{DCR} = I_L \cdot DCR \quad \text{(EQ. 6)}$$

Theses controllers sink a 10µA current into the OCSET1 pin, creating a DC voltage drop across the resistor R_{OCSET}, given by Equation 7:

$$V_{ROCSET} = 10\mu A \cdot R_{OCSET} \quad \text{(EQ. 7)}$$

Resistor R_O is connected between the ISEN1 pin and the actual output of the converter. During normal operation, the ISEN1 pin is a high impedance path, therefore there is no voltage drop across R_O. The DC voltage difference between the OCSET1 pin and the ISEN1 pin can be established using Equation 8:

$$V_{OCSET1} - V_{ISEN1} = I_L \cdot DCR - 10\mu A \cdot R_{OCSET} \quad \text{(EQ. 8)}$$

These controllers monitor the OCSET1 pin and the ISEN1 pin voltages. Once the OCSET1 pin voltage is higher than the ISEN1 pin voltage for more than 10µs, these controllers declare an OCP fault. The value of R_{OCSET} is then written as Equation 9:

$$R_{OCSET} = \frac{I_{OC} \cdot DCR}{10\mu A} \quad \text{(EQ. 9)}$$

Where:

- R_{OCSET} (Ω) is the resistor used to program the overcurrent setpoint
- I_{OC} is the output current threshold that will activate the OCP circuit
- DCR is the inductor DC resistance

For example, if I_{OC} is 20A and DCR is 4.5mΩ, the choice of R_{OCSET} is R_{OCSET} = 20A x 4.5mΩ/10µA = 9kΩ.

Resistor R_{OCSET} and capacitor C_{SEN} form an RC network to sense the inductor current. To sense the inductor current correctly, not only in DC operation but also during dynamic operation, the RC network time constant $R_{OCSET}C_{SEN}$ needs to match the inductor time constant L/DCR. The value of C_{SEN} is then written as Equation 10:

$$C_{SEN} = \frac{L}{R_{OCSET} \cdot DCR} \quad \text{(EQ. 10)}$$

For example, if L is 1.5µH, DCR is 4.5mΩ, and R_{OCSET} is 9kΩ, the choice of C_{SEN} = 1.5µH/(9kΩ x 4.5mΩ) = 0.037µF.

Upon converter start-up, the C_{SEN} capacitor bias is 0V. To prevent false OCP during this time, a 10µA current source flows out of the ISEN1 pin, generating a voltage drop on the R_O resistor, which should be chosen to have the same resistance as R_{OCSET}. When PGOOD pin goes high, the ISEN1 pin current source will be removed.

When an OCP fault is declared, the PGOOD pin will pull-down to 32Ω and latch off the converter. The fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage, or until V_{IN} has decayed below the falling POR threshold.

When using a discrete current sense resistor, inductor time-constant matching is not required. Equation 7 remains unchanged, but Equation 8 is modified in Equation 11:

$$V_{OCSET1} - V_{ISEN1} = I_L \cdot R_{SENSE} - 10\mu A \cdot R_{OCSET} \quad \text{(EQ. 11)}$$

Furthermore, Equation 9 is changed in Equation 12:

$$R_{OCSET} = \frac{I_{OC} \cdot R_{SENSE}}{10\mu A} \quad \text{(EQ. 12)}$$

Where R_{SENSE} is the series power resistor for sensing inductor current. For example, with an R_{SENSE} = 1mΩ and an OCP target of 10A, R_{OCSET} = 1kΩ.

Overvoltage Protection

The OVP fault detection circuit triggers after the FB pin voltage is above the rising overvoltage threshold for more than 2µs. The FB pin voltage is 0.6V in normal operation. The rising over voltage threshold is typically 116% of that value, or 1.16*0.6V = 0.696V.

When an OVP fault is declared, the PGOOD pin will pull down with 65Ω and latch-off the converter. The OVP fault will remain latched until the EN pin has been pulled below the falling EN threshold voltage, or until V_{IN} has decayed below the falling POR threshold.

For ISL62381, ISL62381C, ISL62383 and ISL62383C, although the converter has latched-off in response to an OVP fault, the LGATE gate-driver output will retain the ability to toggle the low-side MOSFET on and off in response to the output voltage transversing the OVP rising and falling thresholds. The LGATE gate-driver will turn on the low-side MOSFET to discharge the output voltage, thus protecting the load from potentially damaging voltage levels. The LGATE gate-driver will turn off the low-side MOSFET once the FB pin voltage is lower than the falling overvoltage threshold for more than 2µs. The falling overvoltage threshold is typically 106% of the reference voltage, or 1.06*0.6V = 0.636V. This process repeats as long as the output voltage fault is present, allowing the ISL62381, ISL62381C, ISL62383 and ISL62383C to protect against persistent overvoltage conditions.

For ISL62382 and ISL62382C, if OVP is detected, it simply tri-states the PHASE node by turning UGATE and LGATE off.

Undervoltage Protection

The UVP fault detection circuit triggers after the FB pin voltage is below the undervoltage threshold for more than 2µs. The undervoltage threshold is typically 86% of the reference voltage, or 0.86*0.6V = 0.516V. If a UVP fault is declared, and the PGOOD pin will pull-down with 93Ω and latch-off the converter. The fault will remain latched until the EN pin has been pulled below the falling enable threshold, or if V_{IN} has decayed below the falling POR threshold.

Programming the Output Voltage

When the converter is in regulation, there will be 0.6V between the FB and GND pins. Connect a two-resistor voltage divider across the OUT and GND pins with the output node connected to the FB pin, as shown in Figure 27. Scale the voltage-divider network such that the FB pin is 0.6V with respect to the GND pin when the converter is regulating at the desired output voltage. The output voltage can be programmed from 0.6V to 5.5V.

Programming the output voltage is written as Equation 13:

$$V_{OUT} = V_{REF} \cdot \left(1 + \frac{R_{TOP}}{R_{BOTTOM}}\right) \quad \text{(EQ. 13)}$$

Where:

- V_{OUT} is the desired output voltage of the converter
- The voltage to which the converter regulates the FB pin is the V_{REF} (0.6V)
- R_{TOP} is the voltage-programming resistor that connects from the FB pin to the converter output. In addition to setting the output voltage, this resistor is part of the loop compensation network
- R_{BOTTOM} is the voltage-programming resistor that connects from the FB pin to the GND pin

Choose R_{TOP} first when compensating the control loop, and then calculate R_{BOTTOM} according to Equation 14:

$$R_{BOTTOM} = \frac{V_{REF} \cdot R_{TOP}}{V_{OUT} - V_{REF}} \quad \text{(EQ. 14)}$$

Compensation Design

Figure 27 shows the recommended Type-II compensation circuit. The FB pin is the inverting input of the error amplifier. The COMP signal, the output of the error amplifier, is inside the chip and unavailable to users. C_{INT} is a 100pF capacitor

integrated inside the IC that connects across the FB pin and the COMP signal. R_{TOP}, R_{FB}, C_{FB} and C_{INT} form the Type-II compensator. The frequency domain transfer function is given by Equation 15:

$$G_{COMP}(s) = \frac{1 + s \cdot (R_{TOP} + R_{FB}) \cdot C_{FB}}{s \cdot R_{TOP} \cdot C_{INT} \cdot (1 + s \cdot R_{FB} \cdot C_{FB})} \quad \text{(EQ. 15)}$$

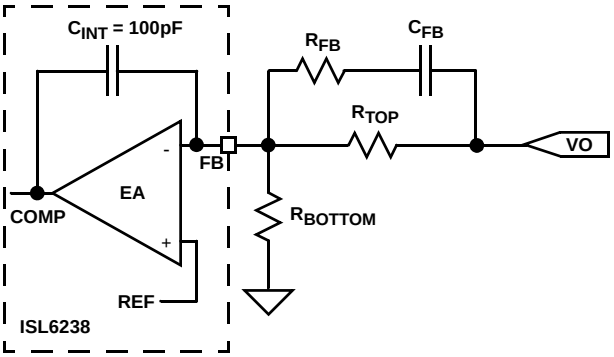


FIGURE 27. COMPENSATION REFERENCE CIRCUIT

The LC output filter has a double pole at its resonant frequency that causes rapid phase change. The R^3 modulator used in these controllers make the LC output filter resemble a first order system in which the closed loop stability can be achieved with the recommended Type-II compensation network. Intersil provides a PC-based tool (example page is shown later) that can be used to calculate compensation network component values and help simulate the loop frequency response.

LDO5 Linear Regulator

In addition to the two SMPS outputs, these controllers also provide two linear regulator outputs. LDO5 is fixed 5V LDO output capable of sourcing 100mA continuous current.

When the output of SMPS2 is programmed to 5V, SMPS2 will automatically take over the load of LDO5. This provides a large power savings and boosts the efficiency. After switchover to SMPS2, the LDO5 output current plus the MOSFET drive current should not exceed 100mA in order to guarantee the LDO5 output voltage in the range of 5V ±5%. The total MOSFET drive current can be estimated by Equation 16.

$$I_{DRIVE} = Q_g \cdot F_{SW} \quad \text{(EQ. 16)}$$

where Q_g is the total gate charge of all the power MOSFET in two SMPS regulators. Then the LDO5 output load current should be less than 100mA-I_{DRIVE}.

LDO3 Linear Regulator

ISL62381, ISL62381C, ISL62382 and ISL62382C include LDO3 linear regulator whose output is adjustable from 1.2V to 5V through LDO3FB pin with a 1.2V reference voltage. It can be independently enabled from both SMPS channels. Logic high of LDO3EN will enable LDO3. LDO3 is capable of sourcing 100mA continuous current and draws its power from LDO3IN pin, which must be connected to a voltage greater than the LDO3 output voltage plus the dropout voltage.

Currents in excess of the limit will cause the LDO3 voltage to drop dramatically, limiting the power dissipation.

Thermal Monitor and Protection

LDO3 and LDO5 can dissipate non-trivial power inside these controllers at high input-to-output voltage ratios and full load conditions. To protect the silicon, these controllers continually monitor the die temperature. If the temperature exceeds +150°C, all outputs will be turned off to sharply curtail power dissipation. The outputs will remain off until the junction temperature has fallen below +135°C.

General Application Design Guide

This design guide is intended to provide a high-level explanation of the steps necessary to design a single-phase power converter. It is assumed that the reader is familiar with many of the basic skills and techniques referenced in the following section. In addition to this guide, Intersil provides complete reference designs that include schematics, bills of materials, and example board layouts.

Selecting the LC Output Filter

The duty cycle of an ideal buck converter is a function of the input and the output voltage. This relationship is written as Equation 17:

$$D = \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 17)}$$

The output inductor peak-to-peak ripple current is written as Equation 18:

$$I_{PP} = \frac{V_{OUT} \cdot (1 - D)}{F_{SW} \cdot L} \quad \text{(EQ. 18)}$$

A typical step-down DC/DC converter will have an I_{P-P} of 20% to 40% of the maximum DC output load current. The value of I_{P-P} is selected based upon several criteria such as MOSFET switching loss, inductor core loss, and the resistive loss of the inductor winding. The DC copper loss of the inductor can be estimated by Equation 19:

$$P_{COPPER} = I_{LOAD}^2 \cdot DCR \quad \text{(EQ. 19)}$$

Where I_{LOAD} is the converter output DC current.

The copper loss can be significant so attention has to be given to the DCR selection. Another factor to consider when choosing the inductor is its saturation characteristics at elevated temperatures. A saturated inductor could cause destruction of circuit components, as well as nuisance OCP faults.

A DC/DC buck regulator must have output capacitance C_O into which ripple current I_{P-P} can flow. Current I_{P-P} develops out of the capacitor. These two voltages are written as Equation 20:

$$\Delta V_{ESR} = I_{PP} \cdot ESR \quad \text{(EQ. 20)}$$

and Equation 21:

$$\Delta V_C = \frac{I_{PP}}{8 \cdot C_O \cdot F_{SW}} \quad \text{(EQ. 21)}$$

If the output of the converter has to support a load with high pulsating current, several capacitors will need to be paralleled to reduce the total ESR until the required V_{P-P} is achieved. The inductance of the capacitor can cause a brief voltage dip if the load transient has an extremely high slew rate. Low inductance capacitors should be considered in this scenario. A capacitor dissipates heat as a function of RMS current and frequency. Be sure that I_{P-P} is shared by a sufficient quantity of paralleled capacitors so that they operate below the maximum rated RMS current at F_{SW}. Take into account that the rated value of a capacitor can fade as much as 50% as the DC voltage across it increases.

Selection of the Input Capacitor

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and capable of supplying the RMS current required by the switching circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a preferred rating. Figure 28 is a graph of the input capacitor RMS ripple current, normalized relative to output load current, as a function of duty cycle and is adjusted for converter efficiency. The normalized RMS ripple current calculation is written as Equation 22:

$$I_{C_{IN}(RMS,NORMALIZED)} = \frac{I_{MAX} \cdot \sqrt{D \cdot (1-D) + \frac{D \cdot k^2}{12}}}{I_{MAX}} \quad \text{(EQ. 22)}$$

Where:

- I_{MAX} is the maximum continuous I_{LOAD} of the converter
- k is a multiplier (0 to 1) corresponding to the inductor peak-to-peak ripple amplitude expressed as a percentage of I_{MAX} (0% to 100%)
- D is the duty cycle that is adjusted to take into account the efficiency of the converter which is written as:

$$D = \frac{V_{OUT}}{V_{IN} \cdot EFF} \quad \text{(EQ. 23)}$$

In addition to the bulk capacitance, some low ESL ceramic capacitance is recommended to decouple between the drain of the high-side MOSFET and the source of the low-side MOSFET.

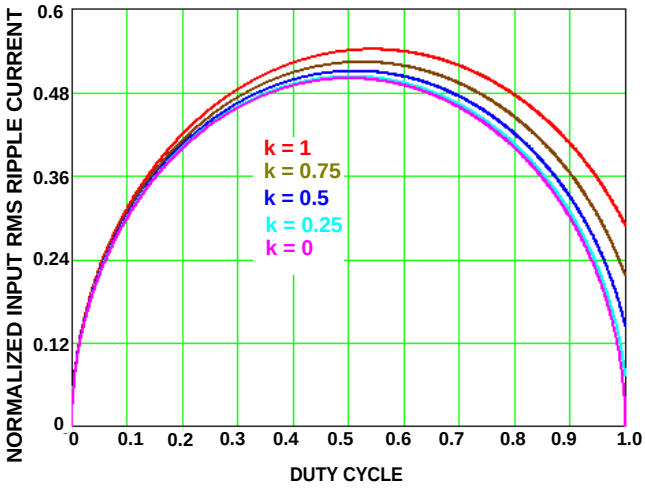


FIGURE 28. NORMALIZED RMS INPUT CURRENT @ EFF = 1

MOSFET Selection and Considerations

Typically, a MOSFET cannot tolerate even brief excursions beyond their maximum drain to source voltage rating. The MOSFETs used in the power stage of the converter should have a maximum V_{DS} rating that exceeds the sum of the upper voltage tolerance of the input power source and the voltage spike that occurs when the MOSFET switches off.

There are several power MOSFETs readily available that are optimized for DC/DC converter applications. The preferred high-side MOSFET emphasizes low gate charge so that the device spends the least amount of time dissipating power in the linear region. Unlike the low-side MOSFET which has the drain-source voltage clamped by its body diode during turn off, the high-side MOSFET turns off with a V_{DS} of approximately V_{IN} - V_{OUT}, plus the spike across it. The preferred low-side MOSFET emphasizes low $r_{DS(ON)}$ when fully saturated to minimize conduction loss. It should be noted that this is an optimal configuration of MOSFET selection for low duty cycle applications (D < 50%). For higher output, low input voltage solutions, a more balanced MOSFET selection for high- and low-side devices may be warranted.

For the low-side (LS) MOSFET, the power loss can be assumed to be conductive only and is written as Equation 24:

$$P_{CON\_LS} \approx I_{LOAD}^2 \cdot r_{DS(ON)\_LS} \cdot (1-D) \quad \text{(EQ. 24)}$$

For the high-side (HS) MOSFET, the its conduction loss is written as Equation 25:

$$P_{CON\_HS} = I_{LOAD}^2 \cdot r_{DS(ON)\_HS} \cdot D \quad \text{(EQ. 25)}$$

For the high-side MOSFET, the switching loss is written as Equation 26:

$$P_{SW\_HS} = \frac{V_{IN} \cdot I_{VALLEY} \cdot t_{ON} \cdot f_{SW}}{2} + \frac{V_{IN} \cdot I_{PEAK} \cdot t_{OFF} \cdot f_{SW}}{2} \quad \text{(EQ. 26)}$$

Where:

- I_{VALLEY} is the difference of the DC component of the inductor current minus 1/2 of the inductor ripple current
- I_{PEAK} is the sum of the DC component of the inductor current plus 1/2 of the inductor ripple current
- t_{ON} is the time required to drive the device into saturation
- t_{OFF} is the time required to drive the device into cut-off

Selecting The Bootstrap Capacitor

The selection of the bootstrap capacitor is written as Equation 27:

$$C_{BOOT} = \frac{Q_g}{\Delta V_{BOOT}} \quad \text{(EQ. 27)}$$

Where:

- Q_g is the total gate charge required to turn on the high-side MOSFET
- ΔV_{BOOT}, is the maximum allowed voltage decay across the boot capacitor each time the high-side MOSFET is switched on

As an example, suppose the high-side MOSFET has a total gate charge Q_g, of 25nC at V_{GS} = 5V, and a ΔV_{BOOT} of 200mV. The calculated bootstrap capacitance is 0.125µF; for a comfortable margin, select a capacitor that is double the calculated capacitance. In this example, 0.22µF will suffice. Use an X7R or X5R ceramic capacitor.

Layout Considerations

As a general rule, power should be on the bottom layer of the PCB and weak analog or logic signals are on the top layer of the PCB. The ground-plane layer should be adjacent to the top layer to provide shielding. The ground plane layer should have an island located under the IC, the compensation components, and the FSET components. The island should be connected to the rest of the ground plane layer at one point.

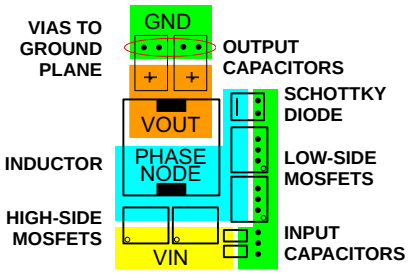


FIGURE 29. TYPICAL POWER COMPONENT PLACEMENT

Because there are two SMPS outputs and only one PGND pin, the power train of both channels should be laid out symmetrically. The line of bilateral symmetry should be drawn through pins 4 and 21 (pins 4 and 18 for ISL62383). This layout approach ensures that the controller does not favor one channel over another during critical switching decisions. Figure 30 illustrates one example of how to achieve proper bilateral symmetry.

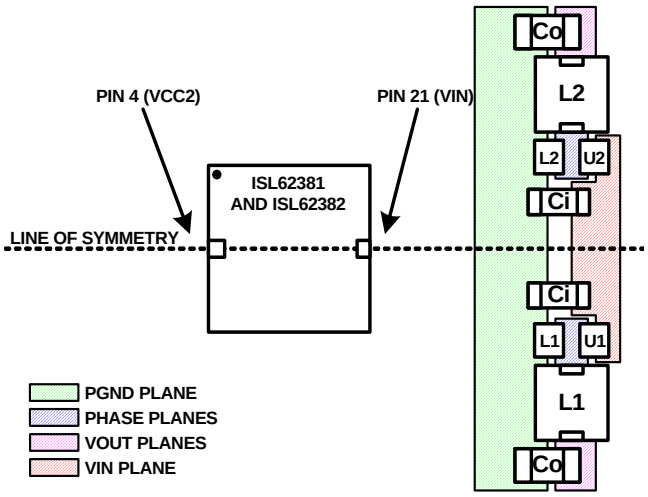


FIGURE 30. SYMMETRIC LAYOUT GUIDE

Signal Ground and Power Ground

The bottom of these controllers TQFN package is the signal ground (GND) terminal for analog and logic signals of the IC. Connect the GND pad of these controllers to the island of ground plane under the top layer using several vias for a robust thermal and electrical conduction path. Connect the input capacitors, the output capacitors, and the source of the lower MOSFETs to the power ground (PGND) plane.

The following pin descriptions use ISL62381 as an example.

PGND (Pin 23)

This is the return path for the pull-down of the LGATE low-side MOSFET gate driver. Ideally, PGND should be connected to the source of the low-side MOSFET with a low-resistance, low-inductance path.

VIN (Pin 21)

The VIN pin should be connected close to the drain of the high-side MOSFET, using a low resistance and low inductance path.

VCC (Pins 4 and 5)

For best performance, place the decoupling capacitor very close to the VCC and GND pins.

LDO5 (Pin 22)

For best performance, place the decoupling capacitor very close to the LDO5 and respective PGND pin, preferably on the same side of the PCB as the ISL62381 IC.

EN (Pins 13 and 28) and PGOOD (Pins 1 and 8)

These are logic signals that are referenced to the GND pin. Treat as a typical logic signal.

OCSET (Pins 12 and 29) and ISEN (Pins 11 and 30)

For DCR current sensing, current-sense network, consisting of R_{OCSET} and C_{SEN}, needs to be connected to the inductor pads for accurate measurement. Connect R_{OCSET} to the phase-node side pad of the inductor, and connect

C_{SEN} to the output side pad of the inductor. The ISEN resistor should also be connected to the output pad of the inductor with a separate trace. Connect the OCSET pin to the common node of node of R_{OCSET} and C_{SEN}.

For resistive current sensing, connect R_{OCSET} from the OCSET pin to the inductor side of the resistor pad. The ISEN resistor should be connected to the V_{OUT} side of the resistor pad.

In both current-sense configurations, the resistor and capacitor sensing elements, with the exclusion of the current sense power resistor, should be placed near the corresponding IC pin. The trace connections to the inductor or sensing resistor should be treated as Kelvin connections.

FB (Pins 9 and 32), and VOUT (Pins 10 and 31)

The VOUT pin is used to generate the R^3 synthetic ramp voltage and for soft-discharge of the output voltage during shutdown events. This signal should be routed as close to the regulation point as possible. The input impedance of the FB pin is high, so place the voltage programming and loop compensation components close to the VOUT, FB, and GND pins keeping the high impedance trace short.

FSET (Pins 2 and 7)

These pins require a quiet environment. The resistor R_{FSET} and capacitor C_{FSET} should be placed directly adjacent to these pins. Keep fast moving nodes away from these pins.

LGATE (Pins 17 and 24)

The signal going through these traces are both high dv/dt and high di/dt, with high peak charging and discharging current. Route these traces in parallel with the trace from the PGND pin. These two traces should be short, wide, and away from other traces. There should be no other weak signal traces in proximity with these traces on any layer.

BOOT (Pins 16 and 25), UGATE (Pins 15 and 26), and PHASE (Pins 14 and 27)

The signals going through these traces are both high dv/dt and high di/dt, with high peak charging and discharging current. Route the UGATE and PHASE pins in parallel with short and wide traces. There should be no other weak signal traces in proximity with these traces on any layer.

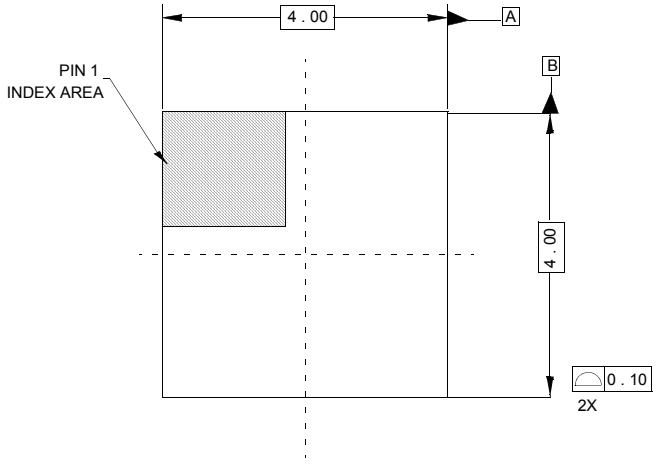
Copper Size for the Phase Node

The parasitic capacitance and parasitic inductance of the phase node should be kept very low to minimize ringing. It is best to limit the size of the PHASE node copper in strict accordance with the current and thermal management of the application. An MLCC should be connected directly across the drain of the upper MOSFET and the source of the lower MOSFET to suppress the turn-off voltage spike.

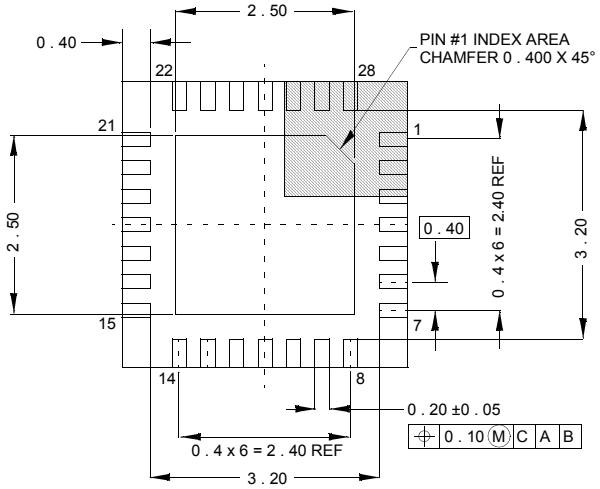
Package Outline Drawing

L28.4x4

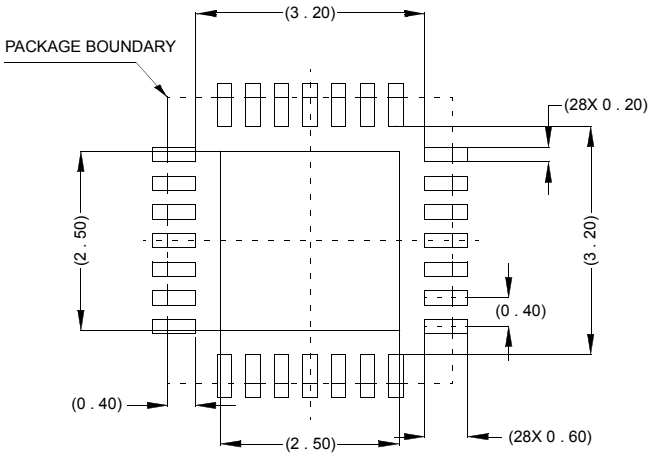
28 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 9/06



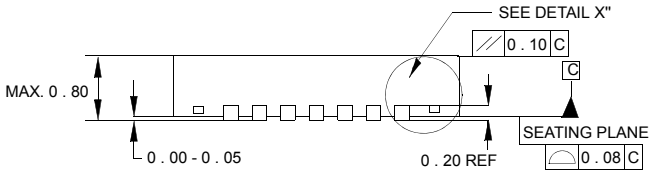
TOP VIEW



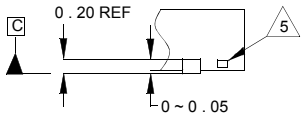
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW

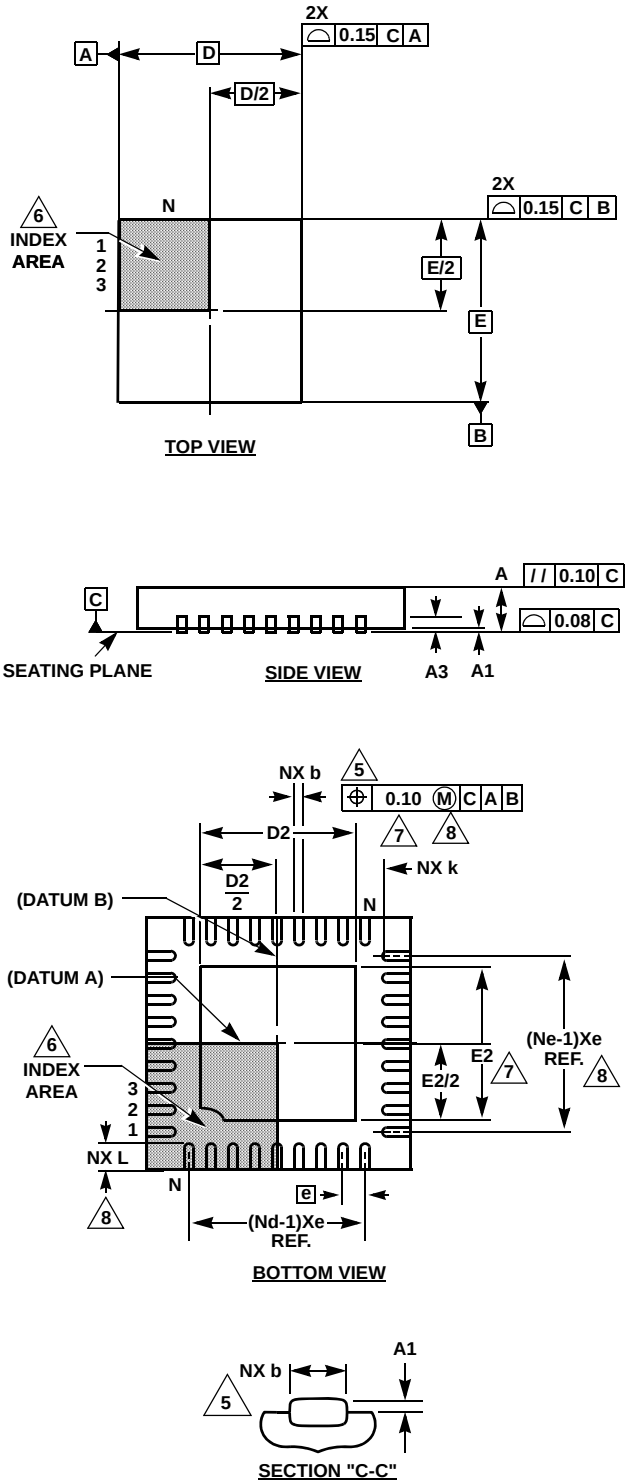


DETAIL "X"

NOTES:

1. Controlling dimensions are in mm.
   Dimensions in ( ) for reference only.
2. Unless otherwise specified, tolerance : Decimal ±0.05
   Angular ±2°
3. Dimensioning and tolerancing conform to AMSE Y14.5M-1994.
4. Bottom side Pin#1 ID is diepad chamfer as shown.
5. Tiebar shown (if present) is a non-functional feature.

Thin Quad Flat No-Lead Plastic Package (TQFN)
Thin Micro Lead Frame Plastic Package (TMLFP)



L32.5x5A

32 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220WJJD-1 ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.25	0.30	5, 8
D		5.00 BSC		-
D2	3.30	3.45	3.55	7, 8
E		5.00 BSC		-
E1		5.75 BSC		9
E2	3.30	3.45	3.55	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.30	0.40	0.50	8
N		32		2
Nd		8		3
Ne		8		3

Rev. 2 05/06

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.