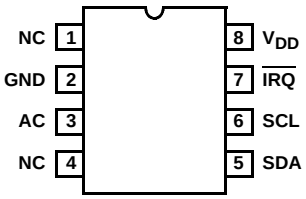
Low Power RTC with 50/60 Cycle AC Input, Alarms and Daylight Savings Correction

The ISL12030 device is a low power real time clock with 50/60 AC input for timing synchronization, clock/calendar registers, single periodic or polled alarms. There are 128 bytes of user SRAM.

The oscillator uses a 50/60 cycle sine wave input. The real time clock tracks time with separate registers for hours, minutes, and seconds. The calendar registers contain the date, month, year, and day of the week. The calendar is accurate through year 2100, with automatic leap year correction and auto daylight savings correction.

Pinout

ISL12030
(8 LD SOIC)
TOP VIEW



Features

- 50/60 Cycle AC as a Primary Clock Input for RTC Timing
- Real Time Clock/Calendar
  - Tracks Time in Hours, Minutes, Seconds and tenths of a Second
  - Day of the Week, Day, Month and Year
- Auto Daylight Saving Time Correction
  - Programmable Forward and Backward Dates
- Dual Alarms with Hardware and Register Indicators
  - Hardware Single Event or Pulse Interrupt Mode
- 128 Bytes of User SRAM
- I^2C Interface
  - 400kHz Data Transfer Rate
- Pb-Free (RoHS Compliant)

Applications

- Utility Meters
- Control Applications
- Vending Machines
- White Goods
- Consumer Electronics

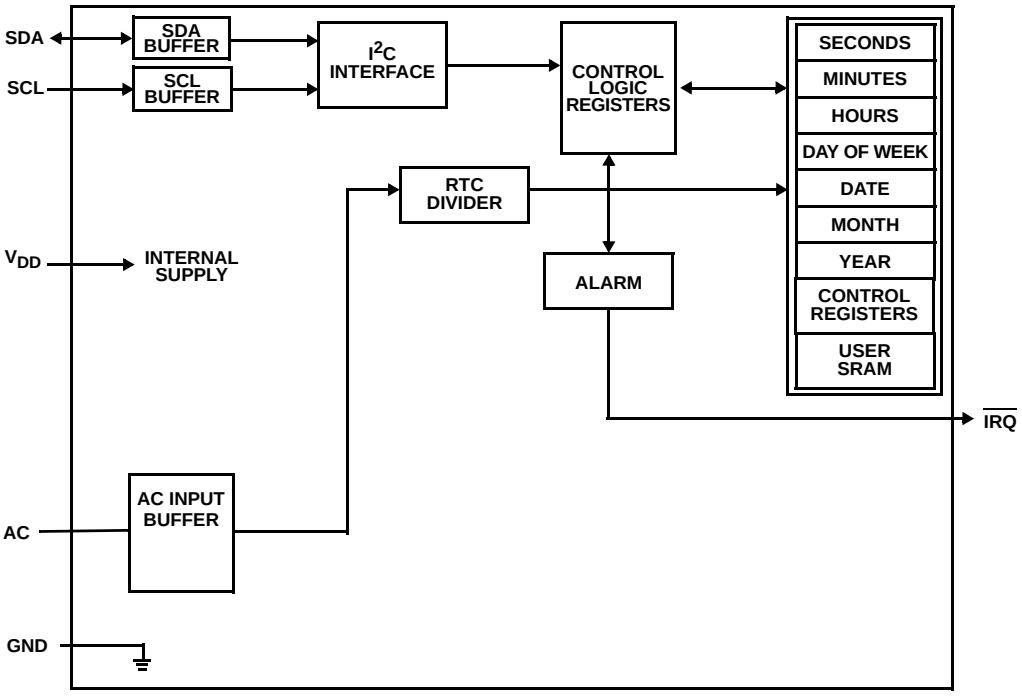
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	V_{DD} RANGE	TEMP RANGE (°C)	PACKAGE (Pb-Free)	PKG DWG #
ISL12030IBZ	12030 IBZ	2.7V to 5.5V	-40 to +85	8 Ld SOIC	M8.15

NOTE:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL12030. For more information on MSL please see techbrief TB363.

Block Diagram



Functional Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
2	GND	**Ground**.
3	AC	**AC Input**. The AC input pin accepts either 50Hz of 60Hz AC 2.5V_{P-P} sine wave signal.
5	SDA	**Serial Data**. SDA is a bi-directional pin used to transfer serial data into and out of the device. It has an open drain output and may be wire OR'ed with other open drain or open collector outputs.
6	SCL	**Serial Clock**. The SCL input is used to clock all serial data into and out of the device.
7	$\overline{IRQ}$	**Interrupt Output.** Open Drain active low output. Interrupt output pin to indicate alarm is triggered.
8	V_{DD}	Power supply.
1, 4	NC	**No Connection**. Do not connect to any electrical circuit, power or ground.

Absolute Maximum Ratings

Voltage on V_{DD}, SCL, SDA, AC, $\overline{IRQ}$ pins
(respect to ground) . . . . . -0.3V to 6.0V
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3014) . . . . .>2kV
Machine Model . . . . . .>200V

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} (°C/W)
8 Ld SOIC 120
Storage Temperature . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature (T_A) . . . . . .-40°C to +85°C
Supply Voltage (V_{DD}) . . . . . 2.7V to 5.5V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Operating Specifications

Specifications apply for: V_{DD} = 2.7V to 5.5V, T_A = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C** .

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 11)	TYP (Note 6)	MAX (Note 11)	UNITS	NOTES
V_{DD}	Main Power Supply		**2.7**		**5.5**	V	
I_{DD1}	Supply Current	V_{DD} = 5V, SCL, SDA = V_{DD}		27	**60**	µA	7
		V_{DD} = 3V, SCL, SDA = V_{DD}		16	**45**	µA	7
I_{DD2}	Supply Current (I^2C Communications Active)	V_{DD} = 5V		43	**75**	µA	5, 7
I_{DD3}	Supply Current for Timekeeping at AC Input	V_{DD} = 5.5V at T_A = +25°C		9.0	18.0	µA	5, 7
I_{LI}	Input Leakage Current on SCL				**1**	µA	
I_{LO}	I/O Leakage Current on SDA				**1**	µA	
$\overline{IRQ}$ (OPEN DRAIN OUTPUT)							
V_{OL}	Output Low Voltage	V_{DD} = 5V, I_{OL} = 3mA			**0.4**	V	
		V_{DD} = 2.7V, I_{OL} = 1mA			**0.4**	V	

Power-Down Timing

Specifications apply for: V_{DD} = 2.7 to 5.5V, T_A = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C** .

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 11)	TYP (Note 6)	MAX (Note 11)	UNITS	NOTES
$V_{DD\ SR-}$	V_{DD} Negative Slew Rate				**10**	V/ms	9

I^2C Interface Specifications

Specifications apply for: V_{DD} = 2.7 to 5.5V, T_A = -40°C to +85°C, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40°C to +85°C** .

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP (Note 6)	MAX (Note 11)	UNITS	NOTES
V_{IL}	SDA and SCL Input Buffer LOW Voltage		**-0.3**		**0.3 x V_{DD}**	V	
V_{IH}	SDA and SCL Input Buffer HIGH Voltage		**0.7 x V_{DD}**		**V_{DD} + 0.3**	V	
Hysteresis	SDA and SCL Input Buffer Hysteresis		**0.05 x V_{DD}**			V	
V_{OL}	SDA Output Buffer LOW Voltage, Sinking 3mA	V_{DD} = 5V, I_{OL} = 3mA			**0.4**	V	

I^2C Interface Specifications Specifications apply for: V_{DD} = 2.7 to 5.5V, T_A = -40℃ to +85℃, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40℃ to +85℃ . (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP (Note 6)	MAX (Note 11)	UNITS	NOTES
C_{PIN}	SDA and SCL Pin Capacitance	T_A = +25℃, f = 1MHz, V_{DD} = 5V, V_{IN} = 0V, V_{OUT} = 0V		10		pF	
f_{SCL}	SCL Frequency				**400**	kHz	
t_{IN}	Pulse Width Suppression Time at SDA and SCL Inputs	Any pulse narrower than the max spec is suppressed.			**50**	ns	
t_{AA}	SCL Falling Edge to SDA Output Data Valid	SCL falling edge crossing 30% of V_{DD}, until SDA exits the 30% to 70% of V_{DD} window.			**900**	ns	
t_{BUF}	Time the Bus Must be Free Before the Start of a New Transmission	SDA crossing 70% of V_{DD} during a STOP condition, to SDA crossing 70% of V_{DD} during the following START condition.	**1300**			ns	
t_{LOW}	Clock LOW Time	Measured at the 30% of V_{DD} crossing.	**1300**			ns	
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_{DD} crossing.	**600**			ns	
$t_{SU:STA}$	START Condition Setup Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_{DD}.	**600**			ns	
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_{DD} to SCL falling edge crossing 70% of V_{DD}.	**600**			ns	
$t_{SU:DAT}$	Input Data Setup Time	From SDA exiting the 30% to 70% of V_{DD} window, to SCL rising edge crossing 30% of V_{DD}.	**100**			ns	
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 30% of V_{DD} to SDA entering the 30% to 70% of V_{DD} window.	**0**		**900**	ns	
$t_{SU:STO}$	STOP Condition Setup Time	From SCL rising edge crossing 70% of V_{DD}, to SDA rising edge crossing 30% of V_{DD}.	**600**			ns	
$t_{HD:STO}$	STOP Condition Hold Time	From SDA rising edge to SCL falling edge. Both crossing 70% of V_{DD}.	**600**			ns	
t_{DH}	Output Data Hold Time	From SCL falling edge crossing 30% of V_{DD}, until SDA enters the 30% to 70% of V_{DD} window.	**0**			ns	
t_R	SDA and SCL Rise Time	From 30% to 70% of V_{DD}.	**20 + 0.1 x Cb**		**300**	ns	10
t_F	SDA and SCL Fall Time	From 70% to 30% of V_{DD}.	**20 + 0.1 x Cb**		**300**	ns	10
Cb	Capacitive loading of SDA or SCL	Total on-chip and off-chip	**10**		**400**	pF	10

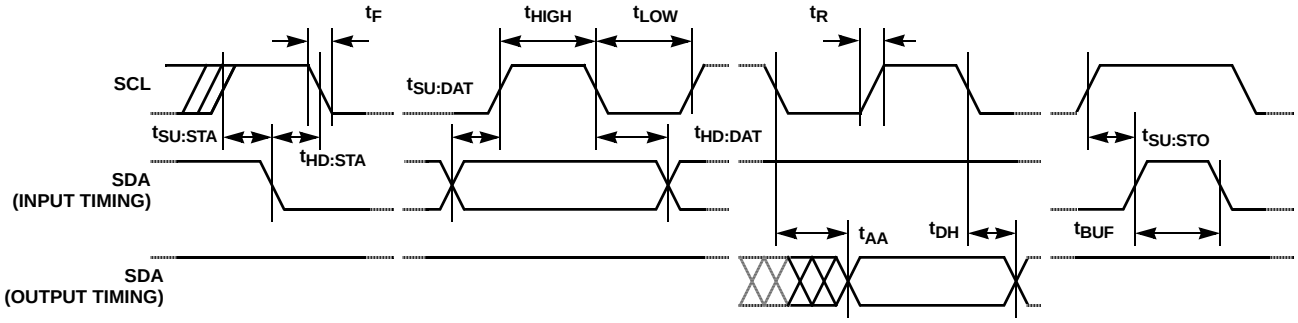
I^2C Interface Specifications Specifications apply for: V_{DD} = 2.7 to 5.5V, T_A = -40℃ to +85℃, unless otherwise stated. **Boldface limits apply over the operating temperature range, -40℃ to +85℃ . (Continued)**

SYMBOL	PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP (Note 6)	MAX (Note 11)	UNITS	NOTES
R_{PU}	SDA and SCL Bus Pull-up Resistor Off-chip	Maximum is determined by t_R and t_F. For Cb = 400pF, max is about 2kΩ. For Cb = 40pF, max is about 15kΩ	**1**			kΩ	10

NOTES:

5. $\overline{IRQ}$ Inactive.
6. Specified at T_A =+25℃.
7. F_{SCL} = 400kHz.
8. In order to ensure proper timekeeping, the $V_{DD\ SR-}$ specification must be followed.
9. Parameter is not 100% tested.
10. These are I^2C specific parameters and are not tested, however, they are used to set conditions for testing devices to validate specification.
11. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

SDA vs SCL Timing



Symbol Table

WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from LOW to HIGH	Will change from LOW to HIGH
	May change from HIGH to LOW	Will change from HIGH to LOW
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

EQUIVALENT AC OUTPUT LOAD CIRCUIT FOR V_{DD} = 5V

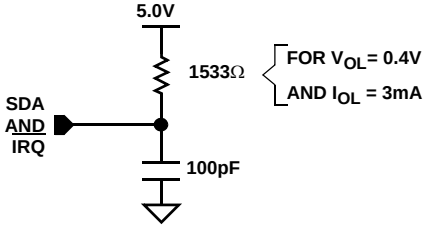


FIGURE 1. STANDARD OUTPUT LOAD FOR TESTING THE DEVICE WITH V_{DD} = 5.0V

General Description

The ISL12030 device is a low power real time clock with 50/60 AC input for timing synchronization, clock/calendar registers, single periodic or polled alarms. There are 128 bytes of user SRAM.

The oscillator uses a 50/60 cycle sine wave input. The real time clock tracks time with separate registers for hours, minutes and seconds. The calendar registers contain the date, month, year and day of the week. The calendar is accurate through year 2100, with automatic leap year correction and auto daylight savings correction.

The ISL12030's alarm can be set to any clock/calendar value for a match. Each alarm's status is available by checking the Status Register. The device also can be configured to provide a hardware interrupt via the $\overline{IRQ}$ pin. There is a repeat mode for the alarms allowing a periodic interrupt every minute, every hour, every day, etc.

The ISL12030 devices are specified for V_{DD} = 2.7V to 5.5V

Pin Descriptions

AC (AC Input)

The AC input is the main clock input for the real time clock. It can be either 50Hz or 60Hz, sine wave. The preferred amplitude is $2.5V_{P-P}$, although amplitudes >0.2 x V_{DD} are acceptable. An AC coupled (series capacitor) sine wave clock waveform is desired as the AC clock input provides DC biasing.

$\overline{IRQ}$ (Interrupt Output)

This pin provides an interrupt signal output. This signal notifies a host processor that an alarm has occurred and requests action. It is an open drain active LOW output.

Serial Clock (SCL)

The SCL input is used to clock all serial data into and out of the device. The input buffer on this pin is always active (not gated). It is disabled when the V_{DD} supply drops below 2.7V.

Serial Data (SDA)

SDA is a bi-directional pin used to transfer data into and out of the device. It has an open drain output and may be OR'ed with other open drain or open collector outputs. The input buffer is always active (not gated) in normal mode.

An open drain output requires the use of a pull-up resistor. The output circuitry controls the fall time of the output signal with the use of a slope controlled pull-down. The circuit is designed for 400kHz I^2C interface speeds.

V_{DD}, GND

Chip power supply and ground pins. The device will operate with a power supply from V_{DD} = 2.7V to 5.5VDC. A 0.1µF capacitor is recommended on the V_{DD} pin to ground.

Functional Description

Power Supply Operation

The ISL12030 will function with inputs from V_{DD} = 2.7V to 5.5VDC. If the V_{DD} supply should drop below this, operation to the specifications may be compromised, although the SRAM memory will hold its values until V_{DD} = 1.8V. Below that, the entire device is not guaranteed to operate or retain SRAM memory.

Power Failure Detection

The ISL12030 provides a Real Time Clock Failure Bit (RTCF) to detect total power failure. It allows users to determine if the device has powered up after having lost all power to the device (V_{DD} very near 0.0VDC).

Real Time Clock Operation

The Real Time Clock (RTC) maintains an accurate internal representation of tenths of a second, second, minute, hour, day of week, date, month and year. The RTC also has leap-year correction. The clock also corrects for months having fewer than 31 days and has a bit that controls 24 hour or AM/PM format. When the ISL12030 powers up after the loss of V_{DD}, the clock will not begin incrementing until at least one byte is written to the clock register.

Alarm Operation

The alarm mode is enabled via the MSB bit. Single event or interrupt alarm mode is selected via the IM bit. The standard alarm allows for alarms of time, date, day of the week, month and year. When a time alarm occurs in single event mode, the $\overline{IRQ}$ pin will be pulled low and the corresponding alarm status bit (ALM0 or ALM1) will be set to "1". The status bits can be written with a "0" to clear, or if the ARST bit is set, a single read of the SRDC status register will clear them.

The pulsed interrupt mode (setting the IM bit to "1") activates a repetitive or recurring alarm. Hence, once the alarm is set, the device will continue to output a pulse for each occurring match of the alarm and present time. The Alarm pulse will occur as often as every minute (if only the nth second is set) or as infrequently as once a year (if at least the nth month is set). During pulsed interrupt mode, the $\overline{IRQ}$ pin will be pulled LOW for 250ms and the alarm status bit (ALM0 or ALM1) will be set to "1".

General Purpose User SRAM

The ISL12030 provides 128 bytes of user SRAM. The SRAM is volatile and will be lost or corrupted if V_{DD} drops below 1.8V.

I^2C Serial Interface

The ISL12030 has an I^2C serial bus interface that provides access to the control and status registers and the user SRAM. The I^2C serial interface is compatible with other

industry I^2C serial bus protocols using a bi-directional data signal (SDA) and a clock signal (SCL).

Register Descriptions

The registers are accessible following an I^2C slave byte of "1101 111x" and reads or writes to addresses [00h:47h]. The defined addresses and default values are described in the Table 1. The general purpose SRAM has a different slave address (1010 111x), so it is not possible to read/write that section of memory while accessing the registers.

REGISTER ACCESS

The contents of the registers can be modified by performing a byte or a page write operation directly to any register address.

The registers are divided into 5 sections. They are:

1. Real Time Clock (8 bytes): Address 00h to 07h.
2. Status (1 bytes): Address 08h.
3. Control (2 bytes): 0Ch and 13h.
4. Day Light Saving Time (8 bytes): 15h to 1Ch
5. Alarm 0/1 (12 bytes):1Dh to 28h

Write capability is allowable into the RTC registers (00h to 07h) only when the WRTC bit (bit 6 of address 0Ch) is set to "1". **A multi-byte read or write operation is limited to one section per operation.** Access to another section requires a new operation. A read or write can begin at any address within the section.

A register can be read by performing a random read at any address at any time. This returns the contents of that register's location. Additional registers are read by performing a sequential read. For the RTC and Alarm registers, the read instruction latches all clock registers into a buffer, so an update of the clock does not change the time being read. At the end of a read, the master supplies a stop condition to end the operation and free the bus. After a read, the address remains at the previous address +1 so the user can execute a current address read and continue reading the next register.

It is only necessary to set the WRTC bit prior to writing into the RTC registers. All other registers are completely accessible without setting the WRTC bit.

TABLE 1. REGISTER MEMORY MAP (X indicates writes to these bits have no effect on the device)

ADDR	SECTION	REG NAME	BIT								RANGE	DEFAULT
			7	6	5	4	3	2	1	0		
00h	RTC	SC	0	SC22	SC21	SC20	SC13	SC12	SC11	SC10	0 to 59	00h
01h		MN	0	MN22	MN21	MN20	MN13	MN12	MN11	MN10	0 to 59	00h
02h		HR	MIL	0	HR21	HR20	HR13	HR12	HR11	HR10	0 to 23	00h
03h		DT	0	0	DT21	DT20	DT13	DT12	DT11	DT10	1 to 31	01h
04h		MO	0	0	0	MO20	MO13	MO12	MO11	MO10	1 to 12	01h
05h		YR	YR23	YR22	YR21	YR20	YR13	YR12	YR11	YR10	0 to 99	00h
06h		DW	0	0	0	0	0	DW2	DW1	DW0	0 to 6	00h
07h		SS	0	0	0	0	SS3	SS2	SS1	SS0	0 to 9	00h
08h	Status	SRDC	0	DSTADJ	ALM1	ALM0	0	0	0	RTCF	N/A	01h
0Ch	Control	INT	ARST	WRTC	IM	X	X	X	ALE1	ALE0	N/A	01h
13h		AC	AC5060	ACENB	X	X	X	X	X	X	N/A	00h
15h	DSTCR	DstMoFd	DSTE	0	0	MoFd20	MoFd13	MoFd12	MoFd11	MoFd10	1 to 12	04h
16h		DstDwFd	0	DwFdE	WkFd12	WkFd11	WkFd10	DwFd12	DwFd11	DwFd10	0 to 6	00h
17h		DstDtFd	0	0	DtFd21	DtFd20	DtFd13	DtFd12	DtFd11	DtFd10	1 to 31	01h
18h		DstHrFd	HrFdMIL	0	HrFd21	HrFd20	HrFd13	HrFd12	HrFd11	HrFd10	0 to 23	02h
19h		DstMoRv	0	0	0	MoRv20	MoRv13	MoRv12	MoRv11	MoRv10	1 to 12	10h
1Ah		DstDwRv	0	DwRvE	WkRv12	WkRv11	WkRv10	DwRv12	DwRv11	DwRv10	0 to 6	00h
1Bh		DstDtRv	0	0	DtRv21	DtRv20	DtRv13	DtRv12	DtRv11	DtRv10	1 to 31	01h
1Ch		DstHrRv	HrRvMIL	0	HrRv21	HrRv20	HrRv13	HrRv12	HrRv11	HrRv10	0 to 23	02h
1Dh	Alarm0	SCA0	ESCA0	SCA022	SCA021	SCA020	SCA013	SCA012	SCA011	SCA010	0 to 59	00h
1Eh		MNA0	EMNA0	MNA021	MNA020	MNA013	MNA012	MNA011	MNA011	MNA010	0 to 59	00h
1Fh		HRA0	EHRA0	0	HRA021	HRA020	HRA013	HRA012	HRA011	HRA010	0 to 23	00h
20h		DTA0	EDTA0	0	DTA021	DTA020	DTA013	DTA012	DTA011	DTA010	1 to 31	01h
21h		MOA0	EMOA0	0	0	MOA020	MOA013	MOA012	MOA011	MOA010	1 to 12	01h
22h		DWA0	EDWA0	0	0	0	0	DWA02	DWA01	DWA00	0 to 6	00h

TABLE 1. REGISTER MEMORY MAP (X indicates writes to these bits have no effect on the device) (Continued)

ADDR	SECTION	REG NAME	BIT 7	6	5	4	3	2	1	0	RANGE	DEFAULT
23h	Alarm1	SCA1	ESCA1	SCA122	SCA121	SCA120	SCA113	SCA112	SCA111	SCA110	0 to 59	00h
24h		MNA1	EMNA1	MNA122	MNA121	MNA120	MNA113	MNA112	MNA111	MNA110	0 to 59	00h
25h		HRA1	EHRA1	0	HRA121	HRA120	HRA113	HRA112	HRA111	HRA110	0 to 23	00h
26h		DTA1	EDTA1	0	DTA121	DTA120	DTA113	DTA112	DTA111	DTA110	1 to 31	01h
27h		MOA1	EMOA1	0	0	MOA120	MOA113	MOA112	MOA111	MOA110	1 to12	01h
28h		DWA1	EDWA1	0	0	0	0	DWA12	DWA11	DWA10	0 to 6	00h

Real Time Clock Registers

Addresses [00h to 07h]

RTC REGISTERS (SC, MN, HR, DT, MO, YR, DW, SS)

These registers depict BCD representations of the time. As such, SC (Seconds) and MN (Minutes) range from 0 to 59, HR (Hour) can be either 12-hour or 24-hour mode, DT (Date) is 1 to 31, MO (Month) is 1 to 12, YR (Year) is 0 to 99, DW (Day of the Week) is 0 to 6, and SS (Sub-Second) is 0 to 9. The Sub-Second register is read-only and will clear to “0” count each time there is a write to a register in the RTC section.

The DW register provides a Day of the Week status and uses three bits DW2 to DW0 to represent the seven days of the week. The counter advances in the cycle 0-1-2-3-4-5-6-0-1-2.... The assignment of a numerical value to a specific day of the week is arbitrary and may be decided by the system software designer. The default value is defined as “0”.

24 HOUR TIME

If the MIL bit of the HR register is “1”, the RTC uses a 24-hour format. If the MIL bit is “0”, the RTC uses a 12-hour format and HR21 bit functions as an AM/PM indicator with a “1” representing PM. The clock defaults to 12-hour format time with HR21 = “0”.

LEAP YEARS

Leap years add the day February 29 and are defined as those years that are divisible by 4. Years divisible by 100 are not leap years, unless they are also divisible by 400. This means that the year 2000 is a leap year and the year 2100 is not. The ISL12030 does not correct for the leap year in the year 2100.

Status Register (SR)

Address [08h]

The Status Registers consist of the DC and AC status registers (see Tables 2 and 3).

Status Register DC (SRDC)

The Status Register DC is located in the memory map at address 08h. This is a volatile register that provides status of RTC failure (RTCF), Alarm0 or Alarm1 trigger, and Daylight Saving Time adjustment.

TABLE 2. STATUS REGISTER DC (SRDC)

ADDR	7	6	5	4	3	2	1	0
08h	X	DSTADJ	ALM1	ALM0	X	X	X	RTCF

DAYLIGHT SAVING TIME ADJUSTMENT BIT (DSTADJ)

DSTADJ is the Daylight Saving Time Adjustment Bit. It indicates that daylight saving time adjustment has happened. The bit will be set to “1” when the Forward DST event has occurred. The bit will stay set until the Reverse DST event has happened. The bit will also reset to “0” when the DSTE bit is set to “0” (DST function disabled). The bit can be forced to “1” with a write to the Status Register. The default value for DSTADJ is “0”.

ALARM BITS (ALM0 AND ALM1)

These bits announce if an alarm matches the real time clock. If there is a match, the respective bit is set to “1”. This bit can be manually reset to “0” by the user or automatically reset by enabling the auto-reset bit (see ARST bit). A write to this bit in the SR can only set it to “0”, not “1”. An alarm bit that is set by an alarm occurring during an SR read operation will remain set after the read operation is complete.

REAL TIME CLOCK FAIL BIT (RTCF)

This bit is set to a “1” after a total power failure. This is a read only bit that is set by hardware (internally) when the device powers up after having lost all power (defined as V_{DD} = 0V). The bit is set as soon as V_{DD} is applied to the device. The first valid write to the RTC section after a complete power failure resets the RTCF bit to “0” (writing one byte is sufficient).

Control Registers

Addresses [0Ch to 13h]

The control registers (INT, AC) contain all the bits necessary to control the parametric functions on the ISL12030.

Interrupt Control Register (INT)

TABLE 3. INTERRUPT CONTROL REGISTER (INT)

ADDR	7	6	5	4	3	2	1	0
0Ch	ARST	WRTC	IM	X	X	X	ALE1	ALE0

AUTOMATIC RESET BIT (ARST)

This bit enables/disables the automatic reset of the ALM0 and ALM1 status bits only. When ARST bit is set to “1”, these status bits are reset to “0” after a valid read of the SRDC Register (with a valid STOP condition). When the ARST is cleared to “0”, the user must manually reset the ALM0 and ALM1 bits.

WRITE RTC ENABLE BIT (WRTC)

The WRTC bit enables or disables write capability into the RTC Register section. The factory default setting of this bit is “0”. Upon initialization or power-up, the WRTC must be set to “1” to enable the RTC. Upon the completion of a valid write (STOP), the RTC starts counting. The RTC internal 1Hz signal is synchronized to the STOP condition during a valid write cycle. This bit will remain set until reset to “0” or a complete power-down occurs (V_{DD} = 0.0V).

ALARM INTERRUPT MODE BIT (IM)

This bit enables/disables the interrupt mode of the alarm function. When the IM bit is set to “1”, the alarms will operate in the interrupt mode, where an active low pulse width of 250ms will appear at the $\overline{IRQ}$ pin when the RTC is triggered by either alarm as defined by the Alarm0 section (1Dh to 22h) or the Alarm1 section (23h to 28h). When the IM bit is

cleared to “0”, the alarm will operate in standard mode, where the $\overline{IRQ}$ pin will be set LOW until both the ALM0/ALM1 status bits are cleared to “0”.

ALARM 1 (ALE 1)

This bit enables the Alarm1 function. When ALE1 = “1”, a match of the RTC section with the Alarm1 section will result is setting the ALM1 status bit to “1” and the $\overline{IRQ}$ output LOW. When set to “0”, the Alarm1 function is disabled.

ALARM 0 (ALE 0)

This bit enables the Alarm0 function. When ALE0 = 1, a match of the RTC section with the Alarm1 section will result is setting the ALM0 status bit to “1” and the $\overline{IRQ}$ output LOW. When set to “0”, the Alarm0 function is disabled.

AC Register (AC)

Address [13h]

This register sets the parameters for the AC input.

TABLE 4. AC REGISTER

ADDR	7	6	5	4	3	2	1	0
13h	AC5060	X	X	X	X	X	X	X

AC 50/60HZ INPUT SELECT (AC5060)

This bit selects either 50Hz or 60Hz powerline AC clock input frequency. Setting this bit to “0” selects a 60Hz input (default). Setting this bit to “1” selects a 50Hz input.

DST Control Registers (DSTCR)

Address [15h to 1Ch]

8 bytes of control registers have been assigned for the Daylight Savings Time (DST) functions. DST beginning (set Forward) time is controlled by the registers DstMoFd, DstDwFd, DstDtFd, and DstHrFd. DST ending time (set Backward or Reverse) is controlled by DstMoRv, DstDwRv, DstDtRv and DstHrRv.

Tables 5 and 6 describe the structure and functions of the DSTCR.

DST FORWARD REGISTERS (15H TO 18H)

DSTE is the DST Enabling Bit located in bit 7 of register 15h (DstMoFdxx). Set DSTE = 1 will enable the DSTE function. Upon powering up for the first time, the DSTE bit defaults to “0”.

DST forward is controlled by the following DST Registers:

DstMoFd sets the Month that DST starts. The default value for the DST begin month is April (04h).

DstDwFd sets the Week and the Day of the Week that DST starts. DstDwFdE sets the priority of the Day of the Week over the Date. For DstDwFdE = 1, Day of the week is the priority. Note that Day of the week counts from 0 to 6, like the RTC registers. The default for the DST Forward Day of the Week is Sunday (00h).

WkFd controls the week of the month that the DST starts. When the day of week option is selected, the WkFd entry set the week in the month and the DwFd selects the day of the week. The range for WdFd is 1 to 5 and 7 with 7 being the last week. Default is 0 (OFF).

DstDtfd controls which Date DST begins. The default value for DST forward date is on the first date of the month (01h). DstDtFd is only effective if DwFdE = 0.

DstHrFd controls the hour that DST begins. It includes the MIL bit, which is in the corresponding RTC register. The RTC hour and DstHrFd registers need to match formats (Military or AM/PM) in order for the DST function to work. The default value for DST hour is 2:00AM (02h). The time is advanced from 2:00:00AM to 3:00:00AM for this setting.

DST REVERSE REGISTERS (19H TO 1CH)

DST end (reverse) is controlled by the following DST Registers:

DstMoRv sets the Month that DST ends. The default value for the DST end month is October (10h).

DstDwRv controls the Week and the Day of the Week that DST should end. The DwRvE bit sets the priority of the Day of the Week over the Date. For DwRvE = 1, Day of the week is the priority. Note that Day of the week counts from 0 to 6, like the RTC registers. The default for DST DwRv end is Sunday (00h).

WkRv controls the week of the month that the DST starts. When the day of week option is selected, the WkRv entry set the week in the month and the DwRv selects the day of the week. The range for WdRv is 1 to 5 and 7 with 7 being the last week. Default is 0 (OFF)

DstDtRv controls which Date DST ends. The default value for DST Date Reverse is on the first date of the month. The DstDtRv is only effective if the DwRvE = 0.

DstHrRv controls the hour that DST ends. It includes the MIL bit, which is in the corresponding RTC register. The RTC hour and DstHrRv registers need to match formats (Military or AM/PM) in order for the DST function to work. The default value sets the DST end at 2:00AM. The time is set back from 2:00:00AM to 1:00:00AM for this setting.

TABLE 5. DST FORWARD REGISTERS

ADDRESS	FUNCTION	7	6	5	4	3	2	1	0
15h	Month Forward	DSTE	0	0	MoFd20	MoFd13	MoFd12	MoFd11	MoFd10
16h	Day Forward	0	DwFdE	WkFd12	WkFd11	WkFd10	DwFd12	DwFd11	DwFd10
17h	Date Forward	0	0	DtFd21	DtFd20	DtFd13	DtFd12	DtFd11	DtFd10
18h	Hour Forward	HrFdMIL	0	HrFd21	HrFd20	HrFd13	HrFd12	HrFd11	HrFd10

TABLE 6. DST REVERSE REGISTERS

ADDRESS	NAME	7	6	5	4	3	2	1	0
19h	Month Reverse	0	0	0	MoRv20	MoRv13	MoRv12	MoRv11	MoRv10
1Ah	Day Reverse	0	DwRvE	WkRv12	WkRv11	WkRv10	DwRv12	DwRv11	DwRv10
1Bh	Date Reverse	0	0	DtRv21	DtRv20	DtRv13	DtRv12	DtRv11	DtRv10
1Ch	Hour Reverse	HrRvMIL	0	HrRv21	HrRv20	HrRv13	HrRv12	HrRv11	HrRv10

ALARM Registers (1Dh to 28h)

The alarm register bytes are set up identical to the RTC register bytes, except that the MSB of each byte functions as an enable bit (enable = “1”). These enable bits specify which alarm registers (seconds, minutes, etc.) are used to make the comparison. Note that there is no alarm byte for year.

The alarm function works as a comparison between the alarm registers and the RTC registers. As the RTC advances, the alarm will be triggered once a match occurs between the alarm registers and the RTC registers. Any one alarm register, multiple registers, or all registers can be enabled for a match.

There are two alarm operation modes: Single Event and periodic Interrupt Mode.

Single Event Mode is enabled by setting either ALE0 or ALE1 to 1, then setting bit 7 on any of the Alarm registers (ESCA... EDWA) to “1”, and setting the IM bit to “0”. This mode permits a one-time match between the Alarm registers and the RTC registers. Once this match occurs, the ALM bit is set to “1” and the $\overline{IRQ}$ output will be pulled LOW and will remain LOW until the ALM bit is reset. This can be done manually or by using the auto-reset feature. Since the $\overline{IRQ}$ output is shared by both alarms, they both need to be reset in order for the $\overline{IRQ}$ output to go HIGH.

Interrupt Mode is enabled by setting either ALE0 or ALE1 to 1, then setting bit 7 on any of the Alarm registers (ESCA... EDWA) to “1”, and setting the IM bit to “1”. Setting the IM bit to 1 puts both ALM0 and ALM1 into Interrupt mode. The $\overline{IRQ}$ output will now be pulsed each time an alarm occurs (either AL0 or AL1). This means that once the interrupt mode alarm is set, it will continue to alarm until it is reset.

To clear a single event alarm, the corresponding ALM0 or ALM1 bit in the SRDC register must be set to “0” with a write. Note that if the ARST bit is set to “1” (address 0Ch, bit 7), the ALM0 and ALM1 bits will automatically be cleared when the status register is read.

The $\overline{IRQ}$ output will be set by an alarm match for either ALM0 or ALM1.

Following are examples of both Single Event and periodic Interrupt Mode alarms.

Example 1

- Alarm set with single interrupt (IM = ”0”)
- A single alarm will occur on January 1 at 11:30am
- Set Alarm registers as follows:

ALARM REGISTER	BIT 7	6	5	4	3	2	1	0	HEX	DESCRIPTION
SCA0	0	0	0	0	0	0	0	0	00h	Seconds disabled
MNA0	1	0	1	1	0	0	0	0	B0h	Minutes set to 30, enabled
HRA0	1	0	0	1	0	0	0	1	91h	Hours set to 11, enabled
DTA0	1	0	0	0	0	0	0	1	81h	Date set to 1, enabled
MOA0	1	0	0	0	0	0	0	1	81h	Month set to 1, enabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

After these registers are set, an alarm will be generated when the RTC advances to exactly 11:30 a.m. on January 1 (after seconds changes from 59 to 00) by setting the ALM0 bit in the status register to “1” and also bringing the $\overline{IRQ}$ output LOW.

Example 2

- Pulsed interrupt once per minute (IM = ”1”)
- Interrupts at one minute intervals when the seconds register is at 30 seconds
- Set Alarm registers as follows:

ALARM REGISTER	BIT									DESCRIPTION
	7	6	5	4	3	2	1	0	HEX	
SCA0	1	0	1	1	0	0	0	0	B0h	Seconds set to 30, enabled
MNA0	0	0	0	0	0	0	0	0	00h	Minutes disabled
HRA0	0	0	0	0	0	0	0	0	00h	Hours disabled
DTA0	0	0	0	0	0	0	0	0	00h	Date disabled
MOA0	0	0	0	0	0	0	0	0	00h	Month disabled
DWA0	0	0	0	0	0	0	0	0	00h	Day of week disabled

Once the registers are set, the following waveform will be seen at $\overline{IRQ}$ as shown in Figure 2:

FIGURE 2. $\overline{IRQ}$ WAVEFORM

Note that the status register ALM0 bit will be set each time the alarm is triggered, but does not need to be read or cleared.

User Memory Registers (accessed by using Slave Address 1010111x)

Addresses [00h to 7Fh]

These registers are 128 bytes of user SRAM. Writes to this section do not need to be proceeded by setting the WRTC bit. Note that this memory, like the status and control registers, is volatile and will be lost or corrupted when V_{DD} drops below 1.8V.

I^2C Serial Interface

The ISL12030 supports a bi-directional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter and the receiving device as the receiver. The device controlling the transfer is the master and the device being controlled is the slave. The master always initiates data transfers and provides the clock for both transmit and receive operations. Therefore, the ISL12030 operates as a slave device in all applications.

All communication over the I^2C interface is conducted by sending the MSB of each byte of data first.

Protocol Conventions

Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 3). On power-up of the ISL12030, the SDA pin is in the input mode.

All I^2C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The ISL12030 continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition is met (see Figure 3). A START condition is ignored during the power-up sequence.

All I^2C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH (see Figure 3). A STOP condition at the end of a read operation or at the end of a write operation to memory only places the device in its standby mode.

An acknowledge (ACK) is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (See Figure 4).

The ISL12030 responds with an ACK after recognition of a START condition followed by a valid Identification Byte, and once again after successful receipt of an Address Byte. The ISL12030 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

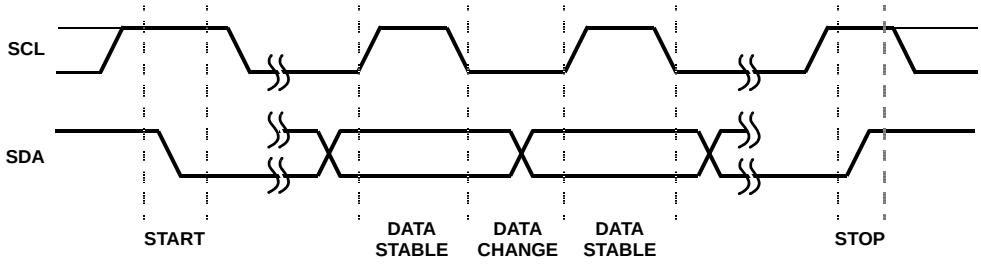


FIGURE 3. VALID DATA CHANGES, START AND STOP CONDITIONS

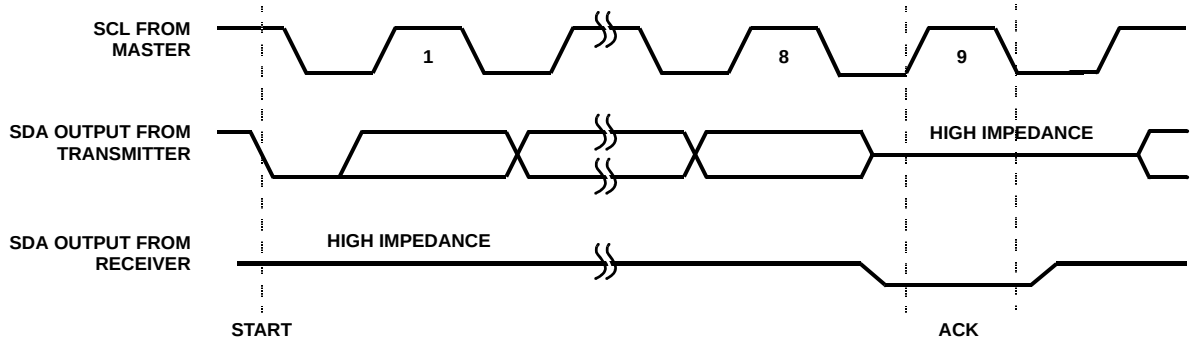


FIGURE 4. ACKNOWLEDGE RESPONSE FROM RECEIVER

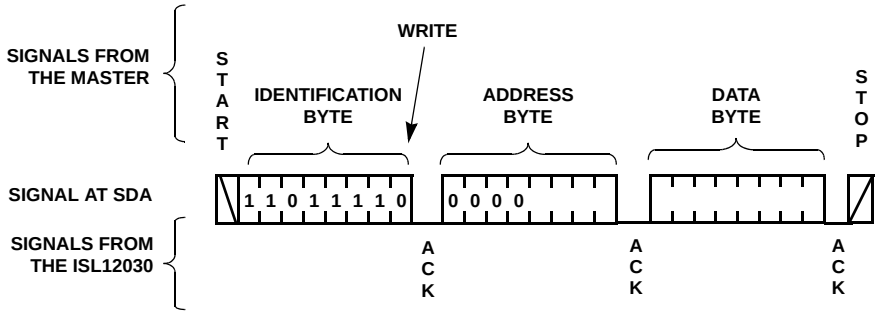


FIGURE 5. BYTE WRITE SEQUENCE (SLAVE ADDRESS FOR CSR SHOWN)

Device Addressing

Following a start condition, the master must output a Slave Address Byte. The 7 MSBs are the device identifier. These bits are “1101111b” for the RTC registers and “1010111b” for the User SRAM.

The last bit of the Slave Address Byte defines a read or write operation to be performed. When this R/$\overline{W}$ bit is a “1”, then a read operation is selected. A “0” selects a write operation (see Figure 6).

After loading the entire Slave Address Byte from the SDA bus, the ISL12030 compares the device identifier and device select bits with “1101111b” or “1010111b”. Upon a correct compare, the device outputs an acknowledge on the SDA line.

Following the Slave Byte is a one byte word address. The word address is either supplied by the master device or obtained from an internal counter. On power-up the internal address counter is set to address 00h, so a current address read starts at address 00h. When required, as part of a random read, the master must supply the 1 Word Address Byte as shown in Figure 6.

In a random read operation, the slave byte in the “dummy write” portion must match the slave byte in the “read” section. For a random read of the Control/Status Registers, the slave byte must be “1101111x” in both places.

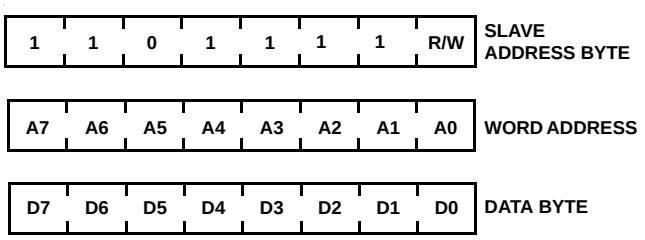


FIGURE 6. SLAVE ADDRESS, WORD ADDRESS AND DATA BYTES

Write Operation

A Write operation requires a START condition, followed by a valid Identification Byte, a valid Address Byte, a Data Byte, and a STOP condition. After each of the three bytes, the ISL12030 responds with an ACK. At this time, the I^2C interface enters a standby state.

A multiple byte operation within a page is permitted. The Address Byte must have the start address, and the data bytes are sent in sequence after the address byte, with the ISL12030 sending an ACK after each byte. The page write is terminated with a STOP condition from the master. The pages within the ISL12030 do not support wrapping around for page read or write operations.

Read Operation

A Read operation consists of a three byte instruction followed by one or more Data Bytes (see Figure 7). The master initiates the operation issuing the following sequence: a START, the Identification byte with the $R\overline{W}$ bit set to “0”, an Address Byte, a second START, and a second Identification byte with the $R\overline{W}$ bit set to “1”. After each of the three bytes, the ISL12030 responds with an ACK. Then the ISL12030 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eighth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (see Figure 7).

The Data Bytes are from the memory location indicated by an internal pointer. This pointers initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the last memory location in a section or page, the master should issue a STOP. Bytes that are read at addresses higher than the last address in a section may be erroneous.

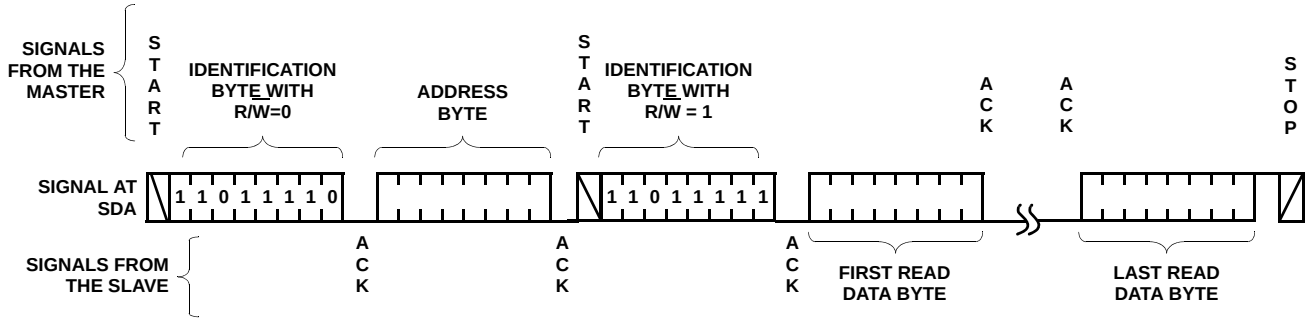


FIGURE 7. READ SEQUENCE (CSR SLAVE ADDRESS SHOWN)

Application Section

AC Input Circuits

The AC input ideally will have a $2.5V_{P-P}$ sine wave at the input, so this is the target for any signal conditioning circuitry for the 50/60Hz waveform. Note that the peak-to-peak amplitude can range from $1V_{P-P}$ up to V_{DD}, although it is best to keep the max signal level just below V_{DD}. The AC input provides DC offset so AC coupling with a series capacitor is advised.

If the AC power supply has a transformer, the secondary output can be used for clocking with a resistor divider and series AC coupling capacitor. A sample circuit is shown in Figure 8. Values for R_1/R_2 are chosen depending on the peak-to-peak range on the secondary voltage in order to match the input of the ISL12030. C_{IN} can be sized to pass up to 300Hz or so, and in most cases, 0.47µF should be the selected value for a ±20% tolerance device.

The AC input to the ISL12030 can be damaged if subjected to a normal AC waveform when V_{DD} is powered down. This can happen in circuits where there is a local LDO or power switch for placing circuitry in standby, while the AC main is still switched ON. Figure 8 shows a modified version of the Figure 9 circuit, which uses an emitter follower to essentially turn off the AC input waveform if the V_{DD} supply goes down.

Adding a Super Capacitor Backup

Since any loss of V_{DD} power will reset the SRAM memory including control and RTC register sections, then having some form of V_{DD} backup is a good idea. Figure 10 shows connections for a super capacitor backup using V_{DD} for the normal source and a signal diode for charging. Be careful not to use a normal Schottky diode as the leakage will greatly reduce the backup life of the super capacitor.

This form of backup should yield at least one full day of backup time, assuming the SCL/SDA pins and their pull-ups are pulled to ground on powerdown.

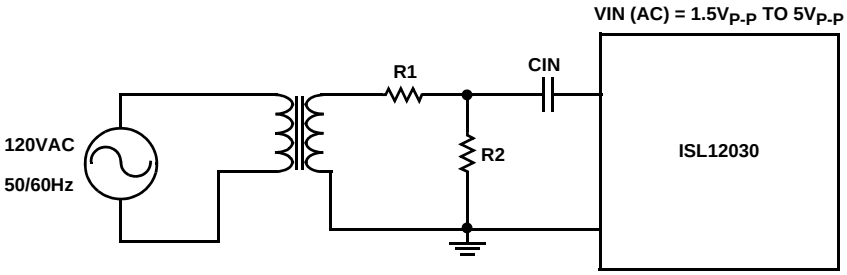


FIGURE 8. AC INPUT USING A TRANSFORMER SECONDARY

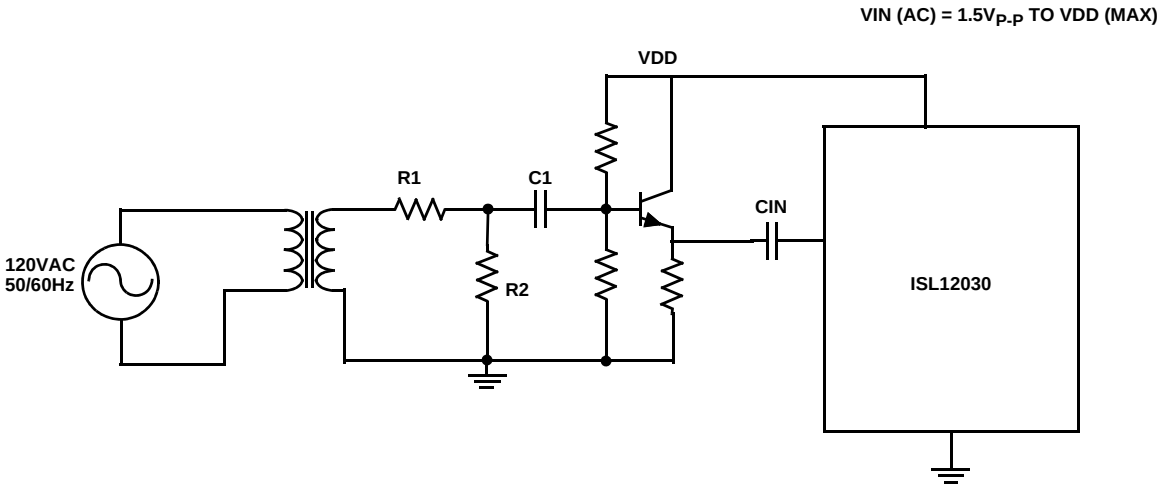


FIGURE 9. USING THE V_{DD} SUPPLY TO GATE THE AC INPUT

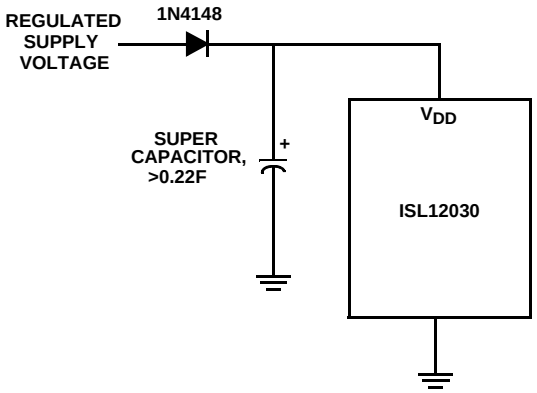


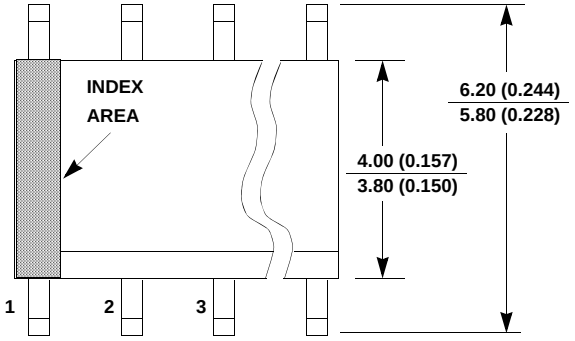
FIGURE 10. ADDING A SUPER CAPACITOR TO PROVIDE BACKUP FOR SRAM

Package Outline Drawing

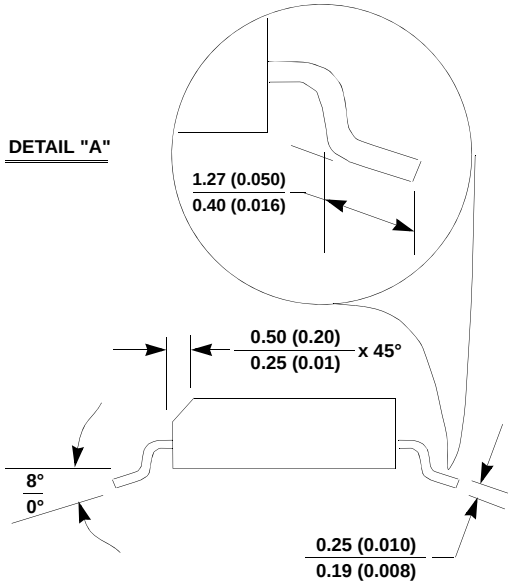
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

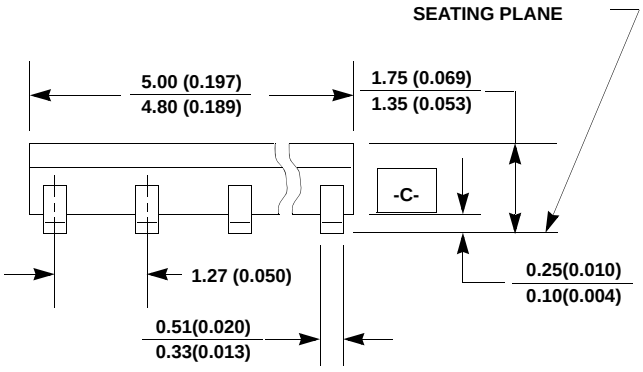
Rev 3, 3/11



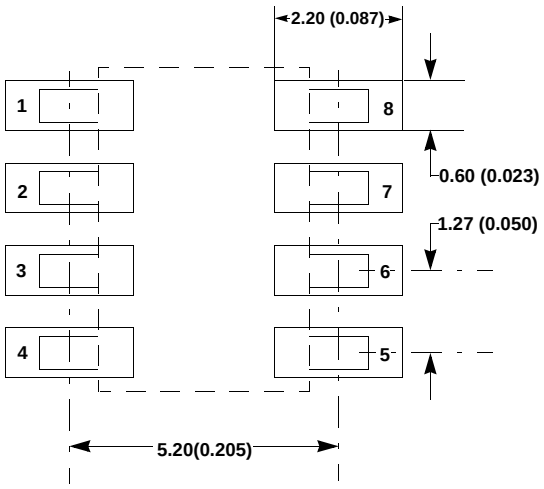
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.