## Ultra Low ON-Resistance, +1.65V to +4.5V, Single Supply, Quad SPDT (Dual DPDT) Analog Switch

The Intersil ISL8499 device is a low ON-Resistance, low voltage, bidirectional, Quad SPDT (Dual DPDT) analog switch designed to operate from a single +1.65V to +4.5V supply. Targeted applications include battery powered equipment that benefit from low $r_{ON}$ (0.24$\Omega$) and fast switching speeds ($t_{ON}$ = 15ns, $t_{OFF}$ = 13ns). The digital logic input is 1.8V logic-compatible when using a single +3V supply. With a supply voltage of 4.2V and logic high voltage of 2.85V at both logic inputs, the part draws only 10µA max of ICC current.

Cell phones, for example, often face ASIC functionality limitations. The number of analog input or GPIO pins may be limited and digital geometries are not well suited to analog switch performance. This part may be used to "mux-in" additional functionality while reducing ASIC design risk. The ISL8499 is offered in small form factor packages, alleviating board space limitations.

The ISL8499 consists of four SPDT switches. It is configured as a dual double-pole/double-throw (DPDT) device with two logic control inputs that control two SPDT switches each. The configuration can be used as a dual differential 2-to-1 multiplexer/demultiplexer. The ISL8499 is pin compatible with the STG3699 and DG2799.

### TABLE 1. FEATURES AT A GLANCE

| - | ISL8499 |
|---|---|
| Number of Switches | 4 |
| SW | Quad SPDT (Dual DPDT) |
| 4.3V $r_{ON}$ | 0.24$\Omega$ |
| 4.3V $t_{ON}/t_{OFF}$ | 15ns/13ns |
| 3.0V $r_{ON}$ | 0.26$\Omega$ |
| 3.0V $t_{ON}/t_{OFF}$ | 21ns/17ns |
| 1.8V $r_{ON}$ | 0.45$\Omega$ |
| 1.8V $t_{ON}/t_{OFF}$ | 51ns/43ns |
| Packages | 16 Ld 3x3 TQFN, 16 Ld 3x3 QFN, 16 Ld TSSOP |

## Features

- Drop in Replacement for the STG3699 and DG2799

- ON-Resistance ($r_{ON}$)
  - V+ = +4.3V . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.24$\Omega$
  - V+ = +3.0V . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.26$\Omega$
  - V+ = +1.8V . . . . . . . . . . . . . . . . . . . . . . . . . . . . 0.45$\Omega$

- $r_{ON}$ Matching between Channels . . . . . . . . . . . . . . . . . 0.04$\Omega$

- $r_{ON}$ Flatness Across Signal Range . . . . . . . . . . . . . . . 0.05$\Omega$

- Single Supply Operation . . . . . ̤. . . . . . . . +1.65V to +4.5V

- Low Power Consumption (PD) . . . . . . . . . . . . . . . . . <0.2µW

- Fast Switching Action (V+ = +4.3V)
  - $t_{ON}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 15ns
  - $t_{OFF}$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 13ns

- Guaranteed Break-Before-Make

- 1.8V Logic Compatible (+3V supply)

- Low ICC Current when VinH is not at the V+ Rail

- Available in 16 Ld 3x3 TQFN, 16 Ld 3x3 QFN and 16 Ld TSSOP

- ESD HBM Rating
  - COM Pins. . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 9kV
  - All Other Pins . . . . . . . . . . . . . . . . . . . . . . . . . . . . . 4kV

- Pb-Free Available (RoHS Compliant)

## Applications

- Battery Powered, Handheld, and Portable Equipment
  - Cellular/Mobile Phones
  - Pagers
  - Laptops, Notebooks, Palmtops

- Portable Test and Measurement

- Medical Equipment

- Audio and Video Switching

## Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

- Application Note AN557 "Recommended Test Procedures for Analog Switches"

## Pinouts (Note 1)

**ISL8499**
**(16 LD QFN TSSOP)**
TOP VIEW



**ISL8499**
**(16 LD 3X3 TQFN, 3X3 QFN)**
TOP VIEW
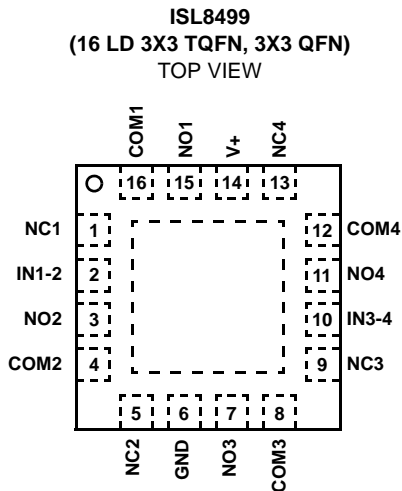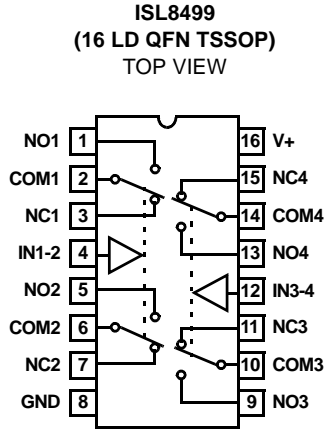


NOTE:

1. Switches Shown for Logic "0" Input.

## Truth Table

| LOGIC | NC SW | NO SW |
|-------|-------|-------|
| 0 | ON | OFF |
| 1 | OFF | ON |

NOTE: Logic "0" ≤0.5V. Logic "1" ≥1.4V with a 3V supply.

## Pin Descriptions

| PIN | FUNCTION |
|-----|----------|
| V+ | System Power Supply Input (+1.65V to +4.5V) |
| GND | Ground Connection |
| IN | Digital Control Input |
| COM | Analog Switch Common Pin |
| NO | Analog Switch Normally Open Pin |
| NC | Analog Switch Normally Closed Pin |

## Ordering Information

| PART NUMBER | PART MARKING | TEMP. RANGE (°C) | PACKAGE | PKG. DWG. # |
|-------------|--------------|------------------|---------|-------------|
| ISL8499IR | 499I | -40 to +85 | 16 Ld 3x3 QFN | L16.3x3 |
| ISL8499IR-T* | 499I | -40 to +85 | 16 Ld 3x3 QFN Tape and Reel | L16.3x3 |
| ISL8499IV | 8499 IV | -40 to +85 | 16 Ld TSSOP | M16.173 |
| ISL8499IV-T* | 8499 IV | -40 to +85 | 16 Ld TSSOP Tape and Reel | M16.173 |
| ISL8499IRZ (Note) | 499Z | -40 to +85 | 16 Ld 3x3 QFN (Pb-free) | L16.3x3 |
| ISL8499IRZ-T* (Note) | 499Z | -40 to +85 | 16 Ld 3x3 QFN Tape and Reel (Pb-free) | L16.3x3 |
| ISL8499IVZ (Note) | 8499 IVZ | -40 to +85 | 16 Ld TSSOP (Pb-free) | M16.173 |
| ISL8499IVZ-T* (Note) | 8499 IVZ | -40 to +85 | 16 Ld TSSOP Tape and Reel (Pb-free) | M16.173 |
| ISL8499IRTZ (Note) | 99TZ | -40 to +85 | 16 Ld 3x3 TQFN (Pb-free) | L16.3x3A |
| ISL8499IRTZ-T* (Note) | 99TZ | -40 to +85 | 16 Ld 3x3 TQFN Tape and Reel (Pb-free) | L16.3x3A |

*Please refer to TB347 for details on reel specifications

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

## Absolute Maximum Ratings

V+ to GND . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -0.3 to 4.7V
Input Voltages
  NO, NC, IN (Note 2) . . . . . . . . . . . . . . . . . . . -0.3 to ((V+) + 0.3V)
Output Voltages
  COM (Note 2) . . . . . . . . . . . . . . . . . . . . . . . . -0.3 to ((V+) + 0.3V)
Continuous Current NO, NC, or COM . . . . . . . . . . . . . . . . ±300mA
Peak Current NO, NC, or COM
  (Pulsed 1ms, 10% Duty Cycle, Max) . . . . . . . . . . . . . . . ±500mA
ESD Ratings:
  HBM $COM_X$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .>9kV
  HBM $NO_X$, $NC_X$, $IN_X$, V+, GND . . . . . . . . . . . . . . . . . . . . . . .>4kV
  MM $COM_X$ . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .>500V
  MM $NO_X$, $NC_X$, $IN_X$, V+, GND . . . . . . . . . . . . . . . . . . . . . . .>300V
  CDM . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . .>1kV

## Thermal Information

| Thermal Resistance (Typical, Note 3) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| TQFN and QFN Package (Notes 4, 5) . | 70 | 10 |
| TSSOP Package (Note 3) . . . . . . . . . | 150 | N/A |

Maximum Junction Temperature (Plastic Package). . . . . . . +150°C
Maximum Storage Temperature Range . . . . . . . . . . . -65°C to +150°C
Pb-Free Reflow Profile. . . . . . . . . . . . . . . . . . . . . . . . . .see link below
  http://www.intersil.com/pbfree/Pb-FreeReflow.asp

## Operating Conditions

Temperature Range
ISL8499IX . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . . -40°C to +85°C

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

2. Signals on NC, NO, IN, or COM exceeding V+ or GND are clamped by internal diodes. Limit forward diode current to maximum current ratings.

3. $\theta_{JA}$ is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

4. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.

5. For $\theta_{JC}$, the "case temp" location is the center of the exposed metal pad on the package underside.

**Electrical Specifications - 4.3V Supply**    Test Conditions:  V+ = +3.9V to +4.5V, GND = 0V, $V_{INH}$ = 1.6V, $V_{INL}$ = 0.5V (Note 6), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 8) | TYP | MAX (Notes 7, 8) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON-Resistance, $r_{ON}$ | V+ = 3.9V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+, (See Figure 5) | 25 | - | 0.25 | - | Ω |
| | | Full | - | 0.28 | - | Ω |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$ | V+ = 3.9V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = Voltage at max $r_{ON}$,(Note 11) | 25 | - | 0.04 | - | Ω |
| | | Full | - | 0.05 | - | Ω |
| $r_{ON}$ Flatness, $R_{FLAT(ON)}$ | V+ = 3.9V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+, (Note 9) | 25 | - | 0.05 | - | Ω |
| | | Full | - | 0.05 | - | Ω |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 4.5V, $V_{COM}$ = 0.3V, 3V, $V_{NO}$ or $V_{NC}$ = 3V, 0.3V | 25 | -50 | - | 50 | nA |
| | | Full | -150 | - | 150 | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 4.5V, $V_{COM}$ = 0.3V, 3V, or $V_{NO}$ or $V_{NC}$ = 0.3V, 3V, or Floating | 25 | -50 | - | 50 | nA |
| | | Full | -150 | - | 150 | nA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn-ON Time, $t_{ON}$ | V+ = 3.9V, $V_{NO}$ or $V_{NC}$ = 3.0V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 1, Note 10) | 25 | - | 15 | 25 | ns |
| | | Full | - | - | 30 | ns |
| Turn-OFF Time, $t_{OFF}$ | V+ = 3.9V, $V_{NO}$ or $V_{NC}$ = 3.0V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 1, Note 10) | 25 | - | 13 | 23 | ns |
| | | Full | - | - | 28 | ns |
| Break-Before-Make Time Delay, $t_D$ | V+ = 4.5V, $V_{NO}$ or $V_{NC}$ = 3.0V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 3, Note 10) | Full | 2 | 3 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω, (See Figure 2) | 25 | - | -120 | - | pC |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$, (See Figure 4) | 25 | - | 68 | - | dB |
| Crosstalk (Channel-to-Channel) | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$, (See Figure 6) | 25 | - | -98 | - | dB |

**Electrical Specifications - 4.3V Supply**  Test Conditions:  V+ = +3.9V to +4.5V, GND = 0V, $V_{INH}$ = 1.6V, $V_{INL}$ = 0.5V (Note 6), Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 8) | TYP | MAX (Notes 7, 8) | UNITS |
|---|---|---|---|---|---|---|
| Total Harmonic Distortion | f = 20Hz to 20kHz, $V_{COM}$ = 2$V_{PP}$, $R_L$ = 600$\Omega$ | 25 | - | 0.003 | - | % |
| NO or NC OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V, (See Figure 7) | 25 | - | 106 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V, (See Figure 7) | 25 | - | 212 | - | pF |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Power Supply Range | | Full | 1.65 | - | 4.5 | V |
| Positive Supply Current, I+ | V+ = +4.5V, $V_{IN}$ = 0V or V+ | 25 | - | - | 0.09 | $\mu$A |
| | | Full | - | - | 1.4 | $\mu$A |
| Positive Supply Current, I+ | V+ = +4.2V, $V_{IN}$ = 2.85V | 25 | - | - | 12 | $\mu$A |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage Low, $V_{INL}$ | | Full | - | - | 0.5 | V |
| Input Voltage High, $V_{INH}$ | | Full | 1.6 | - | - | V |
| Input Current, $I_{INH}$, $I_{INL}$ | V+ = 4.5V, $V_{IN}$ = 0V or V+, (Note 10) | Full | -0.5 | - | 0.5 | $\mu$A |

NOTES:

6. $V_{IN}$ = input voltage to perform proper function.

7. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.

8. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested.

9. Flatness is defined as the difference between maximum and minimum value of ON-Resistance over the specified analog signal range.

10. Limits established by characterization and are not production tested.

11. $r_{ON}$ matching between channels is calculated by subtracting the channel with the highest max $r_{ON}$ value from the channel with lowest max $r_{ON}$ value, between NC1 and NC2, NC3 and NC4 or between NO1 and NO2, NO3 and NO4.

**Electrical Specifications - 3V Supply**  Test Conditions:  V+ = +2.7V to +3.3V, GND = 0V, $V_{INH}$ = 1.4V, $V_{INL}$ = 0.5V (Note 6), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 8) | TYP | MAX (Notes 7, 8) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON-Resistance, $r_{ON}$ | V+ = 2.7V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+, (See Figure 5) | 25 | - | 0.3 | 0.45 | $\Omega$ |
| | | Full | - | - | 0.6 | $\Omega$ |
| $r_{ON}$ Matching Between Channels, $\Delta r_{ON}$ | V+ = 2.7V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = Voltage at max $r_{ON}$, (Note 11) | 25 | - | 0.04 | 0.08 | $\Omega$ |
| | | Full | - | - | 0.09 | $\Omega$ |
| $r_{ON}$ Flatness, $r_{FLAT(ON)}$ | V+ = 2.7V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+, (Note 9) | 25 | - | 0.06 | 0.15 | $\Omega$ |
| | | Full | - | - | 0.15 | $\Omega$ |
| NO or NC OFF Leakage Current, $I_{NO(OFF)}$ or $I_{NC(OFF)}$ | V+ = 3.3V, $V_{COM}$ = 0.3V, 3V, $V_{NO}$ or $V_{NC}$ = 3V, 0.3V | 25 | - | 1.2 | - | nA |
| | | Full | - | 13 | - | nA |
| COM ON Leakage Current, $I_{COM(ON)}$ | V+ = 3.3V, $V_{COM}$ = 0.3V, 3V, or $V_{NO}$ or $V_{NC}$ = 0.3V, 3V, or Floating | 25 | - | 1 | - | nA |
| | | Full | - | 35 | - | nA |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn-ON Time, $t_{ON}$ | V+ = 2.7V, $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ = 50$\Omega$, $C_L$ = 35pF, (See Figure 1, Note 10) | 25 | - | 21 | 30 | ns |
| | | Full | - | - | 35 | ns |
| Turn-OFF Time, $t_{OFF}$ | V+ = 2.7V, $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ = 50$\Omega$, $C_L$ = 35pF, (See Figure 1, Note 10) | 25 | - | 17 | 27 | ns |
| | | Full | - | - | 32 | ns |
| Break-Before-Make Time Delay, $t_D$ | V+ = 3.3V, $V_{NO}$ or $V_{NC}$ = 1.5V, $R_L$ = 50$\Omega$, $C_L$ = 35pF, (See Figure 3, Note 10) | Full | 2 | 3 | - | ns |

**Electrical Specifications - 3V Supply**  Test Conditions: V+ = +2.7V to +3.3V, GND = 0V, $V_{INH}$ = 1.4V, $V_{INL}$ = 0.5V (Note 6), Unless Otherwise Specified **(Continued)**

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 8) | TYP | MAX (Notes 7, 8) | UNITS |
|---|---|---|---|---|---|---|
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω, (See Figure 2) | 25 | - | -82 | - | pC |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$, (See Figure 4) | 25 | - | 68 | - | dB |
| Crosstalk (Channel-to-Channel) | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$, (See Figure 6) | 25 | - | -98 | - | dB |
| Total Harmonic Distortion | f = 20Hz to 20kHz, $V_{COM}$ = 2$V_{P-P}$, $R_L$ = 600Ω | 25 | - | 0.003 | - | % |
| NO or NC OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V, (See Figure 7) | 25 | - | 106 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V, (See Figure 7) | 25 | - | 212 | - | pF |
| **POWER SUPPLY CHARACTERISTICS** | | | | | | |
| Positive Supply Current, I+ | V+ = 3.6V, $V_{IN}$ = 0V or V+ | 25 | - | 0.025 | - | µA |
| | | Full | - | 0.715 | - | µA |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage Low, $V_{INL}$ | | Full | - | - | 0.5 | V |
| Input Voltage High, $V_{INH}$ | | Full | 1.4 | - | - | V |
| Input Current, $I_{INH}$, $I_{INL}$ | V+ = 3.6V, $V_{IN}$ = 0V or V+ (Note 10) | Full | -0.5 | - | 0.5 | µA |

**Electrical Specifications - 1.8V Supply**  Test Conditions: V+ = +1.65V to +2V, GND = 0V, $V_{INH}$ = 1.0V, $V_{INL}$ = 0.4V (Note 6), Unless Otherwise Specified

| PARAMETER | TEST CONDITIONS | TEMP (°C) | MIN (Notes 7, 8) | TYP | MAX (Notes 7, 8) | UNITS |
|---|---|---|---|---|---|---|
| **ANALOG SWITCH CHARACTERISTICS** | | | | | | |
| Analog Signal Range, $V_{ANALOG}$ | | Full | 0 | - | V+ | V |
| ON-Resistance, $r_{ON}$ | V+ = 1.8V, $I_{COM}$ = 100mA, $V_{NO}$ or $V_{NC}$ = 0V to V+, (See Figure 5) | 25 | - | 0.45 | 0.8 | Ω |
| | | Full | - | - | 0.85 | Ω |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| Turn-ON Time, $t_{ON}$ | V+ = 1.65V, $V_{NO}$ or $V_{NC}$ = 1.0V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 1, Note 10) | 25 | - | 51 | 65 | ns |
| | | Full | - | - | 70 | ns |
| Turn-OFF Time, $t_{OFF}$ | V+ = 1.65V, $V_{NO}$ or $V_{NC}$ = 1.0V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 1, Note 10) | 25 | - | 43 | 58 | ns |
| | | Full | - | - | 65 | ns |
| Break-Before-Make Time Delay, $t_D$ | V+ = 2.0V, $V_{NO}$ or $V_{NC}$ = 1.0V, $R_L$ = 50Ω, $C_L$ = 35pF, (See Figure 3, Note 10) | Full | 3 | 8 | - | ns |
| Charge Injection, Q | $C_L$ = 1.0nF, $V_G$ = 0V, $R_G$ = 0Ω, See Figure 2 | 25 | - | -44 | - | pC |
| OFF Isolation | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$, (See Figure 4) | 25 | - | 68 | - | dB |
| Crosstalk (Channel-to-Channel) | $R_L$ = 50Ω, $C_L$ = 5pF, f = 100kHz, $V_{COM}$ = 1$V_{RMS}$, (See Figure 6) | 25 | - | -98 | - | dB |
| NO or NC OFF Capacitance, $C_{OFF}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V, (See Figure 7) | 25 | - | 106 | - | pF |
| COM ON Capacitance, $C_{COM(ON)}$ | f = 1MHz, $V_{NO}$ or $V_{NC}$ = $V_{COM}$ = 0V, (See Figure 7) | 25 | - | 212 | - | pF |
| **DIGITAL INPUT CHARACTERISTICS** | | | | | | |
| Input Voltage Low, $V_{INL}$ | | Full | - | - | 0.4 | V |
| Input Voltage High, $V_{INH}$ | | Full | 1.0 | - | - | V |
| Input Current, $I_{INH}$, $I_{INL}$ | V+ = 2.0V, $V_{IN}$ = 0V or V+ (Note 10) | Full | -0.5 | - | 0.5 | µA |

# Test Circuits and Waveforms
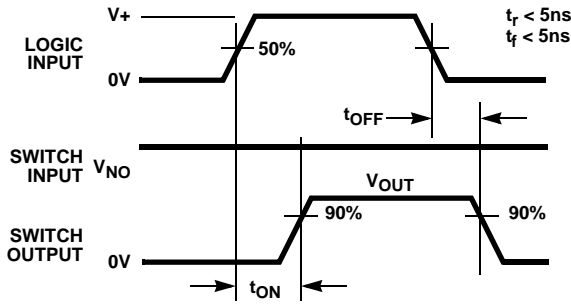


Logic input waveform is inverted for switches that have the opposite logic sense.

**FIGURE 1A. MEASUREMENT POINTS**



Repeat test for all switches. $C_L$ includes fixture and stray capacitance.

$$V_{OUT} = V_{(NO \text{ or } NC)} \frac{R_L}{R_L + r_{(ON)}}$$
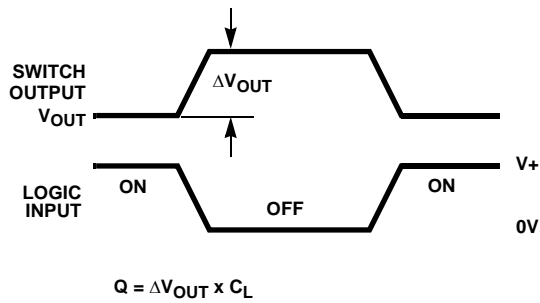
**FIGURE 1B. TEST CIRCUIT**

**FIGURE 1. SWITCHING TIMES**



$$Q = \Delta V_{OUT} \times C_L$$

**FIGURE 2A. MEASUREMENT POINTS**



**FIGURE 2B. TEST CIRCUIT**

**FIGURE 2. CHARGE INJECTION**
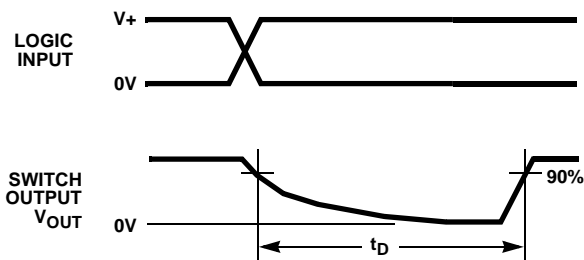


**FIGURE 3A. MEASUREMENT POINTS**



$C_L$ includes fixture and stray capacitance.

**FIGURE 3B. TEST CIRCUIT**

**FIGURE 3. BREAK-BEFORE-MAKE TIME**

## *Test Circuits and Waveforms* (Continued)
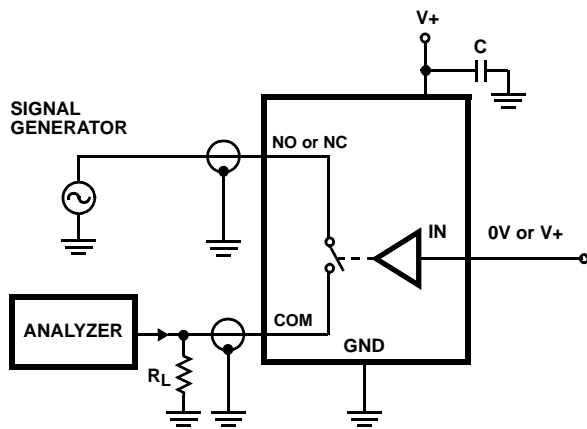


FIGURE 4. OFF ISOLATION TEST CIRCUIT
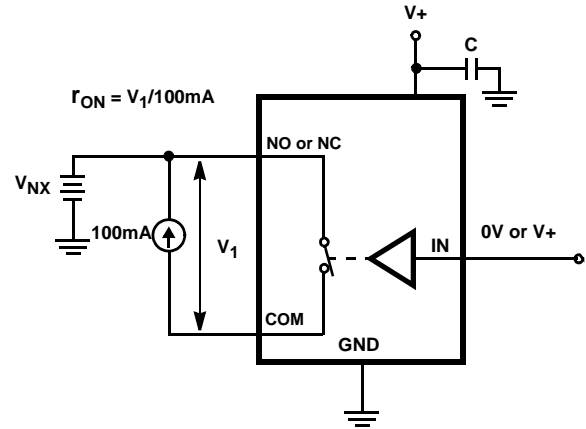


FIGURE 5. $r_{ON}$ TEST CIRCUIT
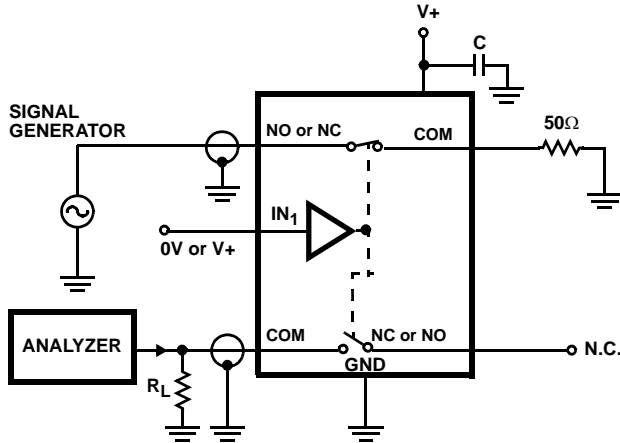


FIGURE 6. CROSSTALK TEST CIRCUIT
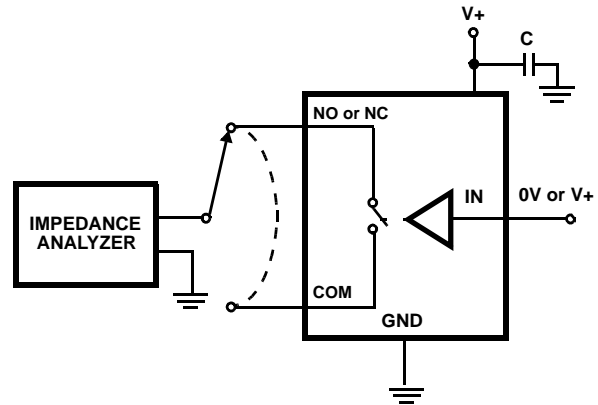


FIGURE 7. CAPACITANCE TEST CIRCUIT

## *Detailed Description*

The ISL8499 is a bidirectional, quad single pole/double throw (SPDT) analog switch that offers precise switching capability from a single 1.65V to 4.5V supply with low on-resistance (0.24Ω) and high speed operation ($t_{ON}$ = 15ns, $t_{OFF}$ = 13ns). The device is especially well suited for portable battery powered equipment due to its low operating supply voltage (1.65V), low power consumption (2.7µW max), low leakage currents (150nA max), and the tiny TQFN, QFN and TSSOP packages. The ultra low ON-Resistance and $r_{ON}$ flatness provide very low insertion loss and distortion to applications that require signal reproduction.

### *Supply Sequencing and Overvoltage Protection*

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents which might permanently damage the IC. All I/O pins contain ESD protection diodes from the pin to V+ and to GND (see Figure 8). To prevent forward biasing these diodes, V+ must be applied before any input signals, and the input signal voltages must remain between V+ and GND. If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input (see Figure 8). The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

This method is not acceptable for the signal path inputs. Adding a series resistor to the switch input defeats the purpose of using a low $r_{ON}$ switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 8). These

additional diodes limit the analog signal from 1V below V+ to 1V above GND. The low leakage current performance is unaffected by this approach, but the switch signal range is reduced and the resistance may increase, especially at low supply voltages.
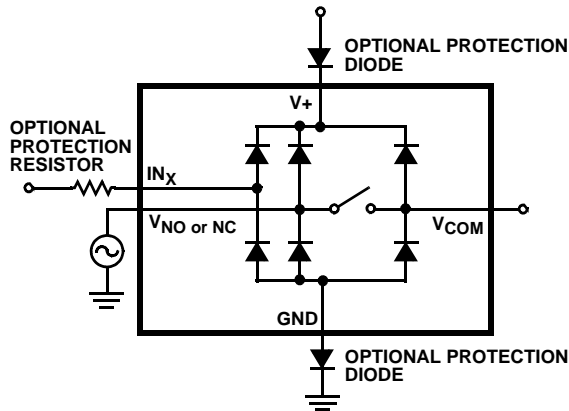


**FIGURE 8. OVERVOLTAGE PROTECTION**

### Power-Supply Considerations

The ISL8499 construction is typical of most single supply CMOS analog switches, in that they have two supply pins: V+ and GND. V+ and GND drive the internal CMOS switches and set their analog voltage limits. Unlike switches with a 4V maximum supply voltage, the ISL8499 4.7V maximum supply voltage provides plenty of room for the 10% tolerance of 4.3V supplies, as well as room for overshoot and noise spikes.

The minimum recommended supply voltage is 1.65V but will operate with a supply voltage below 1.5V. It is important to note that the input signal range, switching times, and on-resistance degrade at lower supply voltages. Refer to the "Electrical Specification" tables starting on page 3 and "Typical Performance" curves starting on page 6 for details.

V+ and GND also power the internal logic and level shiftiers. The level shiftiers convert the input logic levels to switched V+ and GND signals to drive the analog switch gate terminals.

This family of switches cannot be operated with bipolar supplies, because the input switching point becomes negative in this configuration.

### Logic-Level Thresholds

This switch family is 1.8V CMOS compatible (0.5V and 1.4V) over a supply range of 2.7V to 4.5V (see Figure 14). At 2.7V the $V_{IL}$ level is about 0.52V. This is still above the 1.8V CMOS guaranteed low output maximum level of 0.5V, but noise margin is reduced.

The digital input stages draw supply current whenever the digital input voltage is not at one of the supply rails. Driving the digital input signals from GND to V+ with a fast transition time minimizes power dissipation. The ISL8499 has been designed to minimize the supply current whenever the digital input voltage is not driven to the supply rails (0V to V+). For example driving the device with 2.85V logic (0V to 2.85V) while operating with a 4.2V supply the device draws only 6μA of current (see Figure 21 for VIN = 2.85V).

### High-Frequency Performance

In 50Ω systems, the signal response is reasonably flat even past 30MHz with a -3dB bandwidth of 104MHz (see Figure 17). The frequency response is very consistent over a wide V+ range, and for varying analog signal levels.

An OFF switch acts like a capacitor and passes higher frequencies with less attenuation, resulting in signal feedthrough from a switch's input to its output. Off Isolation is the resistance to this feedthrough, while Crosstalk indicates the amount of feedthrough from one switch to another. Figure 18 details the high Off Isolation and Crosstalk rejection provided by this part. At 100kHz, Off Isolation is about 68dB in 50Ω systems, decreasing approximately 20dB per decade as frequency increases. Higher load impedances decrease Off Isolation and Crosstalk rejection due to the voltage divider action of the switch OFF impedance and the load impedance.

### Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both V+ and GND. One of these diodes conducts if any analog signal exceeds V+ or GND.

Virtually all the analog leakage current comes from the ESD diodes to V+ or GND. Although the ESD diodes on a given signal pin are identical and therefore fairly well balanced, they are reverse biased differently. Each is biased by either V+ or GND and the analog signal. This means their leakages will vary as the signal varies. The difference in the two diode leakages to the V+ and GND pins constitutes the analog-signal-path leakage current. All analog leakage current flows between each pin and one of the supply terminals, not to the other switch terminal. This is why both sides of a given switch can show leakage currents of the same or opposite polarity. There is no connection between the analog signal paths and V+ or GND.

## Typical Performance Curves $T_A$ = +25°C, Unless Otherwise Specified
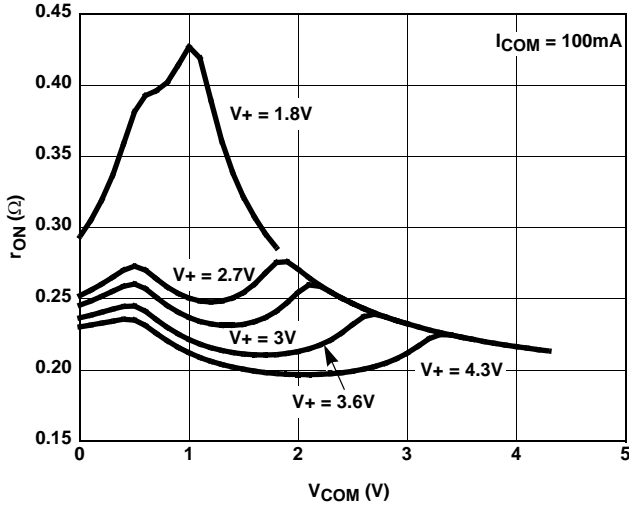


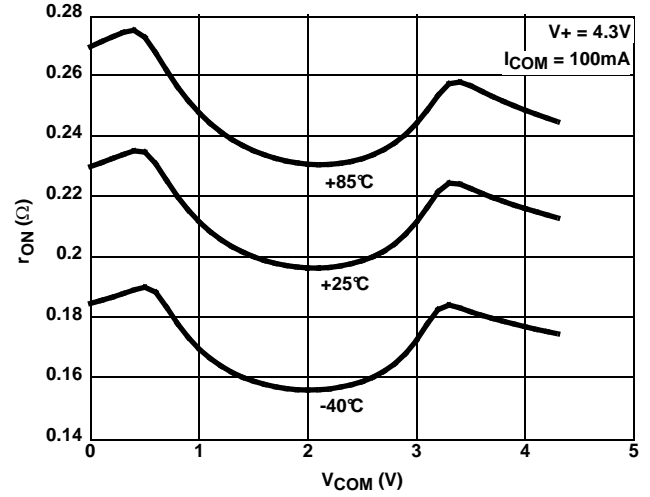FIGURE 9. ON-RESISTANCE vs SUPPLY VOLTAGE vs SWITCH VOLTAGE



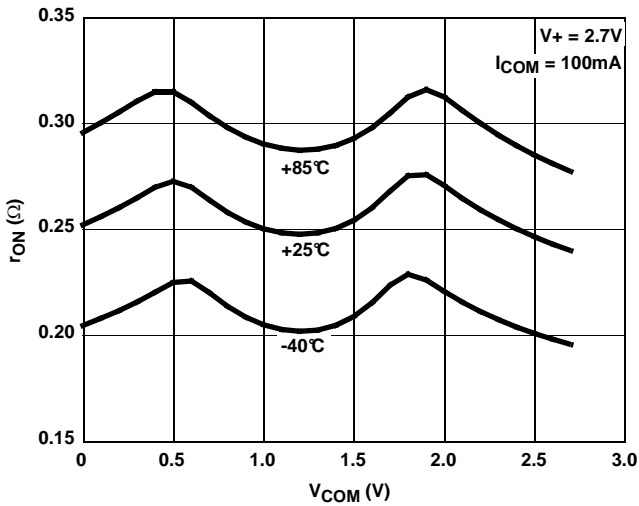FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE



FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE
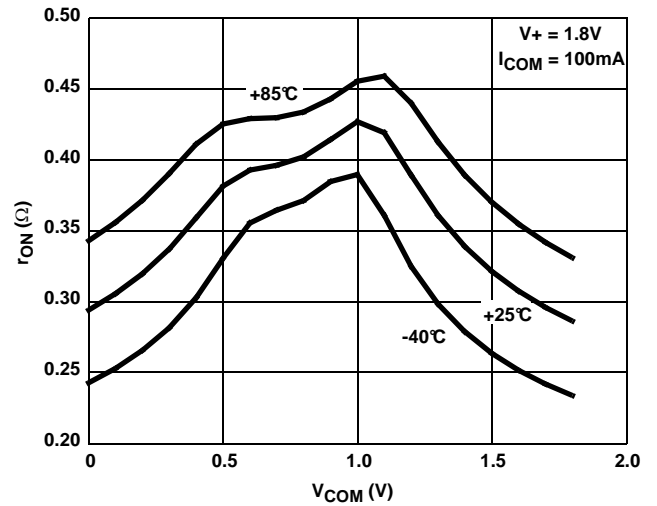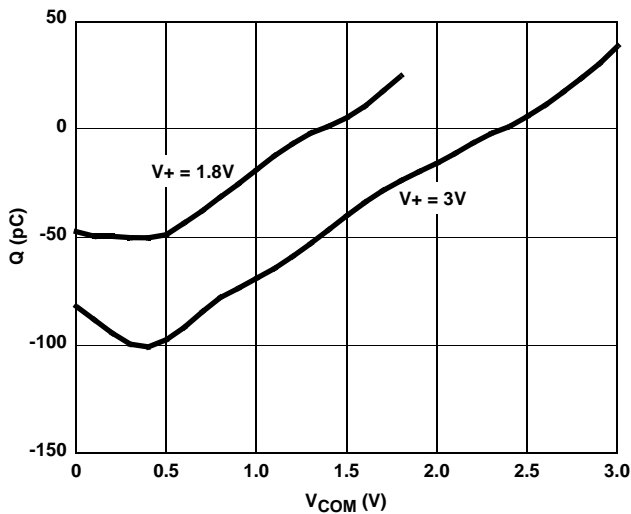


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE



FIGURE 13. CHARGE INJECTION vs SWITCH VOLTAGE



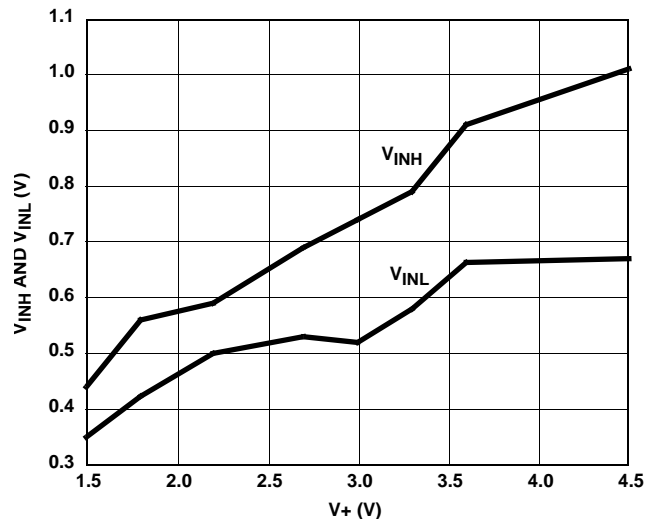FIGURE 14. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

9    intersil

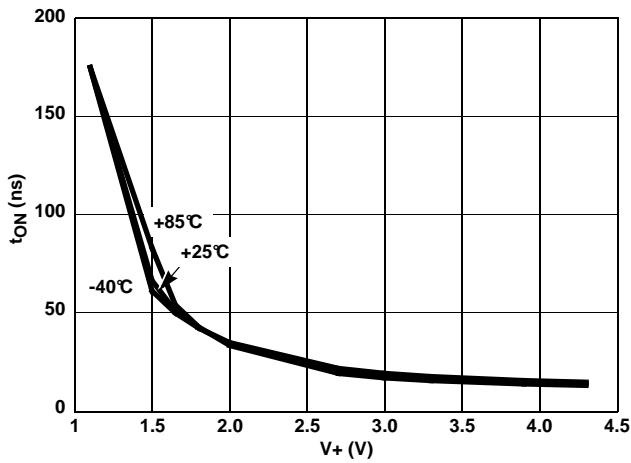## *Typical Performance Curves* T_A = +25°C, Unless Otherwise Specified **(Continued)**

**FIGURE 15. TURN - ON TIME vs SUPPLY VOLTAGE**
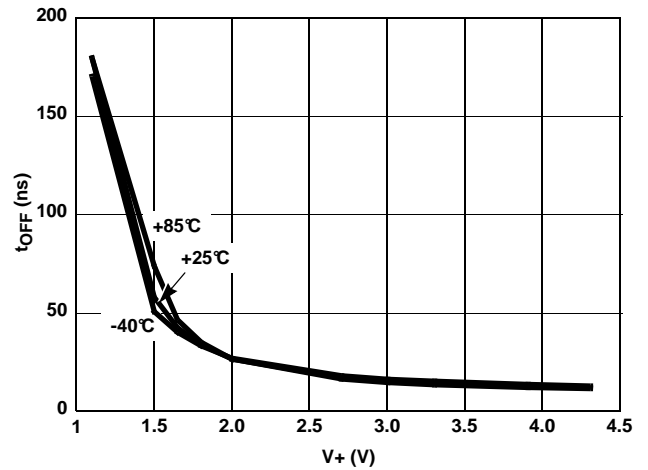
**FIGURE 16. TURN - OFF TIME vs SUPPLY VOLTAGE**
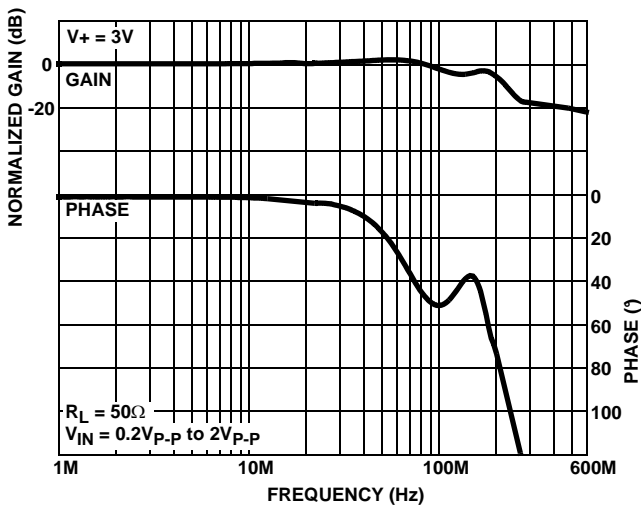
**FIGURE 17. FREQUENCY RESPONSE**
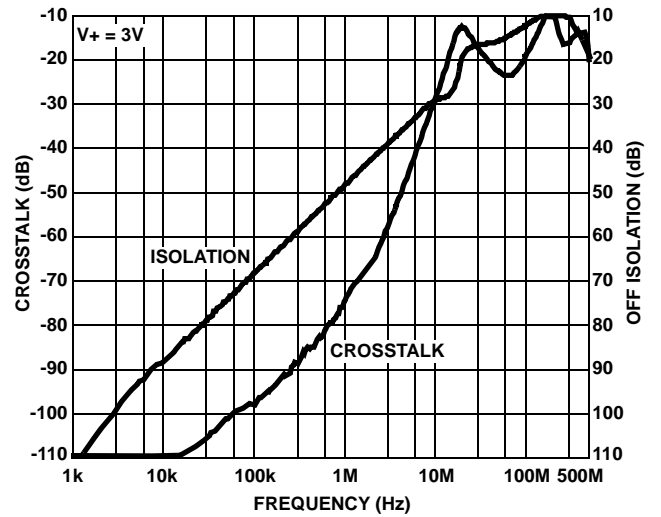
**FIGURE 18. CROSSTALK AND OFF ISOLATION**
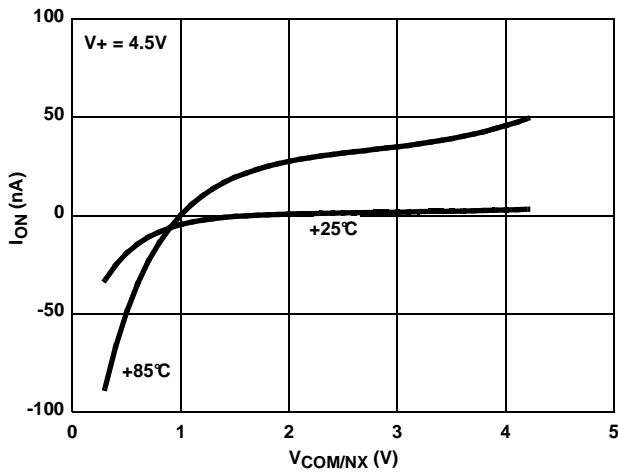
**FIGURE 19. ON LEAKAGE vs SWITCH VOLTAGE**
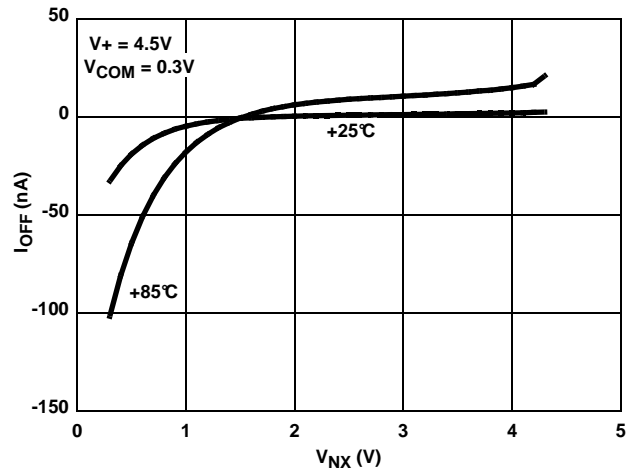
**FIGURE 20. OFF LEAKAGE vs SWITCH VOLTAGE**

## *Typical Performance Curves* $T_A$ = +25°C, Unless Otherwise Specified **(Continued)**
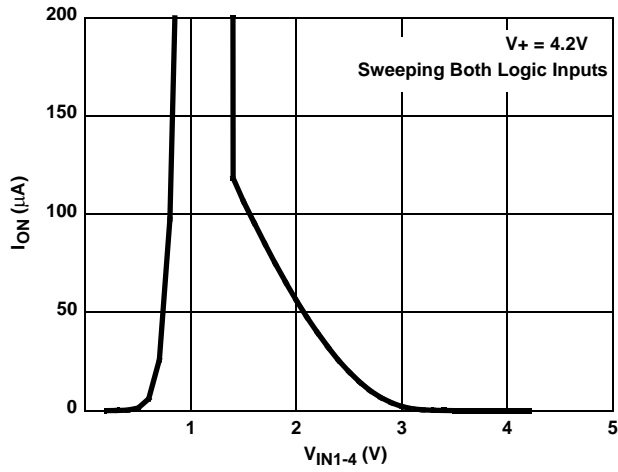


**FIGURE 21. SUPPLY CURRENT vs VLOGIC**

## *Die Characteristics*

**SUBSTRATE POTENTIAL (POWERED UP):**

GND (QFN Paddle Connection: To Ground or Float)

**TRANSISTOR COUNT:**

228

**PROCESS:**

Si Gate CMOS

## *Thin Shrink Small Outline Plastic Packages (TSSOP)*



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.

2. Dimensioning and tolerancing per ANSI Y14.5M-1982.

3. Dimension "D" does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.

4. Dimension "E1" does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.

5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.

6. "L" is the length of terminal for soldering to a substrate.

7. "N" is the number of terminal positions.

8. Terminal numbers are shown for reference only.

9. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of "b" dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).

10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

### M16.173
**16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|--------|--------|--------|--------|--------|--------|
| | MIN | MAX | MIN | MAX | |
| A | - | 0.043 | - | 1.10 | - |
| A1 | 0.002 | 0.006 | 0.05 | 0.15 | - |
| A2 | 0.033 | 0.037 | 0.85 | 0.95 | - |
| b | 0.0075 | 0.012 | 0.19 | 0.30 | 9 |
| c | 0.0035 | 0.008 | 0.09 | 0.20 | - |
| D | 0.193 | 0.201 | 4.90 | 5.10 | 3 |
| E1 | 0.169 | 0.177 | 4.30 | 4.50 | 4 |
| e | 0.026 BSC | | 0.65 BSC | | - |
| E | 0.246 | 0.256 | 6.25 | 6.50 | - |
| L | 0.020 | 0.028 | 0.50 | 0.70 | 6 |
| N | 16 | | 16 | | 7 |
| a | $0^o$ | $8^o$ | $0^o$ | $8^o$ | - |

Rev. 1 2/02

# Package Outline Drawing

## L16.3x3
**16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE**
**Rev 2, 4/07**



TOP VIEW



BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"
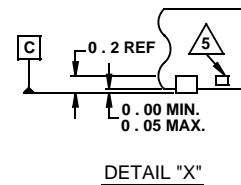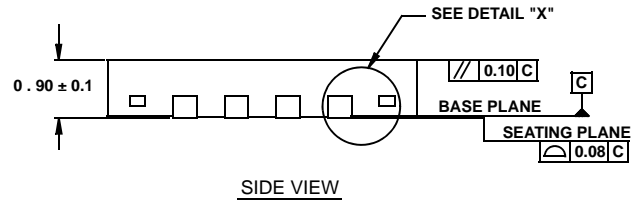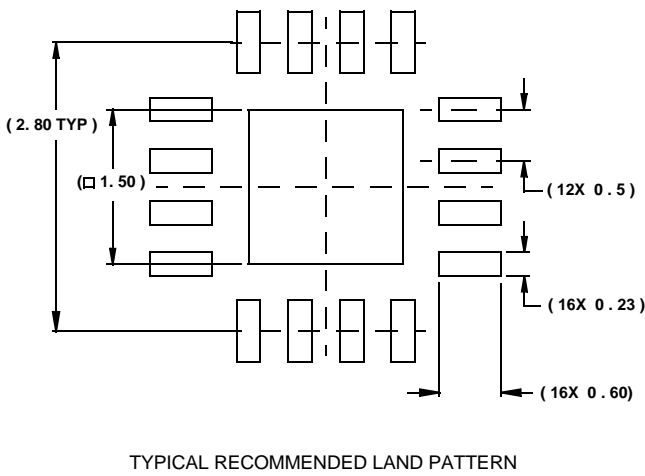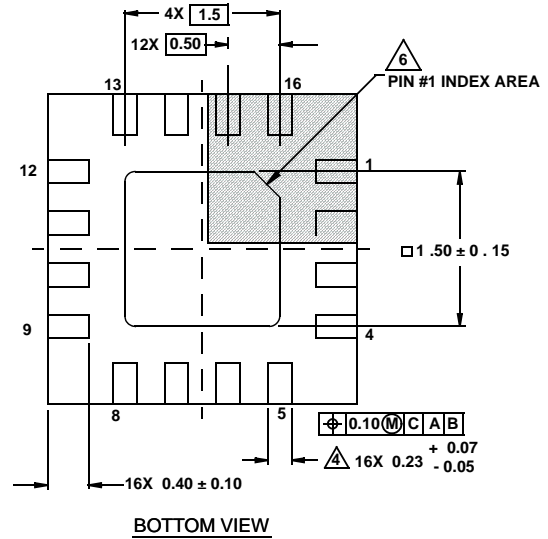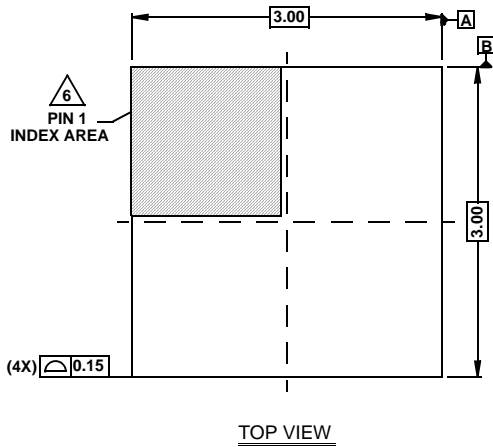
NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.

2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.

3. Unless otherwise specified, tolerance : Decimal ± 0.05

4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

## *Thin Quad Flat No-Lead Plastic Package (TQFN)*
## *Thin Micro Lead Frame Plastic Package (TMLFP)*
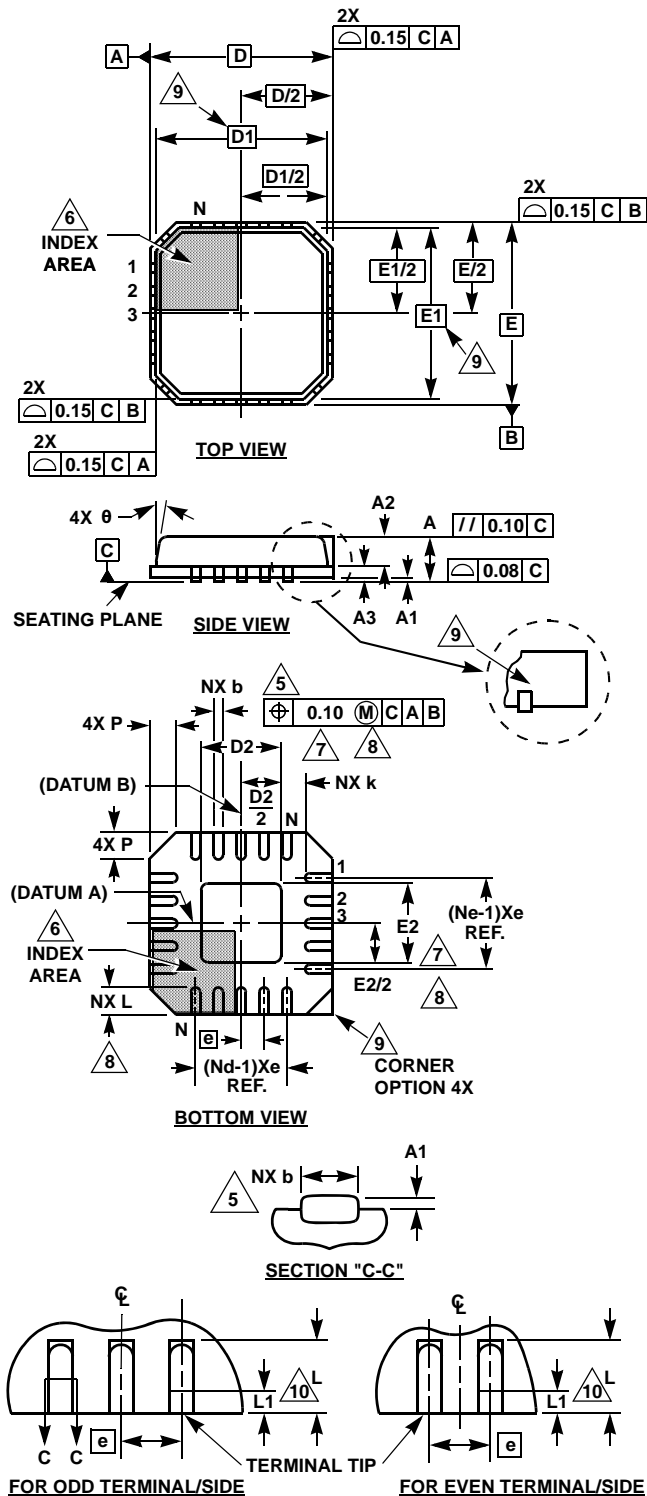
### L16.3x3A
**16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE**

| SYMBOL | MILLIMETERS | | | NOTES |
|---|---|---|---|---|
| | MIN | NOMINAL | MAX | |
| A | 0.70 | 0.75 | 0.80 | - |
| A1 | - | - | 0.05 | - |
| A2 | - | - | 0.80 | 9 |
| A3 | 0.20 REF | | | 9 |
| b | 0.18 | 0.23 | 0.30 | 5, 8 |
| D | 3.00 BSC | | | - |
| D1 | 2.75 BSC | | | 9 |
| D2 | 1.35 | 1.50 | 1.65 | 7, 8, 10 |
| E | 3.00 BSC | | | - |
| E1 | 2.75 BSC | | | 9 |
| E2 | 1.35 | 1.50 | 1.65 | 7, 8, 10 |
| e | 0.50 BSC | | | - |
| k | 0.20 | - | - | - |
| L | 0.30 | 0.40 | 0.50 | 8 |
| N | 16 | | | 2 |
| Nd | 4 | | | 3 |
| Ne | 4 | | | 3 |
| P | - | - | 0.60 | 9 |
| θ | - | - | 12 | 9 |

Rev. 0  6/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Compliant to JEDEC MO-220WEED-2 Issue C, except for the E2 and D2 MAX dimension.

All Intersil U.S. products are manufactured, assembled and tested utilizing ISO9000 quality systems.
Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality

For information regarding Intersil Corporation and its products, see www.intersil.com

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February 5, 2008