Data Sheet | March 19, 2008 | FN6592.0

12V, 1.5Ω Quad SPST Switch with Latched Parallel Interface

The ISL54302 is a quad analog bidirectional switch device targeted at industrial applications, including test and measurement equipment. It features low resistance and low leakage along with 12V operation and can be digitally controlled via a latched parallel interface. This parallel interface features a latch input pin that can be used to connect multiple devices into a parallel arrangement.

The ISL54302 can operate from a single, or split bipolar power supply and has a 3V logic interface. The ISL54302 is specified for use over the -40°C to +85°C temperature range and is available in a 20 Ld 4x4 QFN Pb-free package.

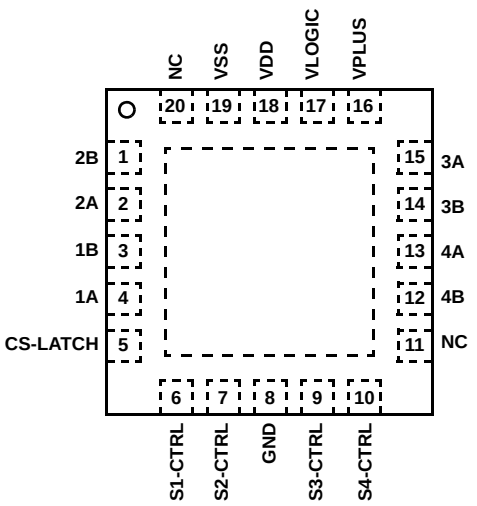
Table 1 summarizes the performance of this family.

TABLE 1. FEATURES AT A GLANCE

CONFIGURATION	QUAD SPST
r_{ON}	1.5Ω
t_{ON}/t_{OFF}	25ns/80ns
Package	20 Ld QFN 4x4

Pinout

ISL54302
(20 LD QFN)
TOP VIEW



Features

- 4 independently controlled SPST switches
- ON-resistance @ 12V. 1.5Ω
- Single or split supply voltage operation
- r_{ON} flatness. . . . . <1Ω
- r_{ON} matching between channels . . . . . <0.2Ω
- Turn-on/Turn-off time 25ns/80ns
- Switch bandwidth 60MHz
- Parallel data interface up to 40MHz
- 3V logic interface
- 20 Ld QFN package
- Pb-free (RoHS compliant)

Related Literature

- TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- TB389 “PCB Land Pattern and Surface Mount Guidelines for QFN Packages”
- AN557 “Recommended Test Procedures for Analog Switches”

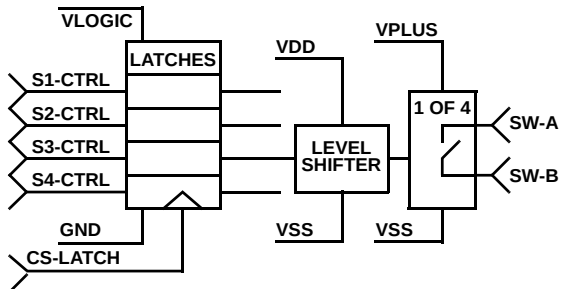
Ordering Information

PART NUMBER (Note)	PART MARKING	TEMP. RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL54302IRZ*	54 302IRZ	-40 to +85	20 Ld 4x4 QFN	L20.4x4C

*Add “-T” for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

ISL54302 Block Diagram



Pin Descriptions

PIN NUMBER	PIN NAME	PIN DESCRIPTION
1	2B	Switch 2 signal terminal
2	2A	Switch 2 signal terminal
3	1B	Switch 1 signal terminal
4	1A	Switch 1 signal terminal
5	CS-LATCH	Chip Select input
6	S1-CTRL	Switch one logic control
7	S2-CTRL	Switch two logic control
8	GND	Device ground terminal
9	S3-CTRL	Switch three logic control
10	S4-CTRL	Switch four logic control
11	NC	Not internally connected
12	4B	Switch 4 signal terminal
13	4A	Switch 4 signal terminal
14	3B	Switch 3 signal terminal
15	3A	Switch 3 signal terminal
16	VPLUS	Positive analog power supply
17	VLOGIC	Logic supply voltage
18	VDD	Level shifter supply voltage
19	VSS	Negative analog power supply
20	NC	Not internally connected

Absolute Maximum Ratings

VPLUS to VSS . . . . . -0.3V to15V
VDD to VSS . . . . . -0.3V to 5V
VLOGIC to GND . . . . . -0.3V to 5V
VSS to GND . . . . . -4V to 0.3V
VPLUS to GND . . . . . -0.3V to 15V
All Other Pins (Note 1) . . . . . ((VSS) - 0.3V) to ((VPLUS) + 0.3V)
Continuous Current (Any Terminal) 35mA
Peak Current, 1A-4A,1B-4B
(Pulsed 1ms, 10% Duty Cycle, Max) 100mA
ESD Rating
Human Body Model . . . . . >3kV
CDM . . . . . >1.5kV
Machine Model 300V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (℃/W)	θ_{JC} (℃/W)
20 Ld QFN Package (Notes 2, 3)	32	1.4

Maximum Junction Temperature (Plastic Package) . . . . . +150℃
Maximum Storage Temperature Range . . . . . -65℃ to +150℃
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Analog Switch Signal Range . . . . . VSS + 0.5V to VPLUS - 0.5V
Temperature Range . . . . . -40℃ to +85℃

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. Signals on 1A-4A,1B-4B, exceeding VPLUS or VSS are clamped by internal diodes. DATA_IN, CLOCK_IN, CS_LATCH exceeding VLOGIC or VSS are clamped by internal diodes. Limit forward diode current to maximum current ratings.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications

Test Conditions: VPLUS = +9V, VSS = -3V Supply, VLOGIC = 3V, VDD = GND = 0V, V_{INH} = 2.2V, V_{INL} = 0.8V, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (℃)	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-resistance, r_{ON}	I_{COM} = 10mA, VXA, VXB within analog signal (see Figure 4)	25		2.0		Ω
		Full		2.5		Ω
r_{ON} Matching Between Channels, Δr_{ON}	I_{COM} = 10mA, VXA, VXB within analog signal range (Note 5)	25		0.2		Ω
		Full		0.3		Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	I_{COM} = 10mA, VXA, VXB within analog signal range (Note 4)	25		0.4		Ω
		Full		0.6		Ω
OFF Leakage Current, $I_{NO(OFF)}$	VXA, VXB within analog signal range	25		15		nA
		Full	-200		+200	nA
DIGITAL INPUT CHARACTERISTICS (Note 8)						
Input Voltage High, Digital Interface	SW-CTRL(1-4), CS_LATCH	Full	2.2	1.75		V
Input Voltage Low, Digital Interface	SW-CTRL(1-4), CS_LATCH	Full		1.75	0.8	V
SW-CTRL (1-4) Into CS_Latch Setup Time	t_{SETUP} (Note 6, Figure 5)	Full		1		ns
SW-CTRL (1-4) Into CS_Latch Hold Time	t_{HOLD} (Note 6, Figure 5)	Full		3.5		ns
Input Current, I_{INH}, I_{INL}	V_{IN} = 0V or VLOGIC	Full	-1	0.01	1	µA
CS_LATCH Rise, Fall Time	10% to 90% and 90% to 10%	Full		3		ns
CS_LATCH Minimum Pulse Width	Rising to Falling Edge 50% Points	Full		10		ns
SWITCH DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	VXA, VXB = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0V to 3V, (see Figure 1)	25		50		ns
		Full		55		ns

Electrical Specifications Test Conditions: VPLUS = +9V, VSS = -3V Supply, VLOGIC = 3V, VDD = GND = 0V, V_{INH} = 2.2V, V_{INL} = 0.8V, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNITS
Turn-OFF Time, t_{OFF}	VXA, VXB = 3V, R_L = 300Ω, C_L = 35pF, V_{IN} = 0V to 3V, (see Figure 1)	25		90		ns
		Full		95		ns
OFF Capacitance, C_{OFF}	f = 1MHz, VXA or VXB = 0V	25		50		pF
ON Capacitance, $C_{COM(ON)}$	f = 1MHz, VXA or VXB = 0V	25		100		pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, VXA or VXB = $1V_{P-P}$ (see Figure 3)	25		-45		dB
Crosstalk (Note 5)		25		-65		dB
Switch Contact 3dB Bandwidth	R_L = 50Ω, C_L = 5pF			60		MHz
Charge Injection, Q	C_L = 1nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25		125		pC
POWER SUPPLY CHARACTERISTICS						
VPLUS Supply, I (Quiescent)		25		15		µA
		Full		17	45	µA
VPLUS Supply, I (40MHz)		25		18		µA
		Full		22		µA
VSS Supply, I (Quiescent)		25		16		µA
		Full		22	50	µA
VSS Supply, I (40MHz)		25		1		mA
		Full		1		mA
VDD Supply, I (Quiescent)		25		1		µA
		Full		4	10	µA
VDD Supply, I (40MHz)		25		0.4		mA
		Full		0.4		mA
VLOGIC Internal Logic Supply, I (Quiescent)		25		0		µA
		Full		1	10	µA
VLOGIC Internal Logic Supply, I (40MHz)		25		3.5		mA
		Full		3.5		mA

Electrical Specifications Test Conditions: VPLUS = +7V, VSS = 0V Supply, VLOGIC= 3V, VDD = 3V, GND = 0V, V_{INH} = 2.2V, V_{INL} = 0.8V, Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNITS
ANALOG SWITCH CHARACTERISTICS						
ON-resistance, r_{ON}	I_{COM} = 10mA, VXA, VXB within Analog Signal Range (see Figure 4)	25		2.7		Ω
		Full		3.5		Ω
r_{ON} Matching Between Channels, Δr_{ON}	I_{COM} = 10mA, VXA, VXB within Analog Signal Range (Note 5)	25		0.1		Ω
		Full		0.15		Ω
r_{ON} Flatness, $r_{FLAT(ON)}$	I_{COM} = 10mA, VXA, VXB within Analog Signal Range (Note 4)	25		0.5		Ω
		Full		0.6		Ω
OFF Leakage Current, $I_{NO(OFF)}$	VXA = 1V, 4.5V, VXB= 4.5V, 1V	25		3		nA
		Full	-200	30	200	nA
DIGITAL INPUT CHARACTERISTICS (Note 8)						
Input Voltage High, Digital Interface	SW-CTRL(1-4), CS_LATCH	Full	2.2	1.75		V
Input Voltage Low, Digital Interface	SW-CTRL(1-4), CS_LATCH	Full		1.75	0.8	V

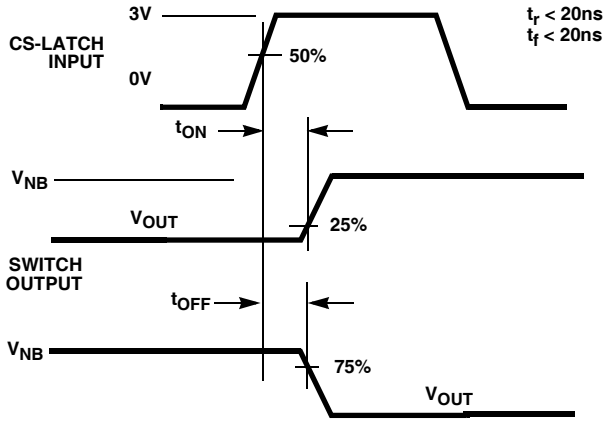
Electrical Specifications Test Conditions: VPLUS = +7V, VSS = 0V Supply, VLOGIC= 3V, VDD = 3V, GND = 0V, V_{INH} = 2.2V, V_{INL} = 0.8V, Unless Otherwise Specified. **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP (°C)	MIN (Note 9)	TYP (Note 10)	MAX (Note 9)	UNITS
SW-CTRL (1-4) Into CS_Latch Setup Time	t_{SETUP} (Note 6, Figure 5)	Full		1		ns
SW-CTRL (1-4) Into CS_Latch Hold Time	t_{HOLD} (Note 6, Figure 5)	Full		3.5		ns
Input Current, I_{INH}, I_{INL}	V_{IN} = 0V or VLOGIC	Full	-1	0.01	1	µA
CS_LATCH Rise, Fall Time	10% to 90% and 90% to 10%	Full		3		ns
CS_LATCH Minimum Pulse Width	Rising to Falling Edge 50% Points	Full		10		ns
DYNAMIC CHARACTERISTICS						
Turn-ON Time, t_{ON}	VXA or VXB = 3V, R_L = 300Ω, C_L = 35pF (see Figure 1)	25		25		ns
		Full		30		ns
Turn-OFF Time, t_{OFF}	VXA or VXB = 3V, R_L = 300Ω, C_L = 35pF (see Figure 1)	25		80		ns
		Full		85		ns
OFF Capacitance, C_{OFF}	f = 1MHz, VXA or VXB = V_{COM} = 0V	25		50		pF
ON Capacitance, $C_{COM(ON)}$	f = 1MHz, VXA or VXB = V_{COM} = 0V	25		100		pF
OFF Isolation	R_L = 50Ω, C_L = 15pF, f = 1MHz, VXA or VXB= $1V_{P-P}$ (see Figure 3)	25		-45		dB
Crosstalk (Note 5)		25		-65		dB
Switch Contact 3dB Bandwidth	R_L = 50Ω, C_L = 5pF	25		60		MHz
Charge Injection, Q	C_L = 1nF, V_G = 0V, R_G = 0Ω (see Figure 2)	25		25		pC
POWER SUPPLY CHARACTERISTICS						
VPLUS Supply, I (Quiescent)		25		13		µA
		Full		15	45	µA
VPLUS Supply, I (40MHz)		25		18		µA
		Full		20		µA
VSS Supply, I (Quiescent)		25		14		µA
		Full		19	50	µA
VSS Supply, I (40MHz)		25		0.7		mA
		Full		0.7		mA
VDD Supply, I (Quiescent)		25		1		µA
		Full		4	10	µA
VDD Supply, I (40MHz)		25		0.4		mA
		Full		0.5		mA
VLOGIC Internal Logic Supply, I (Quiescent)		25		0		µA
		Full		1	10	µA
VLOGIC Internal Logic Supply, I (40MHz)		25		3.2		mA
		Full		3.2		mA

NOTES:

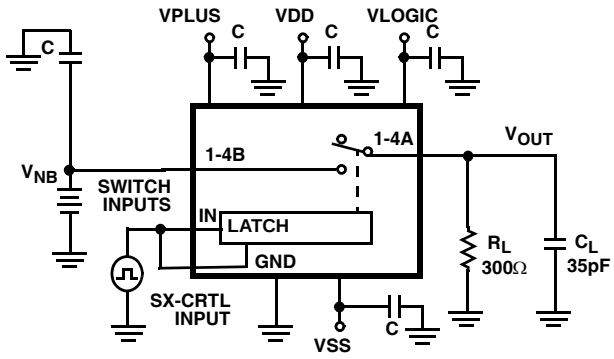
4. Flatness is defined as the delta between the maximum and minimum r_{ON} values over the specified voltage range.
5. Between any two switches.
6. CS_LATCH must remain low when changing SW-CTRL(1-4) condition. Likewise, while CS_LATCH is being toggled, it is important to keep SW-CTRL(1-4) in the intended switch condition.
7. Typical Values are not production tested
8. Digital Characteristics remain stable with respect to VPLUS and VSS variation. These parameters are controlled by the difference between VSS and VDD, which the user should maintain at a constant spread of VDD = VSS + 3V.
9. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.
10. Limits established by characterization and are not production tested.

Test Circuits and Waveforms



Switch changes state on rising edge of CS-LATCH. V_{NA} = VOUT at all times.

FIGURE 1A. MEASUREMENT POINTS

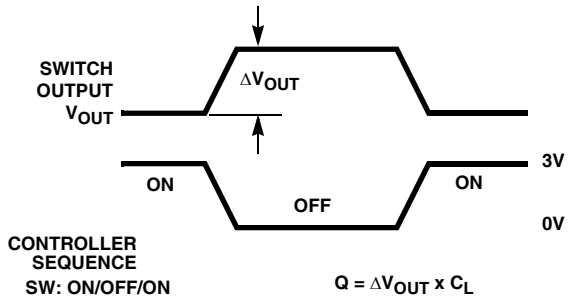


Repeat test for all switches. C_L includes fixture and stray capacitance.

$$V_{OUT} = V_{(NB)} \frac{R_L}{R_L + r_{(ON)}}$$

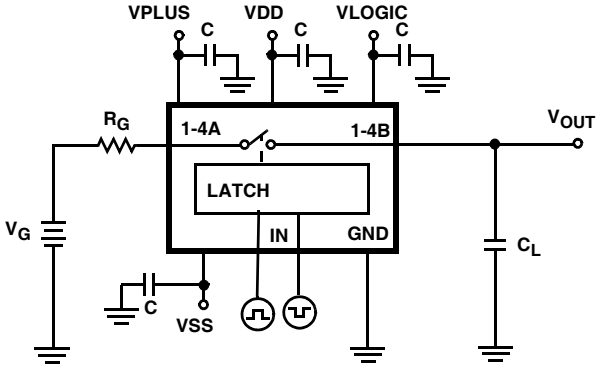
FIGURE 1B. TEST CIRCUIT

FIGURE 1. SWITCHING TIMES



Switch changes state on rising edge of CS-LATCH.

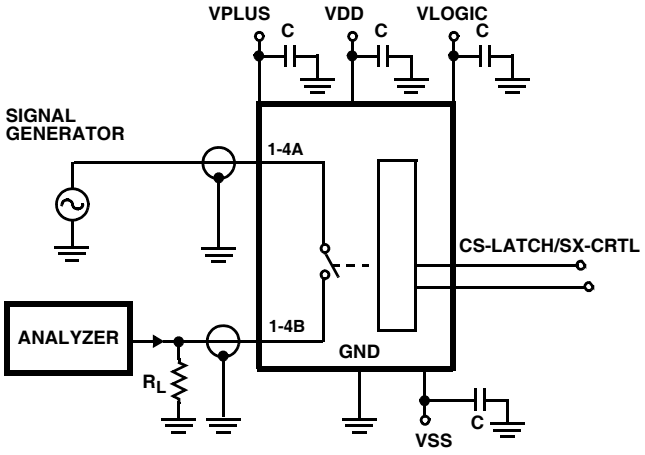
FIGURE 2A. MEASUREMENT POINTS



Repeat test for all switches. C_L includes fixture and stray capacitance.

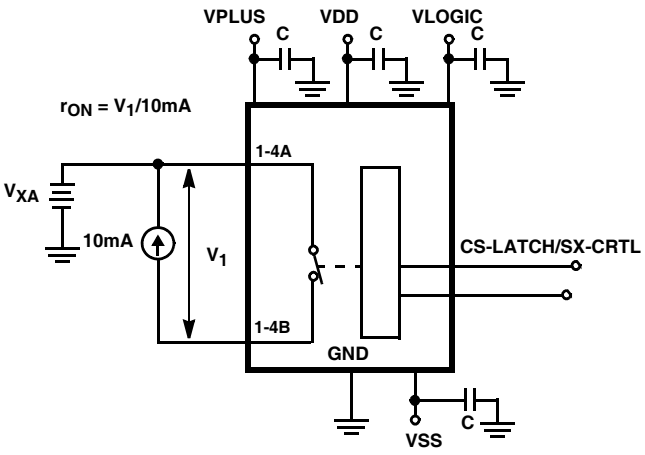
FIGURE 2B. TEST CIRCUIT

FIGURE 2. CHARGE INJECTION



Repeat test for all switches.

FIGURE 3. OFF ISOLATION TEST CIRCUIT



Repeat test for all switches.

FIGURE 4. r_{ON} TEST CIRCUIT

Test Circuits and Waveforms (Continued)

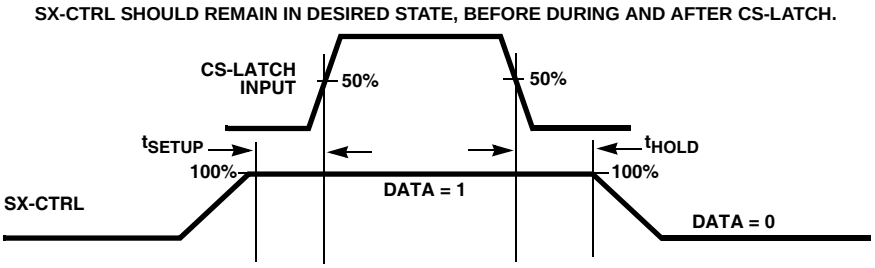


FIGURE 5. SETUP AND HOLD TIMES

ISL54302 Detailed Description

The ISL54302 quad analog switches offer switching capability from a split-supply -3V and +9V or single 0V and 5V to 12V supply. Please review “Power Supply Considerations” on page 7 before powering up the device.

The user can employ multi-device control data in two ways. The S1-S4-CTRL lines can be connected to several devices, with each device having its own CS-LATCH connection to the system controller. The other way is to have separate S1-4-CTRL connections for each switch and a single CS-LATCH connection to all ISL54302s.

Power Supply Considerations

The ISL54302 construction consists of CMOS analog switches and four supply pins: VPLUS, VSS, VLOGIC, VDD and GND. VPLUS and VSS determine the switch voltage range of the four SPST CMOS switches and set their analog voltage limits. There are no connections between the switch contact signal path and GND.

VLOGIC and GND power the digital input/output logic level shifters (thus setting the digital switching point). The level shifters convert the external logic levels to VDD and VSS signals to drive the internal digital circuitry.

VDD and VSS power the internal logic of the device. VDD must always be held at a fixed 3V above VSS to avoid device damage.

Whether operating split or single device, GND will always be @ 0V and VLOGIC will always be @ 3V.

VDD should always remain 3V above VSS. VSS to VPLUS should not exceed a maximum spread of more than 12V. For examples, see the following:

SPLIT POSITIVE AND NEGATIVE SWITCH RANGE OPERATION

- VSS = -3V, VDD = +0V, VPLUS = +9V, VLOGIC = 3V
- VSS = -1V, VDD = +2V, VPLUS = +11V, VLOGIC = 3V

POSITIVE SWITCH RANGE OPERATION

- VSS = 0V, VDD = +3V, VPLUS = +12V, VLOGIC = 3V

ISL54302 Parallel Communications

The ISL54302 operates based on parallel data. CTRL and LATCH inputs are 3V level compatible. Setup and Hold times relative to the rising the edge of the CS-LATCH input must be maintained for proper operation. Switch control data is clocked into internal registers on the rising edge of CS-LATCH.

MULTIPLE DEVICE CONNECTION

The user can configure the four SX-CTRL inputs to connect to several ISL54302’s. In this configuration each ISL54302 requires a separate/dedicated CS-LATCH input. Therefore, each device will update at different times.

So in essence, the S1-S4-CTRL signals are multiplexed and connected to all switch control inputs in parallel (see Figure 8).

For non-multiplexed connections, each SX-CTRL input must have a dedicated logic input for each switch/each device. If three ISL54302s are being used, the user must supply 12 dedicated SX-CTRL signals. All switches are then tied to the same CS-LATCH pin and all devices would change state at the same time.

ISL54302 CS-LATCH Pin Discussion

The ISL54302’s operational state does not change while SX-CTRL inputs are changing. The user must insure that the CS-LATCH pin remains low and does not change state while SX-CTRL inputs are changing.

Once the user has set the SX-CTRL inputs, the CS-LATCH pin is then utilized. Just as the CS-LATCH pin must remain low during SX-CTRL setup, the SX-CTRL pins must remain stable during and after the CS-LATCH operation.

The switch from present to next operation occurs on the rising edge on the CS-LATCH pin. This rising edge transfers data to the internal 4-bit switch control registers. This transfer updates opening/closing of the four switches.

ISL54302 Power On Reset (POR)

Switch conditions are controlled during POR (Power On Reset). During and after a POR condition, the switches are opened until closed by the controller.

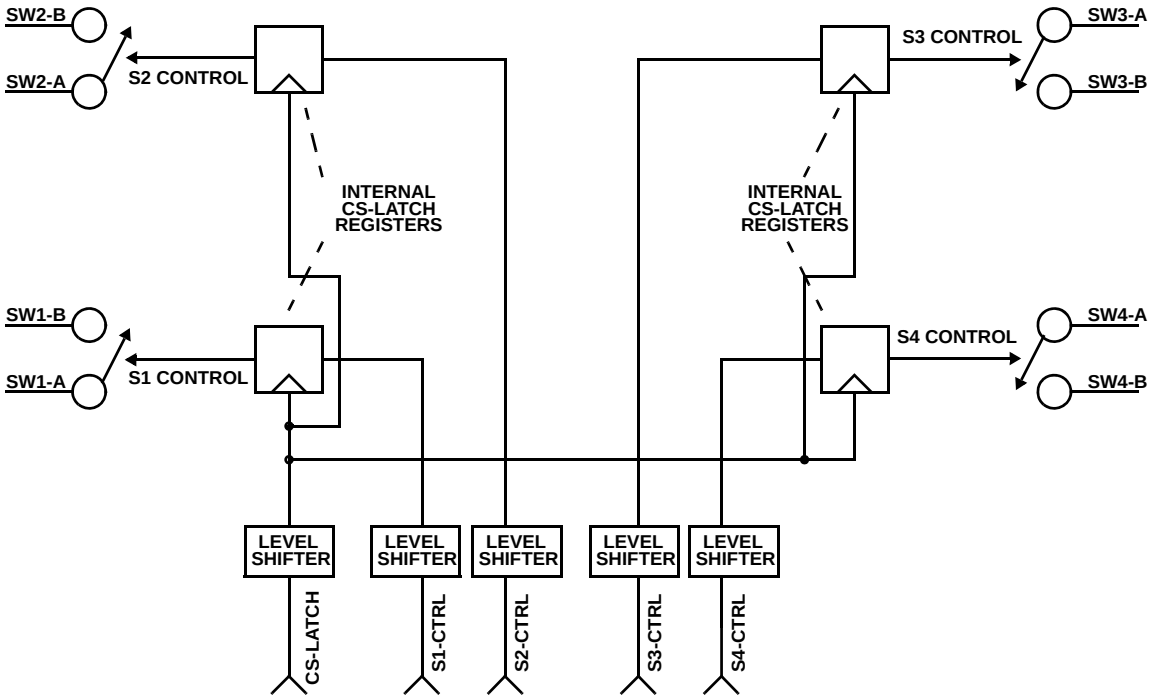


FIGURE 6. ISL54302 FUNCTIONAL DIAGRAM

Supply Sequencing and Overvoltage Protection

With any CMOS device, proper power supply sequencing is required to protect the device from excessive input currents, which might permanently damage the IC. All switch contact I/O pins contain ESD protection diodes from the pin to VPLUS and to VSS (see Figure 7). To prevent forward biasing these diodes, VPLUS, GND and VSS must be applied before any input signals, and switch signal voltages must remain between VPLUS and VSS. Digital control signals should be limited to VLOGIC and VSS.

SPECIFIC POWER SEQUENCE

1. GND
2. VSS Typical . . . . . 3V to 0V with respect to GND
3. VPLUS Typical . . . . . +5V to +9V with respect to GND
4. VDD . . . . . +3V to with respect to VSS
5. VLOGIC . . . . . +3V with respect to GND

If these conditions cannot be guaranteed, then one of the following two protection methods should be employed.

Logic inputs can easily be protected by adding a 1kΩ resistor in series with the input. The resistor limits the input current below the threshold that produces permanent damage, and the sub-microamp input current produces an insignificant voltage drop during normal operation.

Adding a series resistor to the switch input defeats the purpose of using a low r_{ON} switch, so two small signal diodes can be added in series with the supply pins to provide overvoltage protection for all pins (see Figure 7). These additional diodes limit the analog signal from 1V below VPLUS to 1V above VSS. The leakage current performance is unaffected by this approach, but the switch resistance may increase, especially at low supply voltages.

ESD Protection

The device contains ESD protection on the device pins. These devices are design to work based on dV/dt. During power-up, the user should review the rise/fall times on the power connections. The rise time of the power rails should not be faster than 1µs.

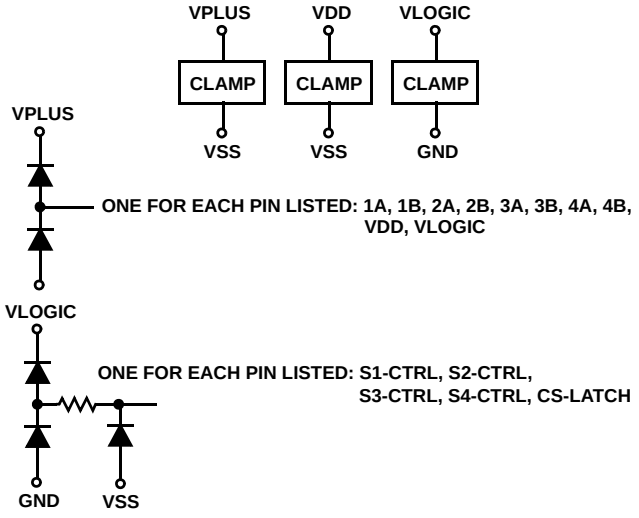


FIGURE 7. ESD/OVERVOLTAGE PROTECTION

Logic-Level Thresholds

VLOGIC and GND power the internal logic level shifter stages, so VPLUS and VSS have no affect on logic thresholds. Thus, SX-CTRL, CS-LATCH receive thresholds which will remain constant, despite changes to VPLUS and VSS.

Leakage Considerations

Reverse ESD protection diodes are internally connected between each analog-signal pin and both VPLUS and VSS. One of these diodes conducts if any analog signal exceeds VPLUS or VSS.

ISL54302 Device Programming

Programming the device entails accessing the internal switch control registers. To write data into the register, the data must be transferred via the CS-LATCH pin.

Via the CS-LATCH pin, the programmer has complete control as to “when” data is transferred to the internal latches. Until such time as the CS-LATCH pin is “toggled,” the device will remain as previously programmed. Therefore, data transitions on the SX-CTRL inputs will not effect the switch’s operational condition.

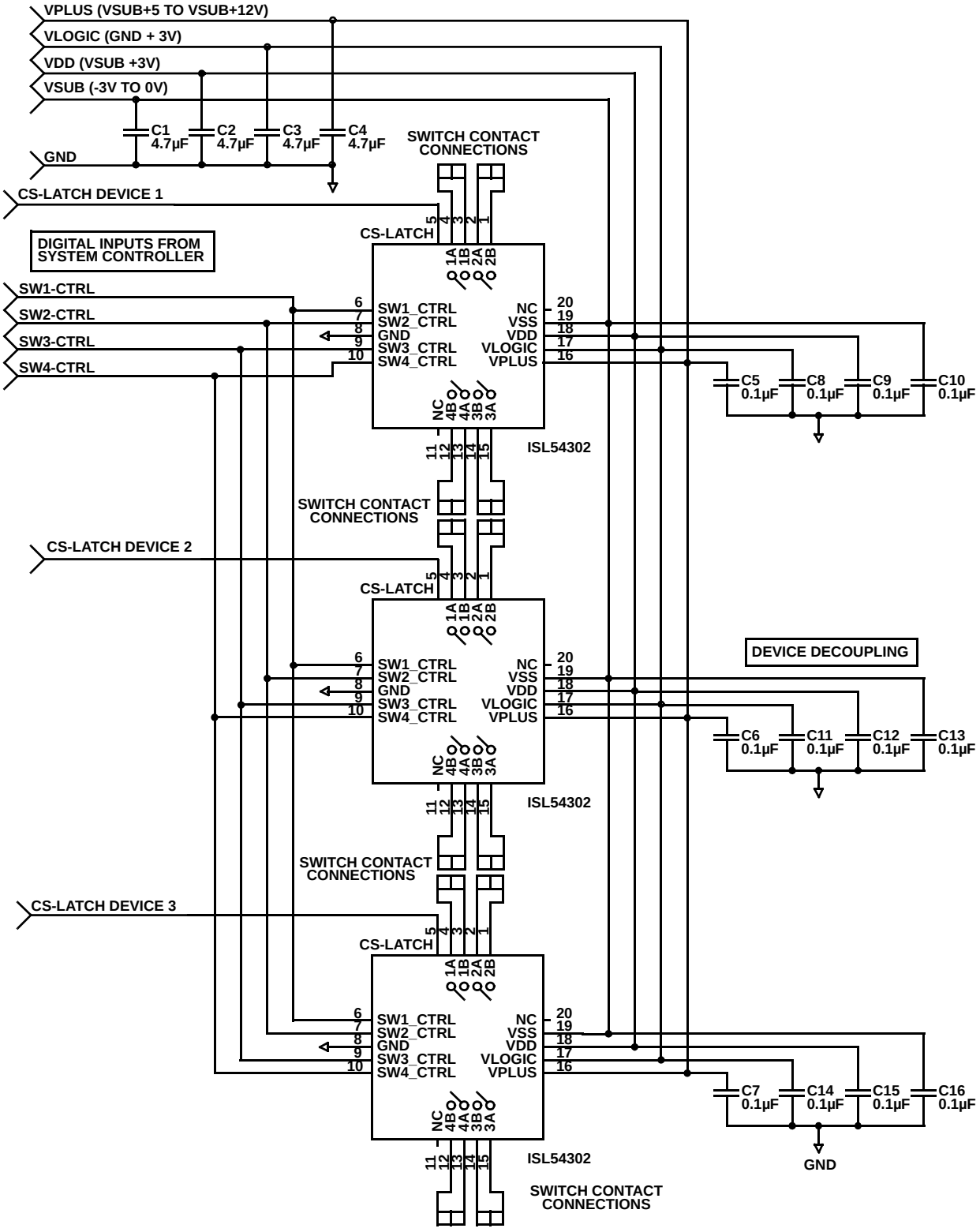


FIGURE 8. ISL54302 SW-CONTROL LINES MULTIPLEXED

Typical Performance Curves

VLOGIC = 3V, T_A = +25°C, V_{IH} = 3V, V_{IL} = 0V, Unless Otherwise Specified.

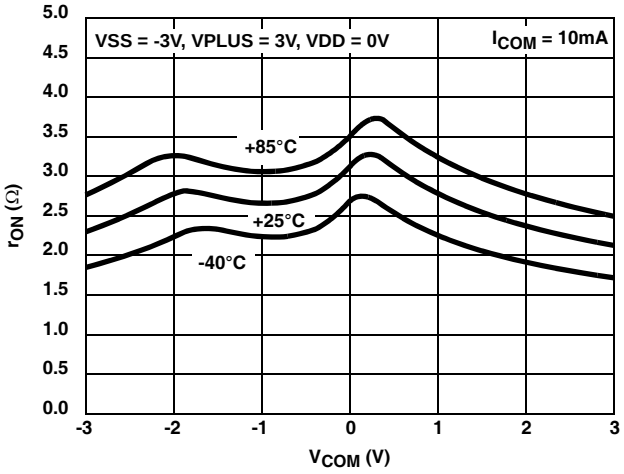


FIGURE 9. ON-RESISTANCE vs SWITCH VOLTAGE

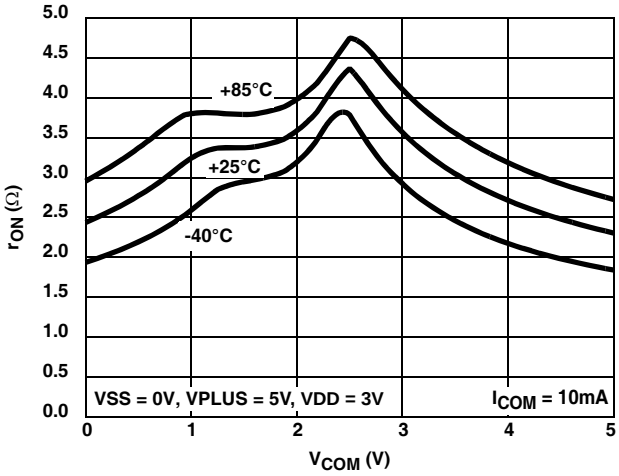


FIGURE 10. ON-RESISTANCE vs SWITCH VOLTAGE

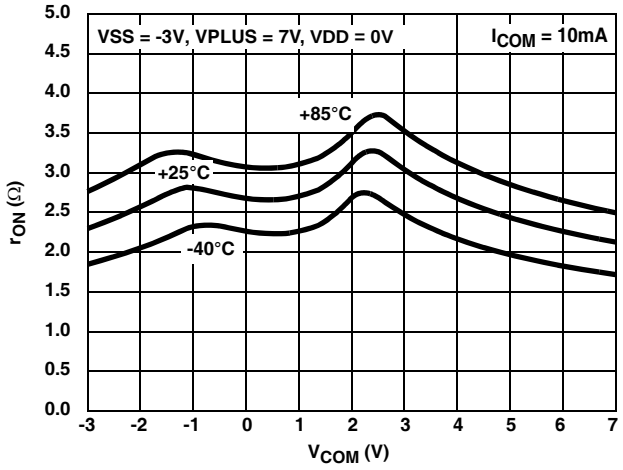


FIGURE 11. ON-RESISTANCE vs SWITCH VOLTAGE

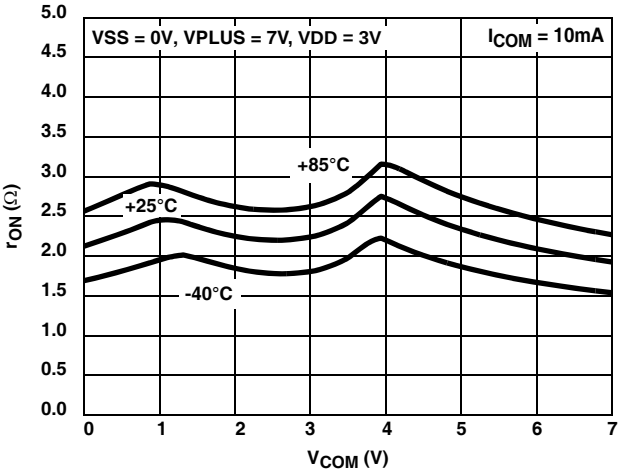


FIGURE 12. ON-RESISTANCE vs SWITCH VOLTAGE

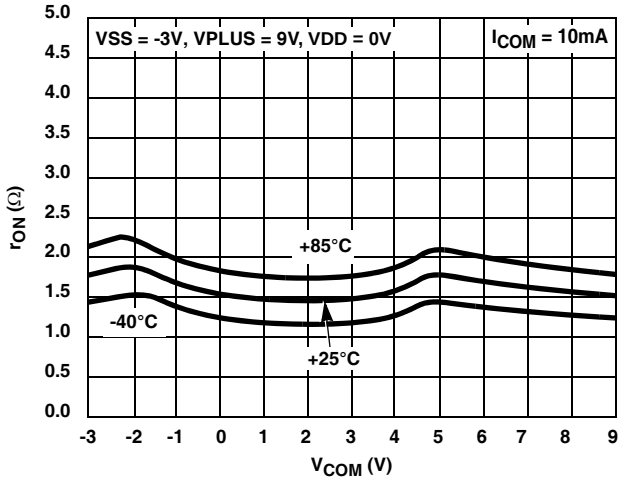


FIGURE 13. ON-RESISTANCE vs SWITCH VOLTAGE

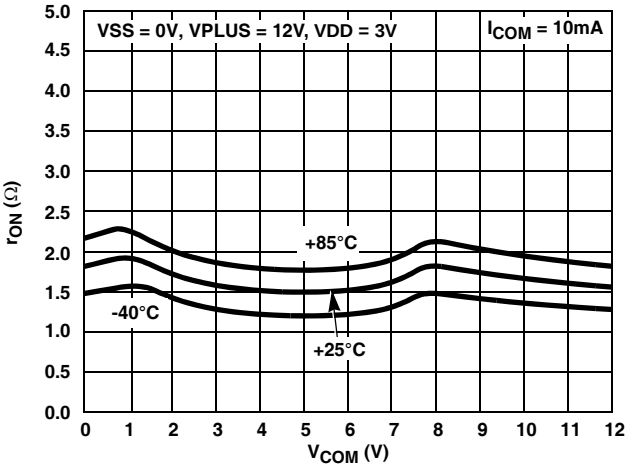


FIGURE 14. ON-RESISTANCE vs SWITCH VOLTAGE

Typical Performance Curves

VLOGIC = 3V, T_A = +25°C, V_{IH} = 3V, V_{IL} = 0V, Unless Otherwise Specified. **(Continued)**

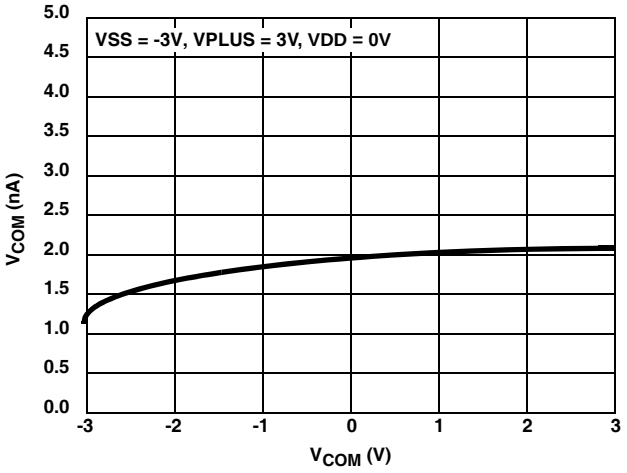


FIGURE 15. ON-LEAKAGE vs SWITCH VOLTAGE

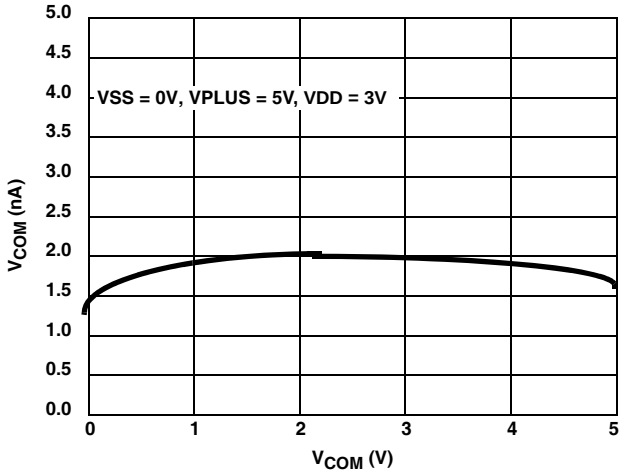


FIGURE 16. ON-LEAKAGE vs SWITCH VOLTAGE

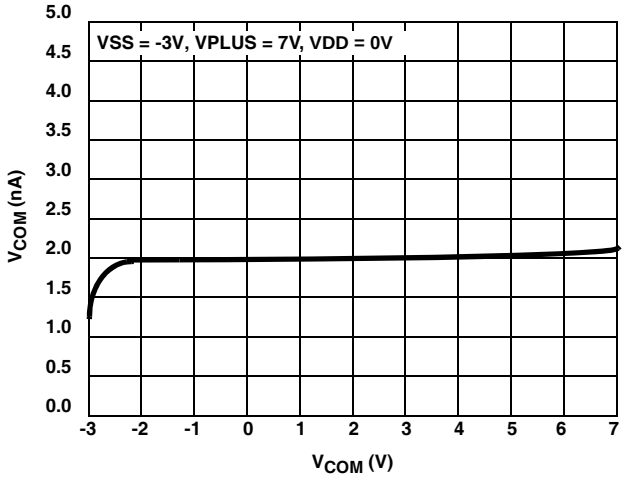


FIGURE 17. ON-LEAKAGE vs SWITCH VOLTAGE

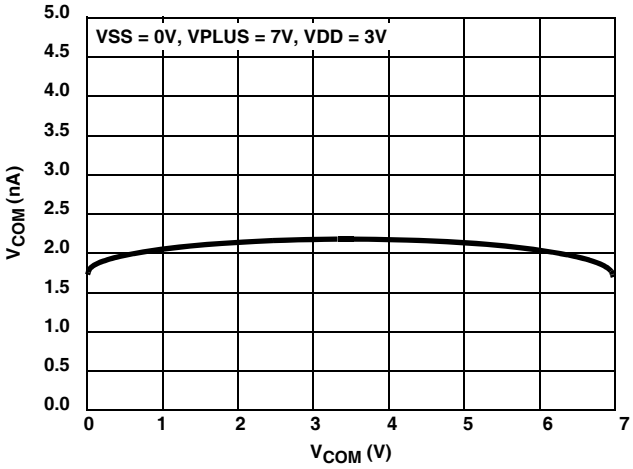


FIGURE 18. ON-LEAKAGE vs SWITCH VOLTAGE

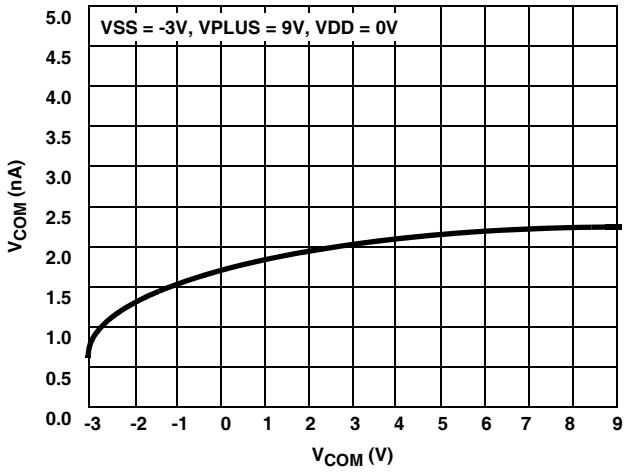


FIGURE 19. ON-LEAKAGE vs SWITCH VOLTAGE

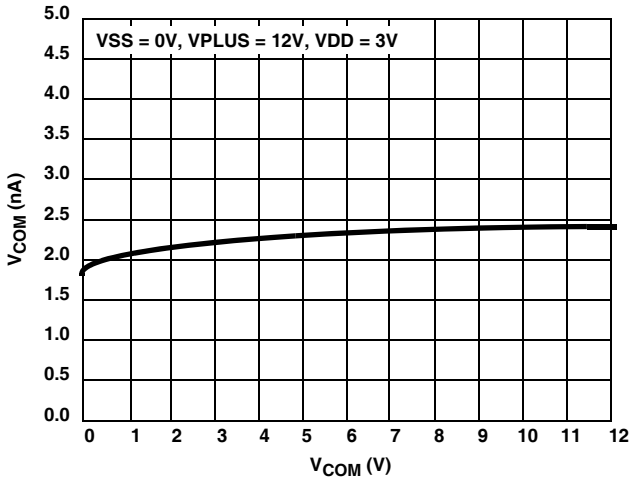


FIGURE 20. ON-LEAKAGE vs SWITCH VOLTAGE

Typical Performance Curves

VLOGIC = 3V, T_A = +25°C, V_{IH} = 3V, V_{IL} = 0V, Unless Otherwise Specified. **(Continued)**

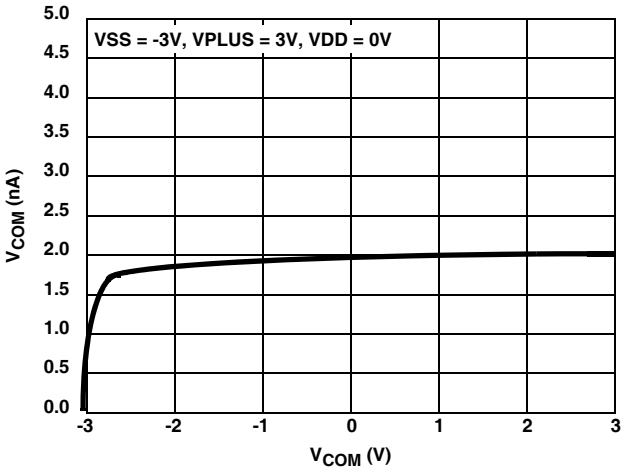


FIGURE 21. OFF-LEAKAGE vs SWITCH VOLTAGE

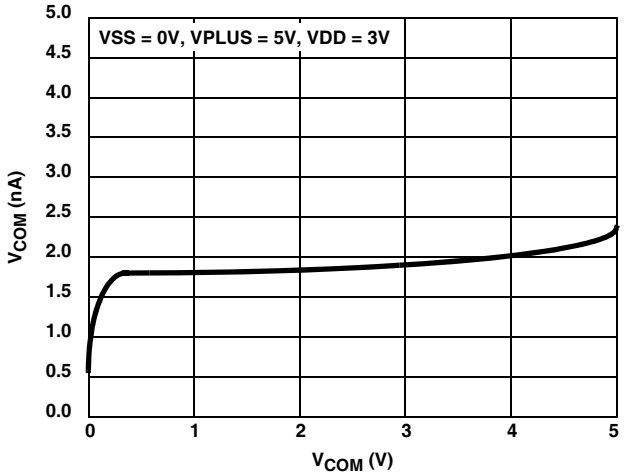


FIGURE 22. OFF-LEAKAGE vs SWITCH VOLTAGE

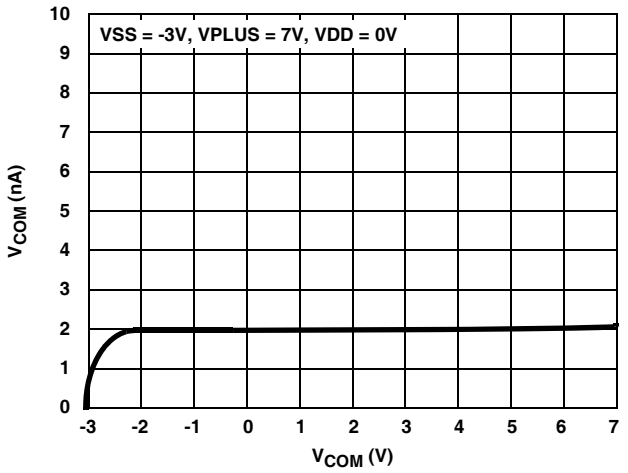


FIGURE 23. OFF-LEAKAGE vs SWITCH VOLTAGE

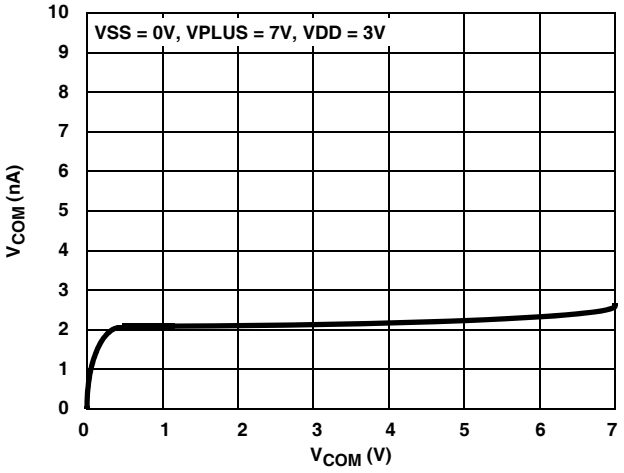


FIGURE 24. OFF-LEAKAGE vs SWITCH VOLTAGE

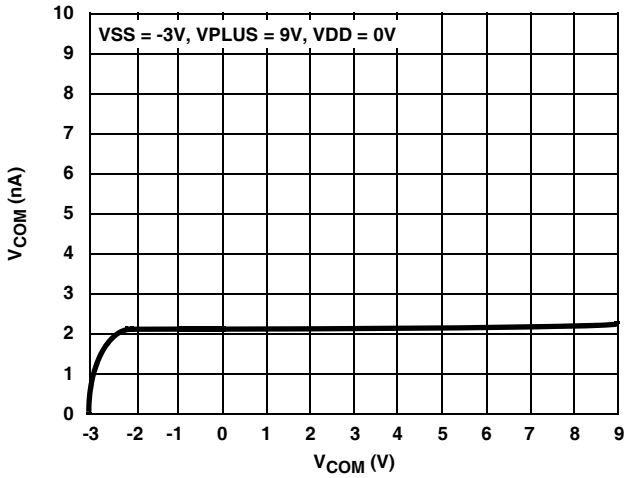


FIGURE 25. OFF-LEAKAGE vs SWITCH VOLTAGE

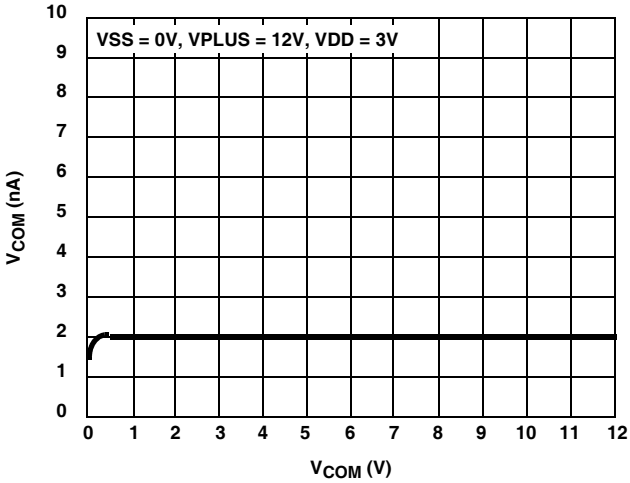


FIGURE 26. OFF-LEAKAGE vs SWITCH VOLTAGE

Typical Performance Curves

VLOGIC = 3V, T_A = +25°C, V_{IH} = 3V, V_{IL} = 0V, Unless Otherwise Specified. **(Continued)**

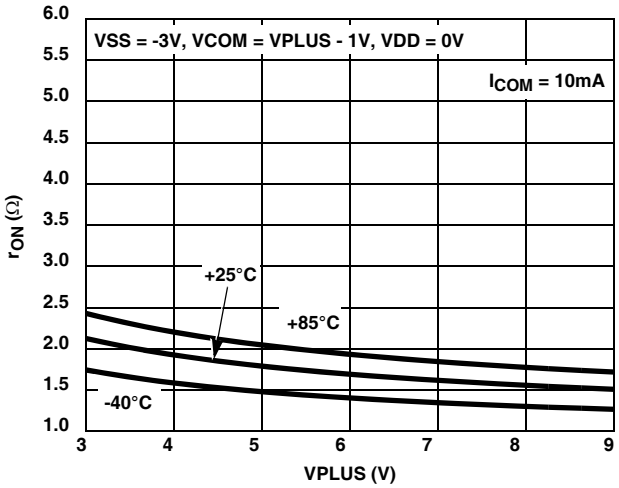


FIGURE 27. ON-RESISTANCE vs SUPPLY VOLTAGE

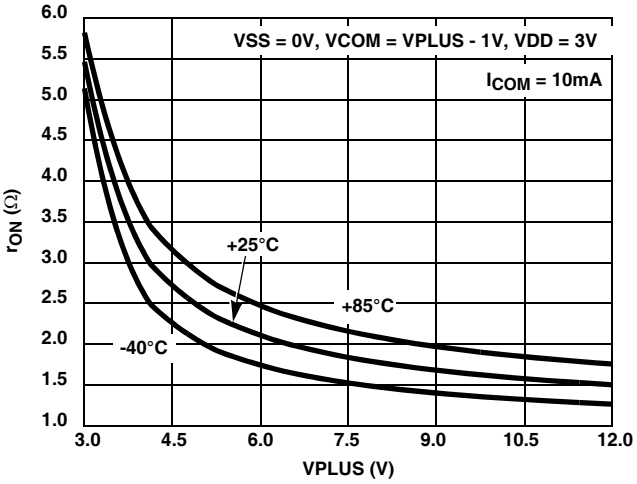


FIGURE 28. ON-RESISTANCE vs SUPPLY VOLTAGE

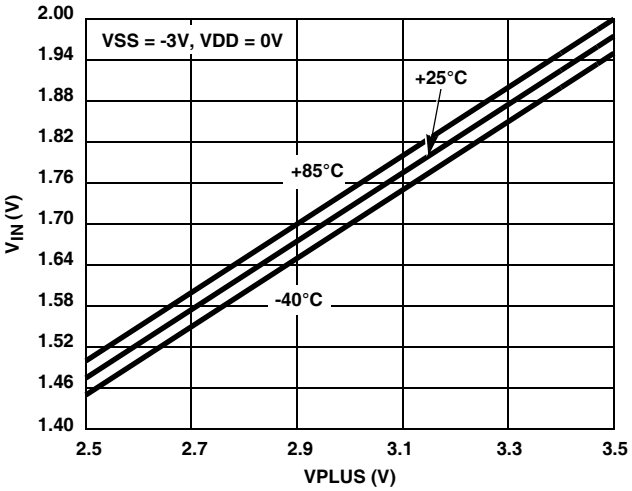


FIGURE 29. DIGITAL SWITCHING POINT vs SUPPLY VOLTAGE

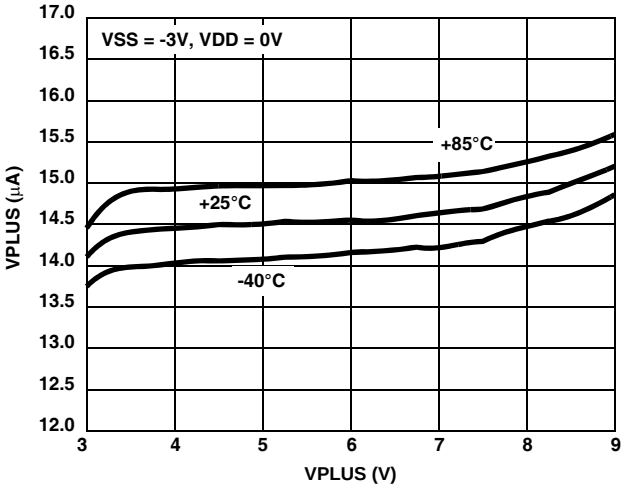


FIGURE 30. DEVICE QUIESCENT CURRENT (VPLUS)

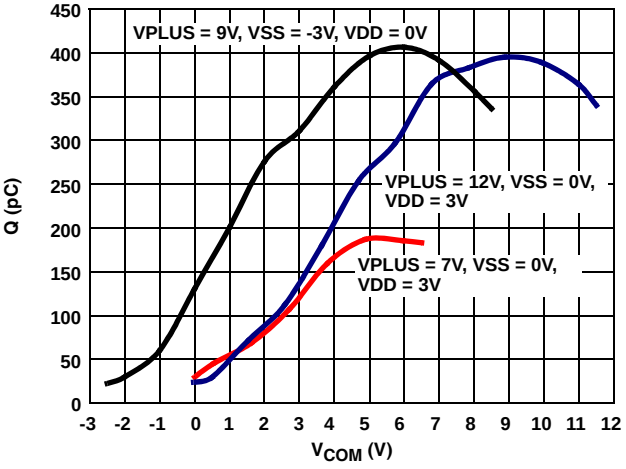


FIGURE 31. CHARGE INJECTION vs SWITCH VOLTAGE

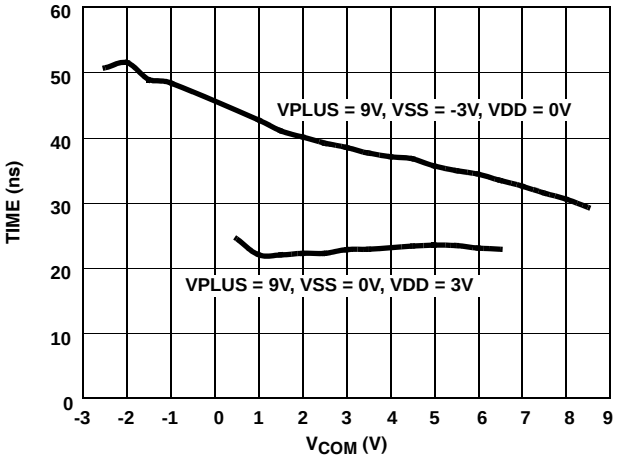


FIGURE 32. t_{ON} vs VCOM

Typical Performance Curves

VLOGIC = 3V, T_A = +25°C, V_{IH} = 3V, V_{IL} = 0V, Unless Otherwise Specified. **(Continued)**

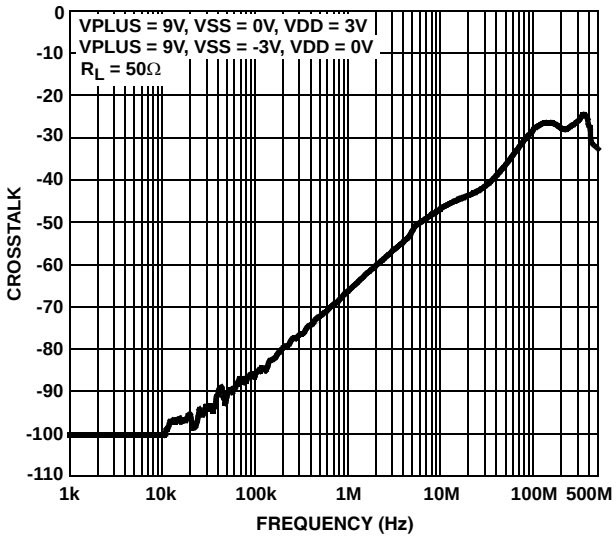


FIGURE 33. CROSSTALK

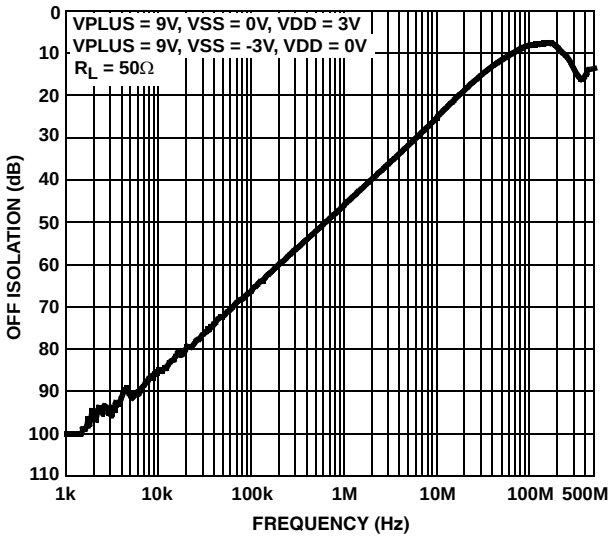


FIGURE 34. OFF-ISOLATION

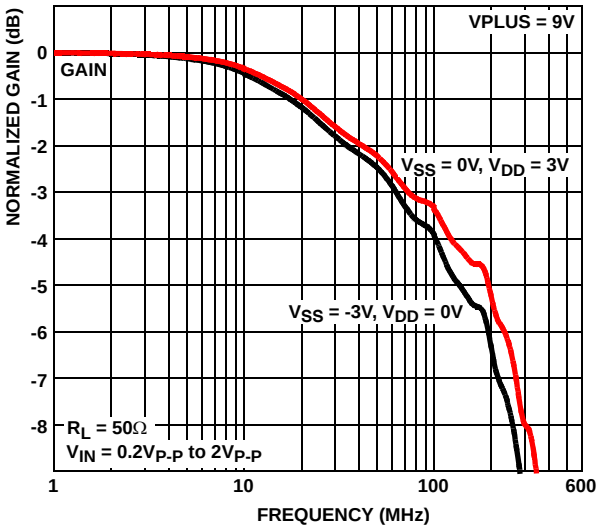


FIGURE 35. FREQUENCY RESPONSE

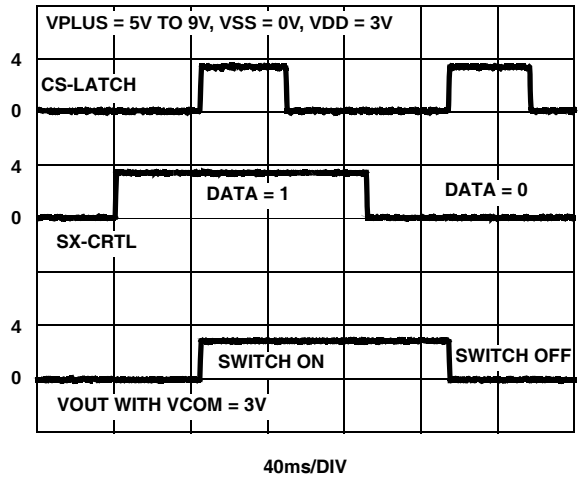
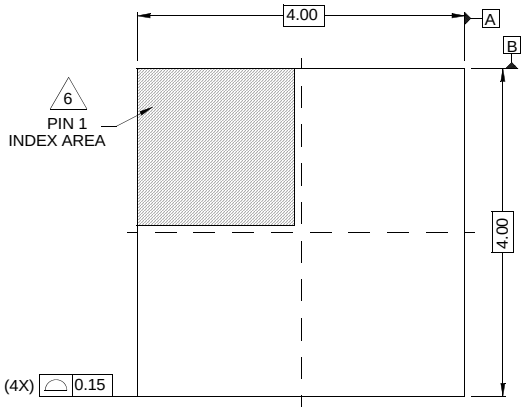


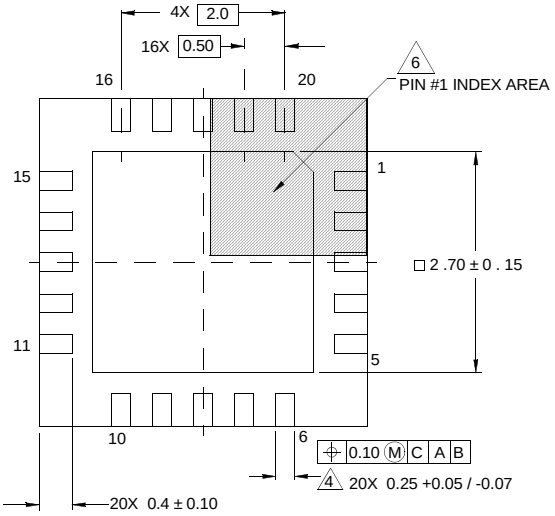
FIGURE 36. TIMING

L20.4x4C

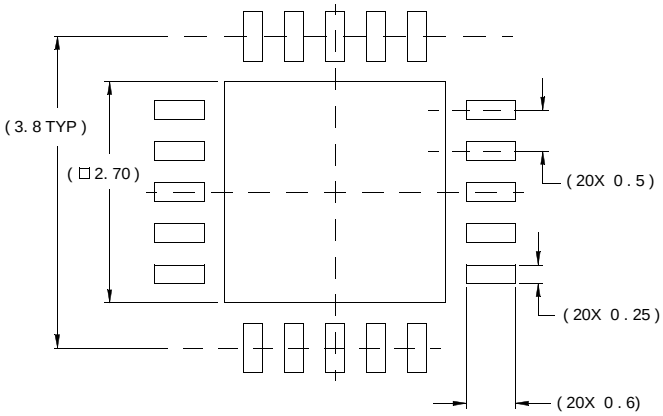
20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 11/06



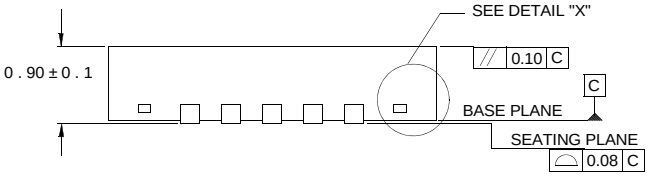
TOP VIEW



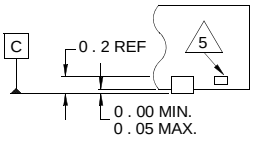
BOTTOM VIEW



TYPICAL RECOMMENDED LAND PATTERN



SIDE VIEW



DETAIL "X"

NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.