Data Sheet | February 8, 2006 | FN3550.6

Quad 125MHz Video Current Feedback Amplifier with Disable

The HA5024 is a quad version of the popular Intersil HA5020. It features wide bandwidth and high slew rate, and is optimized for video applications and gains between 1 and 10. It is a current feedback amplifier and thus yields less bandwidth degradation at high closed loop gains than voltage feedback amplifiers.

The low differential gain and phase, 0.1dB gain flatness, and ability to drive two back terminated 75Ω cables, make this amplifier ideal for demanding video applications.

The HA5024 also features a disable function that significantly reduces supply current while forcing the output to a true high impedance state. This functionality allows 2:1 and 4:1 video multiplexers to be implemented with a single IC.

The current feedback design allows the user to take advantage of the amplifier's bandwidth dependency on the feedback resistor. By reducing R_F, the bandwidth can be increased to compensate for decreases at higher closed loop gains or heavy output loads.

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
HA5024IP	HA5024IP	-40 to 85	20 Ld PDIP	E20.3
HA5024IPZ (Note)	HA5024IPZ	-40 to 85	20 Ld PDIP* (Pb-free)	E20.3
HA5024IB	HA5024IB	-40 to 85	20 Ld SOIC	M20.3
HA5024IBZ (Note)	HA5024IBZ	-40 to 85	20 Ld SOIC (Pb-free)	M20.3
HA5024IBZ96 (See Note)	HA5024IBZ	-40 to 85	20 Ld SOIC Tape and Reel (Pb-free)	M20.3
HA5024EVAL		High Speed Op Amp DIP Evaluation Board		

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Features

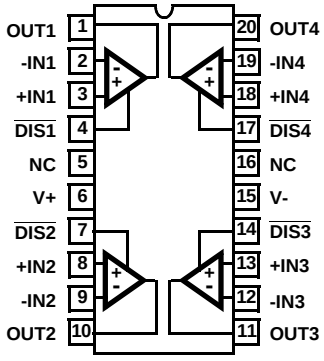
- Quad Version of HA-5020
- Individual Output Enable/Disable
- Input Offset Voltage 800µV
- Wide Unity Gain Bandwidth 125MHz
- Slew Rate 475V/µs
- Differential Gain 0.03%
- Differential Phase . . . . . 0.03 Degrees
- Supply Current (per Amplifier) 7.5mA
- ESD Protection 4000V
- Guaranteed Specifications at ±5V Supplies
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Video Multiplexers; Video Switching and Routing
- Video Gain Block
- Video Distribution Amplifier/RGB Amplifier
- Flash A/D Driver
- Current to Voltage Converter
- Medical Imaging
- Radar and Imaging Systems

Pinout

HA5024
(PDIP, SOIC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 36V
DC Input Voltage (Note 3) . . . . . $\pm V_{SUPPLY}$
Differential Input Voltage 10V
Output Current (Note 4) . . . . . Short Circuit Protected
ESD Rating (Note 3)
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 2000V

Operating Conditions

Temperature Range . . . . . -40℃ to 85℃
Supply Voltage Range (Typical) . . . . . ±4.5V to ±15V

Thermal Information

Thermal Resistance (Typical, Note 2)	θ_{JA} (℃/W)
PDIP Package*	75
SOIC Package	90

Maximum Junction Temperature (Note 1) . . . . . 175℃
Maximum Junction Temperature (Plastic Package, Note 1) . . . 150℃
Maximum Storage Temperature Range . . . . . -65℃ to 150℃
Maximum Lead Temperature (Soldering 10s) . . . . . 300℃
(SOIC - Lead Tips Only)

*Pb-free PDIPs can be used for through hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain junction temperature below 175℃ for die, and below 150℃ for plastic packages. See Application Information section for safe operating area information.
2. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.
3. The non-inverting input of unused amplifiers must be connected to GND.
4. Output is protected for short circuits to ground. Brief short circuits to ground will not degrade reliability, however, continuous (100% duty cycle) output current should not exceed 15mA for maximum reliability.

Electrical Specifications

$V_{SUPPLY} = \pm 5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 11) TEST LEVEL	TEMP. (℃)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage (V_{IO})		A	25	-	0.8	3	mV
		A	Full	-	-	5	mV
Delta V_{IO} Between Channels		A	Full	-	1.2	3.5	mV
Average Input Offset Voltage Drift		B	Full	-	5	-	µV/℃
V_{IO} Common Mode Rejection Ratio	Note 5	A	25	53	-	-	dB
		A	Full	50	-	-	dB
V_{IO} Power Supply Rejection Ratio	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	60	-	-	dB
		A	Full	55	-	-	dB
Input Common Mode Range	Note 5	A	Full	±2.5	-	-	V
Non-Inverting Input (+IN) Current		A	25	-	3	8	µA
		A	Full	-	-	20	µA
+IN Common Mode Rejection ($+I_{BCMR} = \frac{1}{R_{IN}}$)	Note 5	A	25	-	-	0.15	µA/V
		A	Full	-	-	0.5	µA/V
+IN Power Supply Rejection	$\pm 3.5V \leq V_S \leq \pm 6.5V$	A	25	-	-	0.1	µA/V
		A	Full	-	-	0.3	µA/V
Inverting Input (-IN) Current		A	25,85	-	4	12	µA
		A	-40	-	10	30	µA
Delta -IN BIAS Current Between Channels		A	25,85	-	6	15	µA
		A	-40	-	10	30	µA
-IN Common Mode Rejection	Note 5	A	25	-	-	0.4	µA/V
		A	Full	-	-	1.0	µA/V

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 11) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
-IN Power Supply Rejection	$\pm3.5V \leq V_S \leq \pm6.5V$	A	25	-	-	0.2	µA/V
		A	Full	-	-	0.5	µA/V
Input Noise Voltage	f = 1kHz	B	25	-	4.5	-	nV/√Hz
+Input Noise Current	f = 1kHz	B	25	-	2.5	-	pA/√Hz
-Input Noise Current	f = 1kHz	B	25	-	25.0	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Transimpedence	Note 16	A	25	1.0	-	-	MΩ
		A	Full	0.85	-	-	MΩ
Open Loop DC Voltage Gain	$R_L = 400\Omega$, $V_{OUT} = \pm2.5V$	25A	25	70	-	-	dB
		A	Full	65	-	-	dB
Open Loop DC Voltage Gain	$R_L = 100\Omega$, $V_{OUT} = \pm2.5V$	A	25	50	-	-	dB
		A	Full	45	-	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing	$R_L = 150\Omega$	A	25	±2.5	±3.0	-	V
		A	Full	±2.5	±3.0	-	V
Output Current	$R_L = 150\Omega$	B	Full	±16.6	±20.0	-	mA
Output Current, Short Circuit	$V_{IN} = \pm2.5V$, $V_{OUT} = 0V$	A	Full	±40	±60	-	mA
Output Current, Disabled (Note 5)	$\overline{DISABLE} = 0V$, $V_{OUT} = \pm2.5V$, $V_{IN} = 0V$	A	Full	-	-	2	µA
Output Disable Time	Note 12	B	25	-	40	-	µs
Output Enable Time	Note 13	B	25	-	40	-	ns
Output Capacitance Disabled	Note 14	B	25	-	15	-	pF
POWER SUPPLY CHARACTERISTICS							
Supply Voltage Range		A	25	5	-	15	V
Quiescent Supply Current		A	Full	-	7.5	10	mA/Op Amp
Supply Current, Disabled	$\overline{DISABLE} = 0V$	A	Full	-	5	7.5	mA/Op Amp
$\overline{Disable}$ Pin Input Current	$\overline{DISABLE} = 0V$	A	Full	-	1.0	1.5	mA
Minimum Pin 8 Current to Disable	Note 6	A	Full	350	-	-	µA
Maximum Pin 8 Current to Enable	Note 7	A	Full	-	-	20	µA
AC CHARACTERISTICS ($A_V = +1$)							
Slew Rate	Note 8	B	25	275	350	-	V/µs
Full Power Bandwidth	Note 9	B	25	22	28	-	MHz
Rise Time	Note 10	B	25	-	6	-	ns
Fall Time	Note 10	B	25	-	6	-	ns
Propagation Delay	Note 10	B	25	-	6	-	ns
Overshoot		B	25	-	4.5	-	%
-3dB Bandwidth	$V_{OUT} = 100mV$	B	25	-	125	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	75	-	ns

Electrical Specifications $V_{SUPPLY} = \pm5V$, $R_F = 1k\Omega$, $A_V = +1$, $R_L = 400\Omega$, $C_L \leq 10pF$, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 11) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
AC CHARACTERISTICS ($A_V = +2$, $R_F = 681\Omega$)							
Slew Rate	Note 8	B	25	-	475	-	V/µs
Full Power Bandwidth	Note 9	B	25	-	26	-	MHz
Rise Time	Note 10	B	25	-	6	-	ns
Fall Time	Note 10	B	25	-	6	-	ns
Propagation Delay	Note 10	B	25	-	6	-	ns
Overshoot		B	25	-	12	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	95	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	50	-	ns
Settling Time to 0.25%	2V Output Step	B	25	-	100	-	ns
Gain Flatness	5MHz	B	25	-	0.02	-	dB
	20MHz	B	25	-	0.07	-	dB
AC CHARACTERISTICS ($A_V = +10$, $R_F = 383\Omega$)							
Slew Rate	Note 8	B	25	350	475	-	V/µs
Full Power Bandwidth	Note 9	B	25	28	38	-	MHz
Rise Time	Note 10	B	25	-	8	-	ns
Fall Time	Note 10	B	25	-	9	-	ns
Propagation Delay	Note 10	B	25	-	9	-	ns
Overshoot		B	25	-	1.8	-	%
-3dB Bandwidth	V_{OUT} = 100mV	B	25	-	65	-	MHz
Settling Time to 1%	2V Output Step	B	25	-	75	-	ns
Settling Time to 0.1%	2V Output Step	B	25	-	130	-	ns
VIDEO CHARACTERISTICS							
Differential Gain (Note 15)	$R_L = 150\Omega$	B	25	-	0.03	-	%
Differential Phase (Note 15)	$R_L = 150\Omega$	B	25	-	0.03	-	Degrees

NOTES:

5. $V_{CM} = \pm2.5V$. At -40°C Product is tested at $V_{CM} = \pm2.25V$ because short test duration does not allow self heating.
6. $R_L = 100\Omega$, $V_{IN} = 2.5V$. This is the minimum current which must be pulled out of the $\overline{\text{Disable}}$ pin in order to disable the output. The output is considered disabled when $-10mV \leq V_{OUT} \leq +10mV$.
7. $V_{IN} = 0V$. This is the maximum current that can be pulled out of the $\overline{\text{Disable}}$ pin with the HA5024 remaining enabled. The HA5024 is considered disabled when the supply current has decreased by at least 0.5mA.
8. V_{OUT} switches from -2V to +2V, or from +2V to -2V. Specification is from the 25% to 75% points.
9. $FPBW = \frac{\text{Slew Rate}}{2\pi V_{PEAK}}$; $V_{PEAK} = 2V$.
10. $R_L = 100\Omega$, $V_{OUT} = 1V$. Measured from 10% to 90% points for rise/fall times; from 50% points of input and output for propagation delay.
11. A. Production Tested; B. Typical or Guaranteed Limit based on characterization; C. Design Typical for information only.
12. $V_{IN} = +2V$, $\overline{\text{DISABLE}} = +5V$ to 0V. Measured from the 50% point of $\overline{\text{DISABLE}}$ to $V_{OUT} = 0V$.
13. $V_{IN} = +2V$, $\overline{\text{DISABLE}} = 0V$ to +5V. Measured from the 50% point of $\overline{\text{DISABLE}}$ to $V_{OUT} = 2V$.
14. $V_{IN} = 0V$, Force V_{OUT} from 0V to $\pm2.5V$, $t_R = t_F = 50ns$, $\overline{\text{DISABLE}} = 0V$.
15. Measured with a VM700A video tester using an NTC-7 composite VITS.
16. $V_{OUT} = \pm2.5V$. At -40°C Product is tested at $V_{OUT} = \pm2.25V$ because short test duration does not allow self heating.

Test Circuits and Waveforms

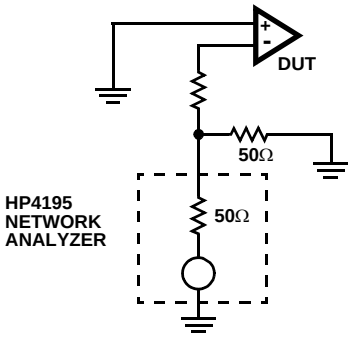


FIGURE 1. TEST CIRCUIT FOR TRANSIMPEDANCE MEASUREMENTS

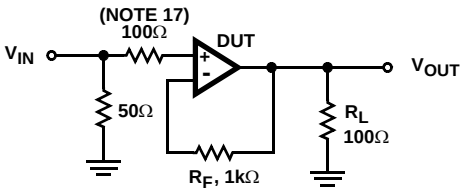


FIGURE 2. SMALL SIGNAL PULSE RESPONSE CIRCUIT

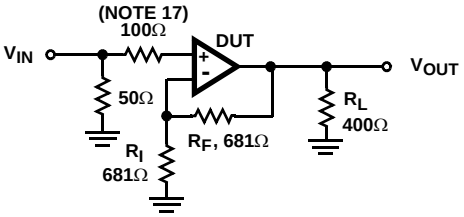
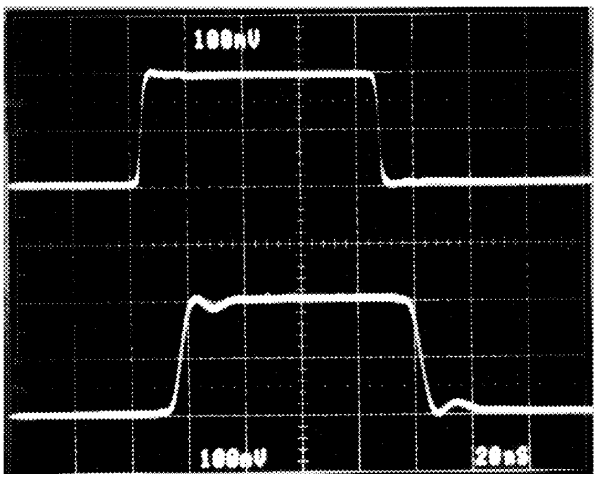


FIGURE 3. LARGE SIGNAL PULSE RESPONSE CIRCUIT

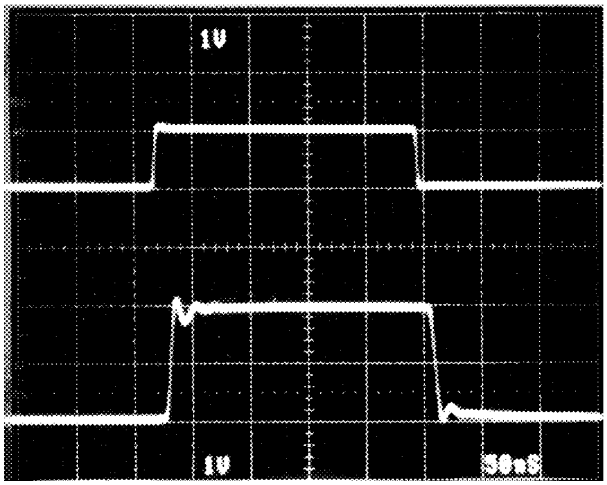
NOTE:

17. A series input resistor of ≥100Ω is recommended to limit input currents in case input signals are present before the HA5024 is powered up.



Vertical Scale: V_{IN} = 100mV/Div., V_{OUT} = 100mV/Div.

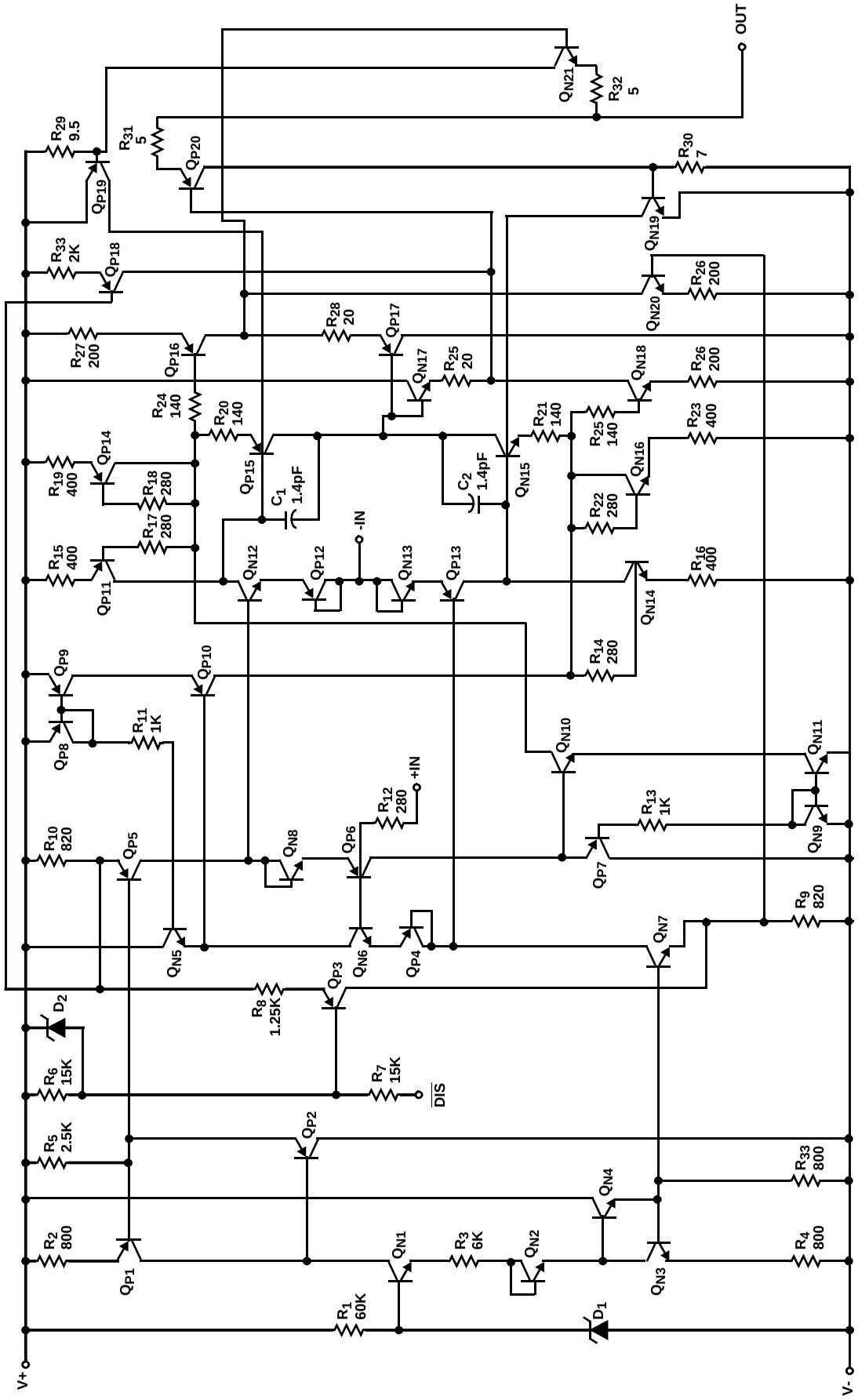
FIGURE 4. SMALL SIGNAL RESPONSE



Vertical Scale: V_{IN} = 1V/Div., V_{OUT} = 1V/Div.
Horizontal Scale: 50ns/Div.

FIGURE 5. LARGE SIGNAL RESPONSE

Schematic (One Amplifier of Four)



Application Information

Optimum Feedback Resistor

The plots of inverting and non-inverting frequency response, see Figure 11 and Figure 12 in the Typical Performance Curves section, illustrate the performance of the HA5024 in various closed loop gain configurations. Although the bandwidth dependency on closed loop gain isn't as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier's unique relationship between bandwidth and R_F. All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier's bandwidth is inversely proportional to R_F. The HA5024 design is optimized for a 1000Ω R_F at a gain of +1. Decreasing R_F in a unity gain application decreases stability, resulting in excessive peaking and overshoot. At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

The table below lists recommended R_F values for various gains, and the expected bandwidth.

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	750	100
+1	1000	125
+2	681	95
+5	1000	52
+10	383	65
-10	750	22

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. The use of low inductance components such as chip resistors and chip capacitors is strongly recommended. If leaded components are used the leads must be kept short especially for the power supply decoupling components and those components connected to the inverting input.

Attention must be given to decoupling the power supplies. A large value (10μF) tantalum or electrolytic capacitor in parallel with a small value (0.1μF) chip capacitor works well in most cases.

A ground plane is strongly recommended to control noise. Care must also be taken to minimize the capacitance to ground seen by the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. It is recommended that the ground plane be removed under traces connected to -IN, and that connections to -IN be kept as short as possible to minimize the capacitance from this node to ground.

Driving Capacitive Loads

Capacitive loads will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases the oscillation can be avoided by placing an isolation resistor (R) in series with the output as shown in Figure 6.

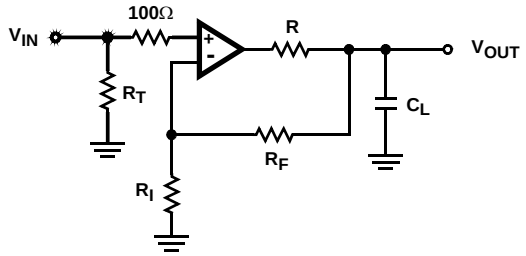


FIGURE 6. PLACEMENT OF THE OUTPUT ISOLATION RESISTOR, R

The selection criteria for the isolation resister is highly dependent on the load, but 27Ω has been determined to be a good starting value.

Power Dissipation Considerations

Due to the high supply current inherent in quad amplifiers, care must be taken to insure that the maximum junction temperature (T_J, see Absolute Maximum Ratings) is not exceeded. Figure 7 shows the maximum ambient temperature versus supply voltage for the available package styles (Plastic DIP, SOIC). At $\pm 5V_{DC}$ quiescent operation both package styles may be operated over the full industrial range of -40°C to 85°C. It is recommended that thermal calculations, which take into account output power, be performed by the designer.

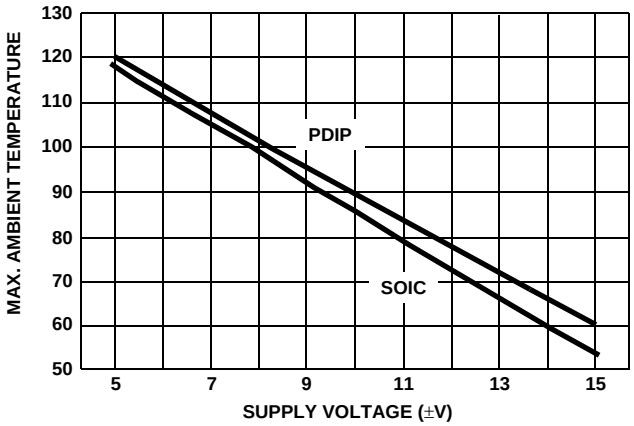


FIGURE 7. MAXIMUM OPERATING AMBIENT TEMPERATURE vs SUPPLY VOLTAGE

Enable/Disable Function

When enabled the amplifier functions as a normal current feedback amplifier with all of the data in the electrical specifications table being valid and applicable. When disabled the amplifier output assumes a true high impedance state and the supply current is reduced significantly.

The circuit shown in Figure 8 is a simplified schematic of the enable/disable function. The large value resistors in series with the DISABLE pin makes it appear as a current source to the driver. When the driver pulls this pin low current flows out of the pin and into the driver. This current, which may be as large as 350μA when external circuit and process variables are at their extremes, is required to insure that point “A” achieves the proper potential to disable the output.The driver must have the compliance and capability of sinking all of this current.

When V_{CC} is +5V the DISABLE pin may be driven with a dedicated TTL gate. The maximum low level output voltage of the TTL gate, 0.4V, has enough compliance to insure that the amplifier will always be disabled even though D_1 will not turn on, and the TTL gate will sink enough current to keep point “A” at its proper voltage. When V_{CC} is greater than +5V the DISABLE pin should be driven with an open collector device that has a breakdown rating greater than V_{CC}.

Referring to Figure 8, it can be seen that R_6 will act as a pull-up resistor to $+V_{CC}$ if the DISABLE pin is left open. In those cases where the enable/disable function is not required on all circuits some circuits can be permanently enabled by letting the DISABLE pin float. If a driver is used to set the enable/disable level, be sure that the driver does not sink more than 20μA when the DISABLE pin is at a high level. TTL gates, especially CMOS versions, do not violate this criteria so it is permissible to control the enable/disable function with TTL.

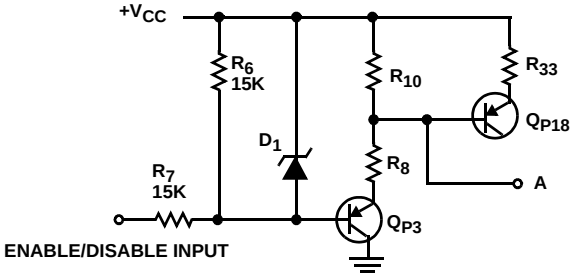


FIGURE 8. SIMPLIFIED SCHEMATIC OF ENABLE/DISABLE FUNCTION

Typical Applications

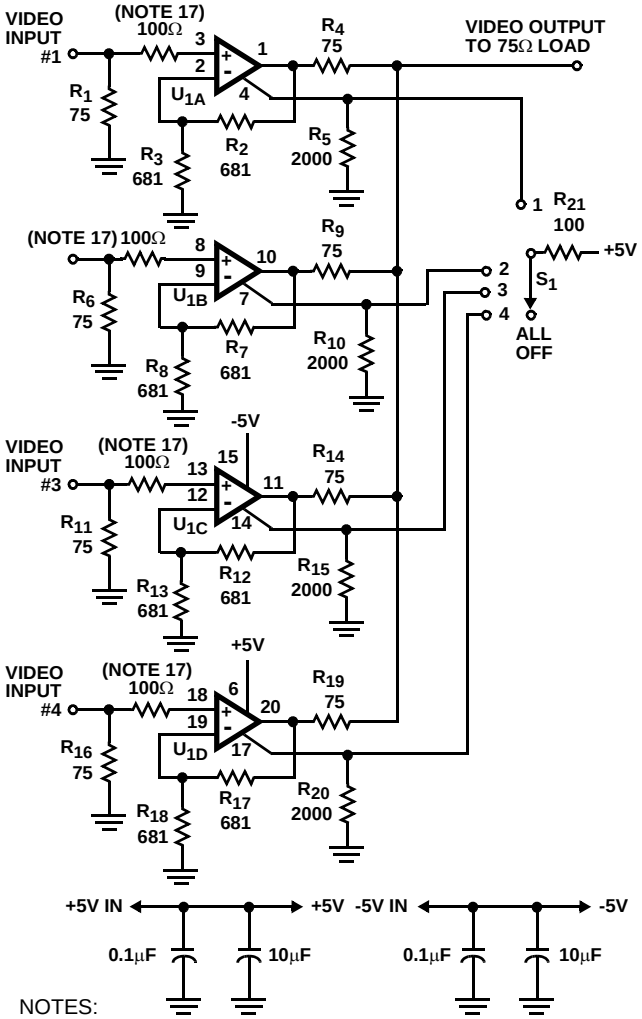
Four Channel Video Multiplexer

Referring to the amplifier U_{1A} in Figure 9, R_1 terminates the cable in its characteristic impedance of 75Ω, and R_4 back terminates the cable in its characteristic impedance. The amplifier is set up in a gain configuration of +2 to yield an overall network gain of +1 when driving a double terminated cable. The value of R_3 can be changed if a different network gain is desired. R_5 holds the disable pin at ground thus inhibiting the amplifier until the switch, S_1, is thrown to position 1. At position 1 the switch pulls the disable pin up to the plus supply rail thereby enabling the amplifier. Since all of the actual signal switching takes place within the amplifier, its differential gain and phase parameters, which are 0.03% and 0.03 degrees respectively, determine the circuit’s performance. The other three circuits, U_{1B} through U_{1D}, operate in a similar manner.

When the plus supply rail is 5V the disable pin can be driven by a dedicated TTL gate as discussed earlier. If a multiplexer IC or its equivalent is used to select channels its logic must be break before make. When these conditions are satisfied the HA5024IP is often used as a remote video multiplexer, and the multiplexer may be extended by adding more amplifier ICs.

Low Impedance Multiplexer

Two common problems surface when you try to multiplex multiple high speed signals into a low impedance source such as an A/D converter. The first problem is the low source impedance which tends to make amplifiers oscillate and causes gain errors. The second problem is the multiplexer which supplies no gain, introduces all kinds of distortion and limits the frequency response. Using op amps which have an enable/disable function, such as the HA5024, eliminates the multiplexer problems because the external mux chip is not needed, and the HA5024 can drive low impedance (large capacitance) loads if a series isolation resistor is used.

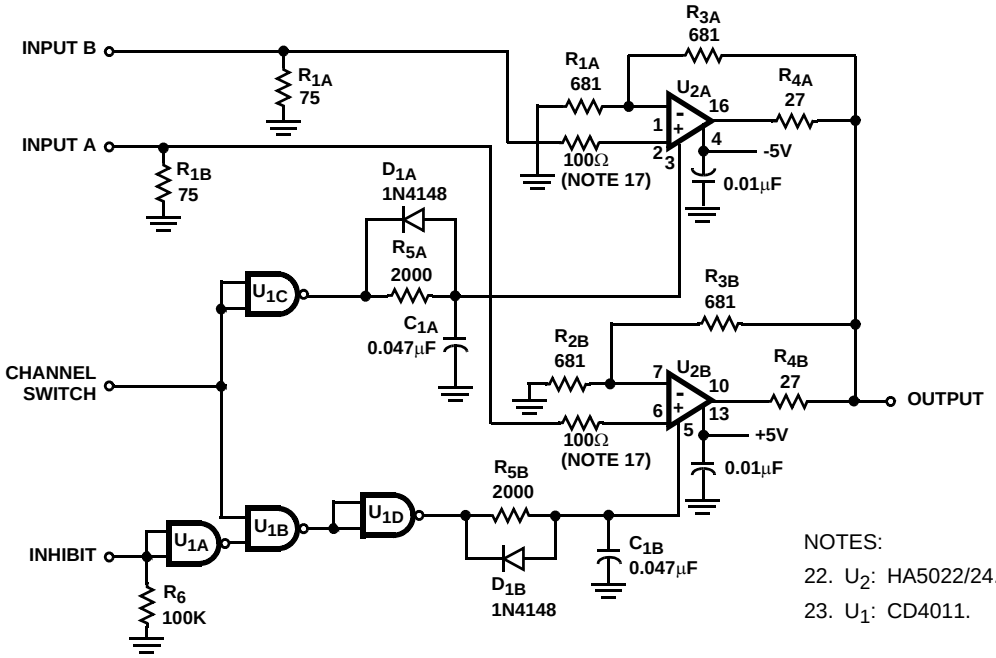


NOTES:
18. U_1 is HA5024IP.
19. All resistors in Ω.
20. S_1 is break before make.
21. Use ground plane.

FIGURE 9. FOUR CHANNEL VIDEO MULTIPLEXER

Referring to Figure 10, both inputs are terminated in their characteristic impedance; 75Ω is typical for video applications. Since the drivers usually are terminated in their characteristic impedance the input gain is 0.5, thus the amplifiers, U_2, are configured in a gain of +2 to set the circuit gain equal to one. Resistors R_2 and R_3 determine the amplifier gain, and if a different gain is desired R_2 should be changed according to the equation $G = (1 + R_3/R_2)$. R_3 sets the frequency response of the amplifier so you should refer to the manufacturers data sheet before changing its value. R_5, C_1 and D_1 are an asymmetrical charge/discharge time circuit which configures U_1 as a break before make switch to prevent both amplifiers from being active simultaneously. If this design is extended to more channels the drive logic must be designed to be break before make. R_4 is enclosed in the feedback loop of the amplifier so that the large open loop amplifier gain of U_2 will present the load with a small closed loop output impedance while keeping the amplifier stable for all values of load capacitance.

The circuit shown in Figure 10 was tested for the full range of capacitor values with no oscillations being observed; thus, problem one has been solved.The frequency and gain characteristics of the circuit are now those of the amplifier independent of any multiplexing action; thus, problem two has been solved. The multiplexer transition time is approximately 15μs with the component values shown.



NOTES:

22. U_2: HA5022/24.
23. U_1: CD4011.

FIGURE 10. LOW IMPEDANCE MULTIPLEXER

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified

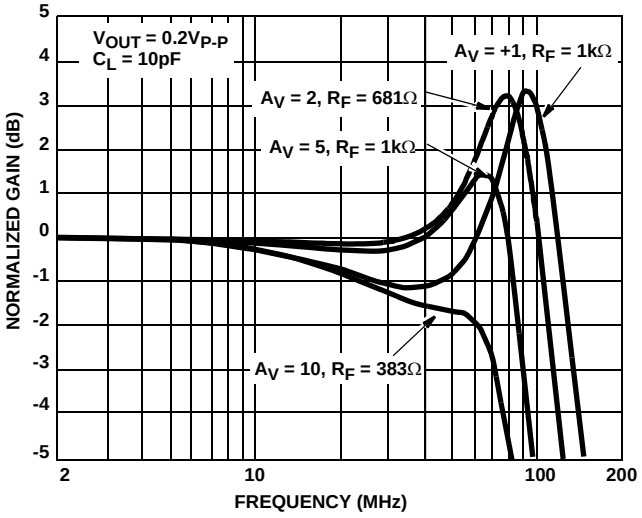


FIGURE 11. NON-INVERTING FREQUENCY RESPONSE

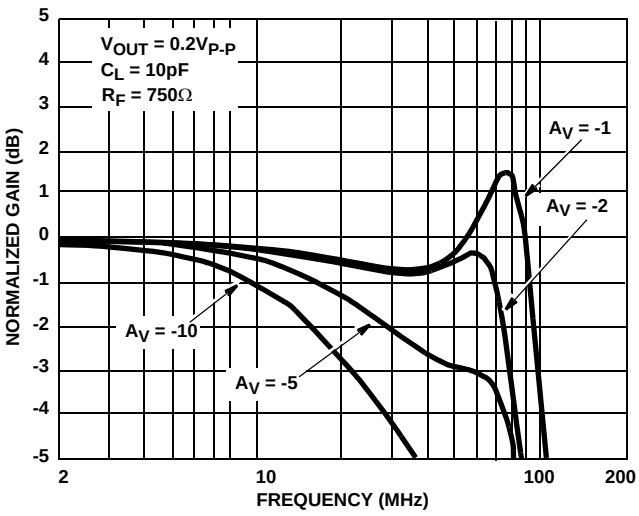


FIGURE 12. INVERTING FREQUENCY RESPONSE

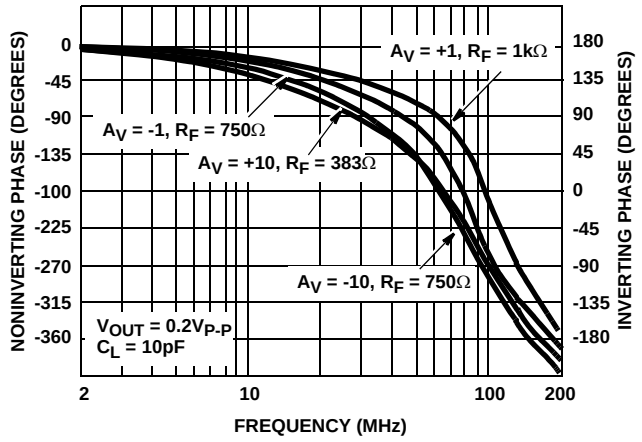


FIGURE 13. PHASE RESPONSE AS A FUNCTION OF FREQUENCY

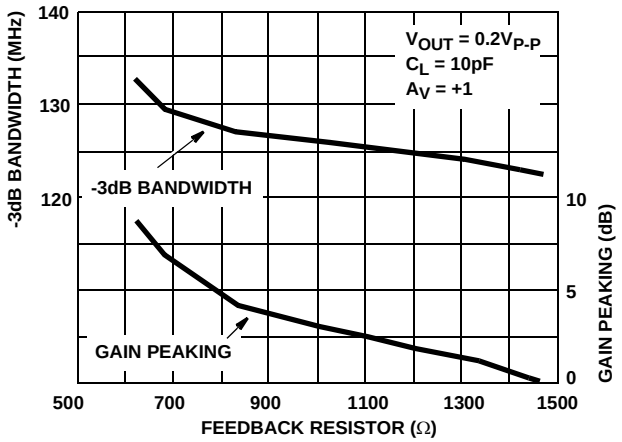


FIGURE 14. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

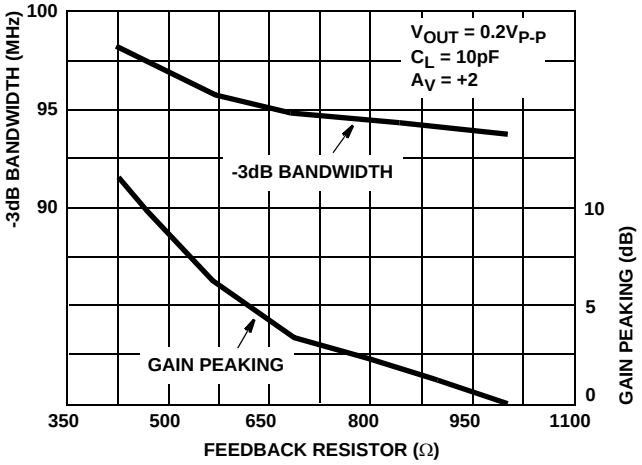


FIGURE 15. BANDWIDTH AND GAIN PEAKING vs FEEDBACK RESISTANCE

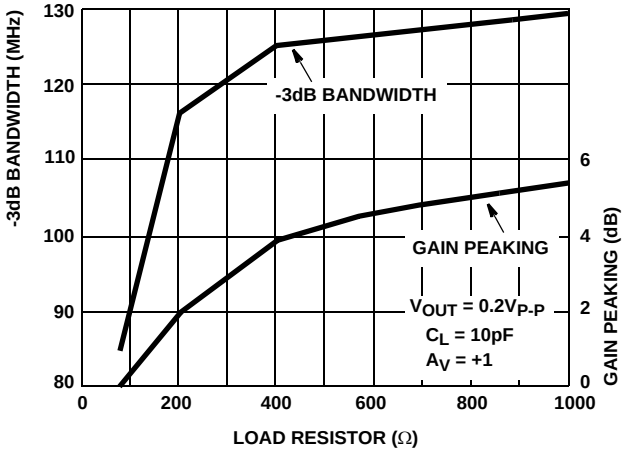


FIGURE 16. BANDWIDTH AND GAIN PEAKING vs LOAD RESISTANCE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

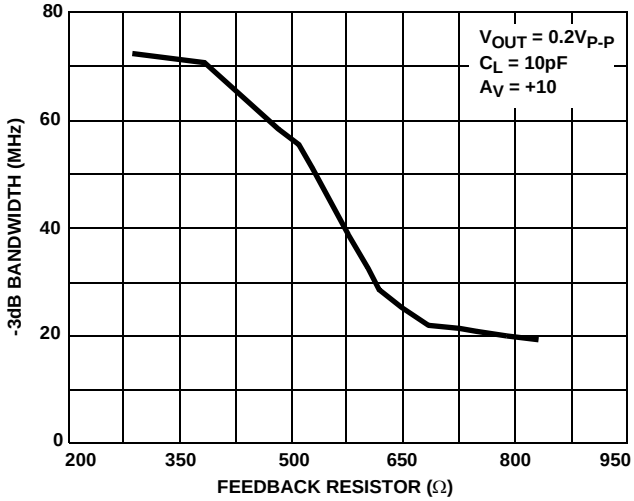


FIGURE 17. BANDWIDTH vs FEEDBACK RESISTANCE

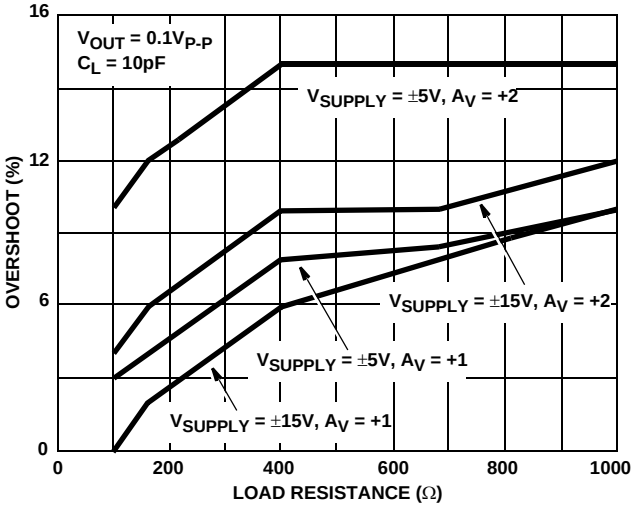


FIGURE 18. SMALL SIGNAL OVERSHOOT vs LOAD RESISTANCE

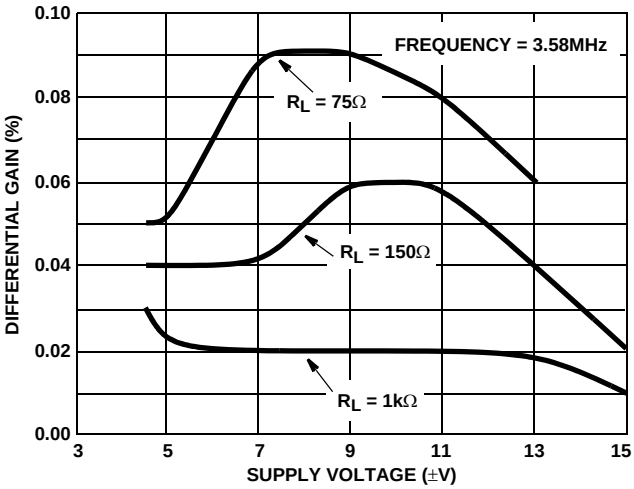


FIGURE 19. DIFFERENTIAL GAIN vs SUPPLY VOLTAGE

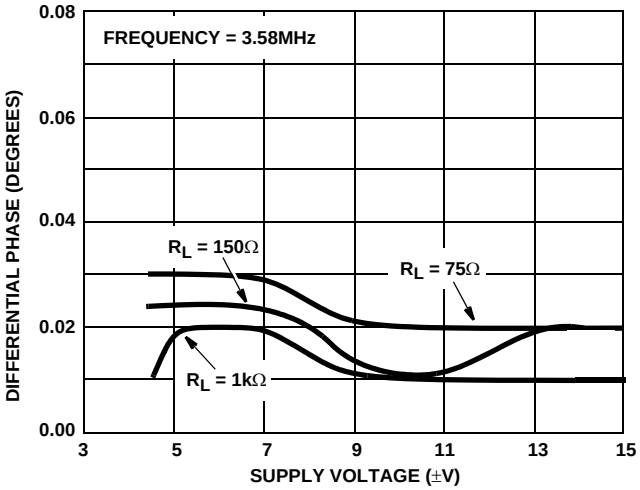


FIGURE 20. DIFFERENTIAL PHASE vs SUPPLY VOLTAGE

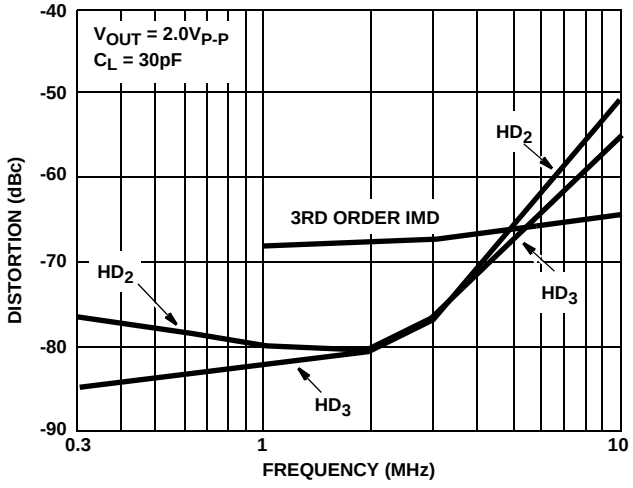


FIGURE 21. DISTORTION vs FREQUENCY

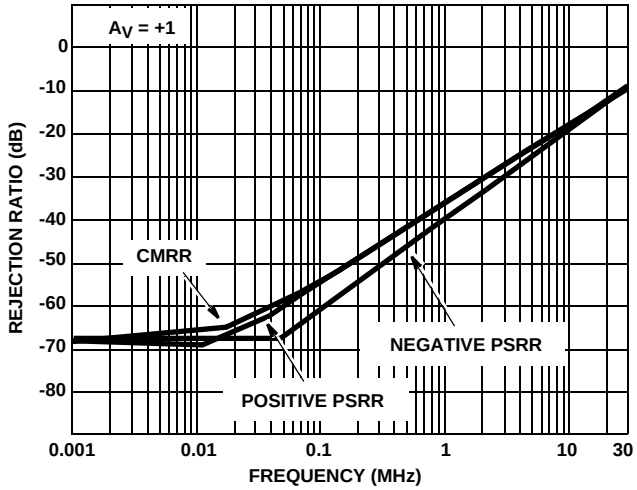


FIGURE 22. REJECTION RATIOS vs FREQUENCY

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

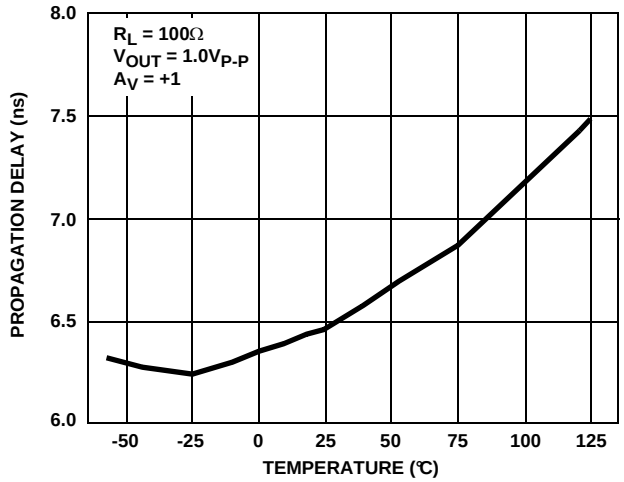


FIGURE 23. PROPAGATION DELAY vs TEMPERATURE

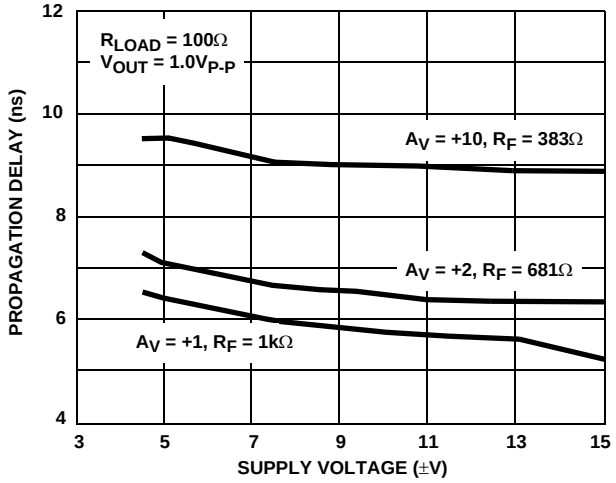


FIGURE 24. PROPAGATION DELAY vs SUPPLY VOLTAGE

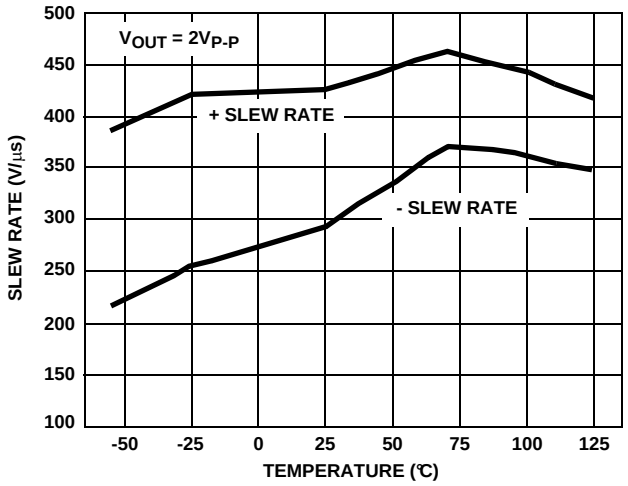


FIGURE 25. SLEW RATE vs TEMPERATURE

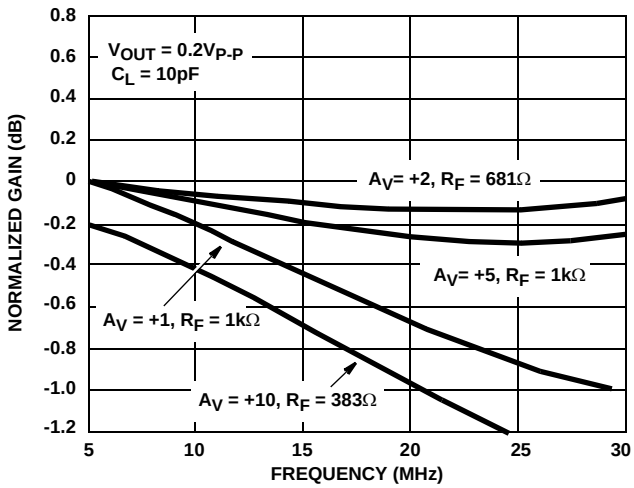


FIGURE 26. NON-INVERTING GAIN FLATNESS vs FREQUENCY

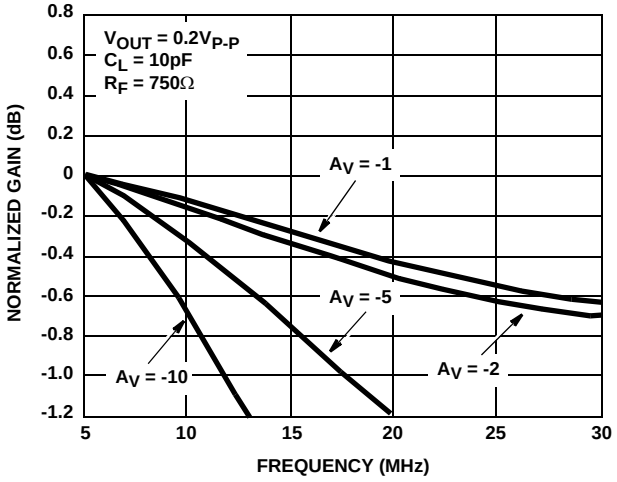


FIGURE 27. INVERTING GAIN FLATNESS vs FREQUENCY

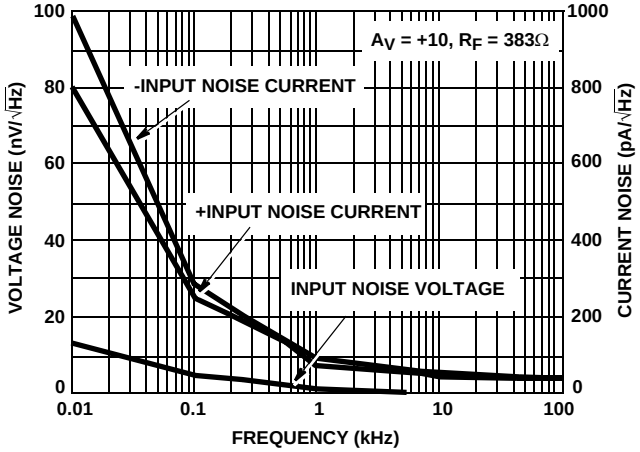


FIGURE 28. INPUT NOISE CHARACTERISTICS

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25℃$, Unless Otherwise Specified **(Continued)**

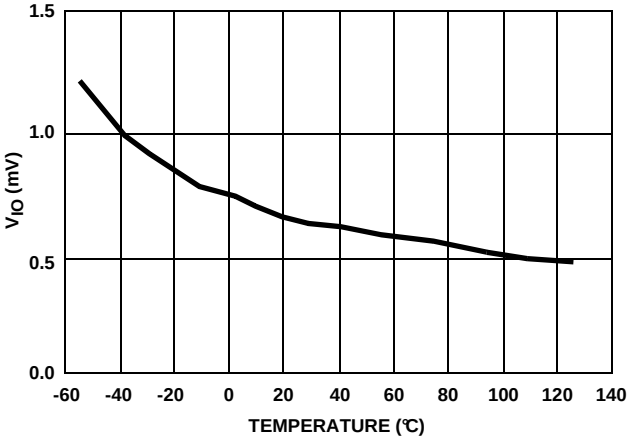


FIGURE 29. INPUT OFFSET VOLTAGE vs TEMPERATURE

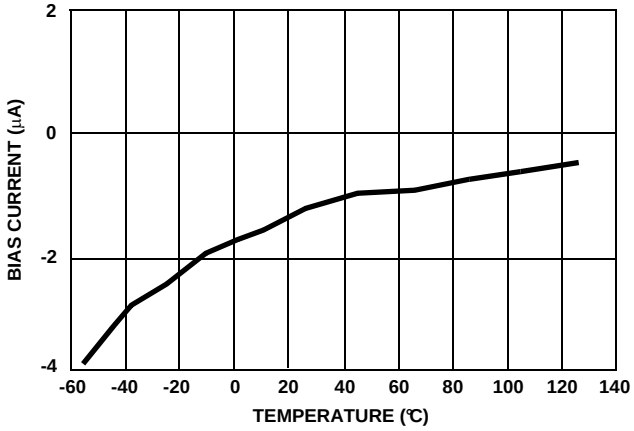


FIGURE 30. +INPUT BIAS CURRENT vs TEMPERATURE

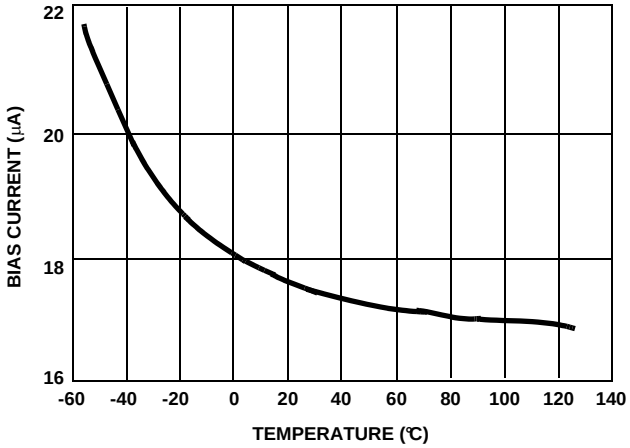


FIGURE 31. -INPUT BIAS CURRENT vs TEMPERATURE

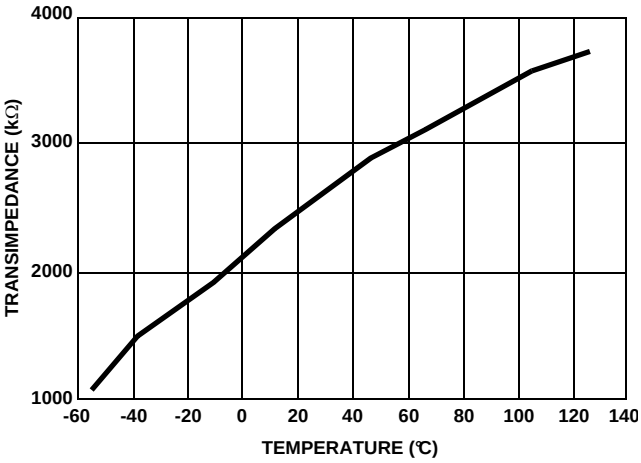


FIGURE 32. TRANSIMPEDANCE vs TEMPERATURE

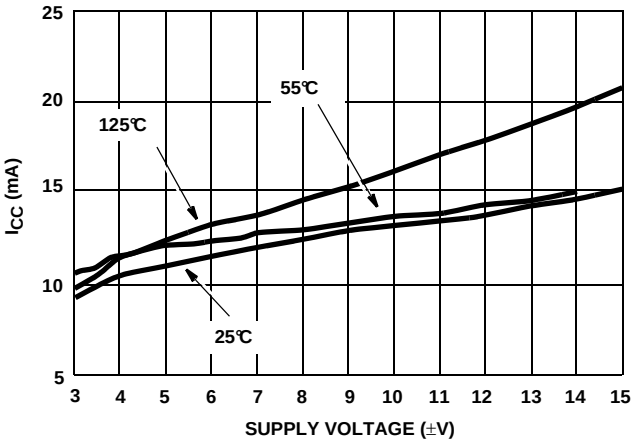


FIGURE 33. SUPPLY CURRENT vs SUPPLY VOLTAGE

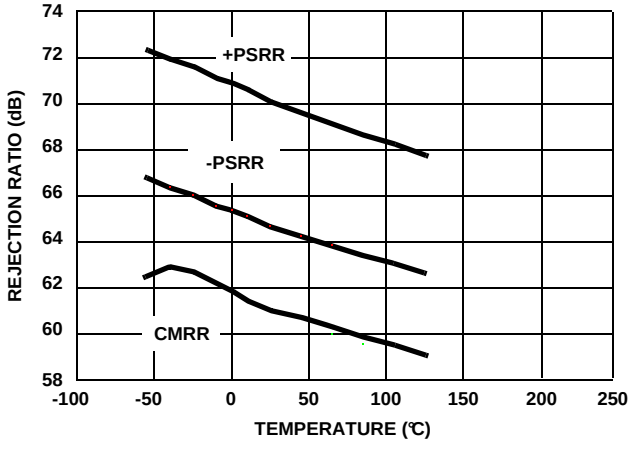


FIGURE 34. REJECTION RATIO vs TEMPERATURE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25℃$, Unless Otherwise Specified **(Continued)**

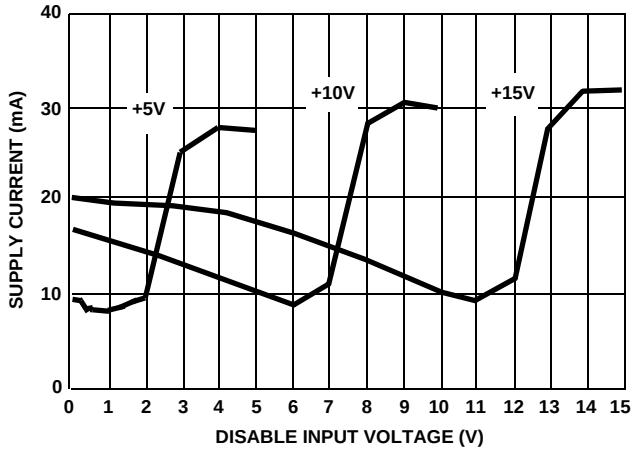


FIGURE 35. SUPPLY CURRENT vs DISABLE INPUT VOLTAGE

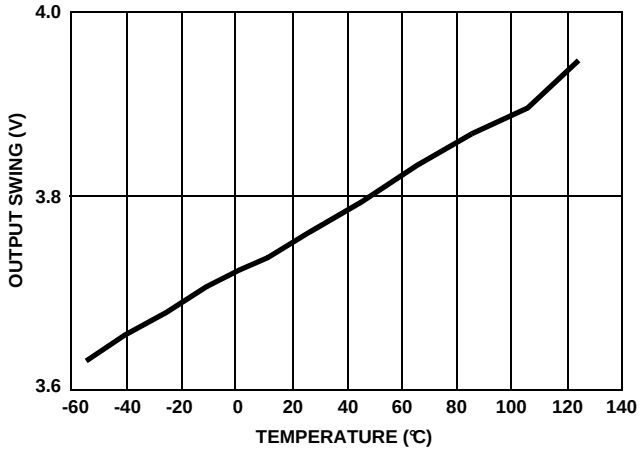


FIGURE 36. OUTPUT SWING vs TEMPERATURE

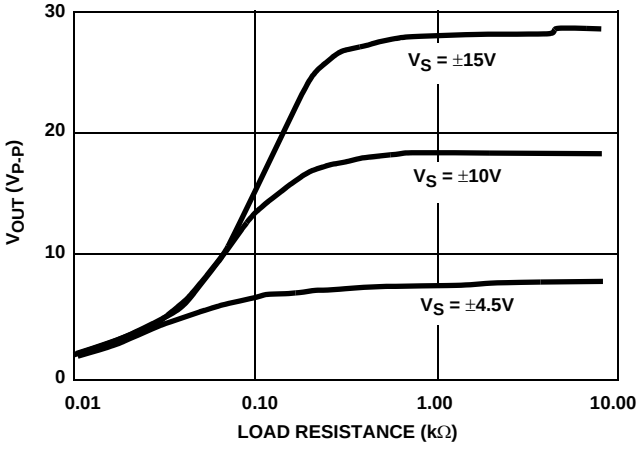


FIGURE 37. OUTPUT SWING vs LOAD RESISTANCE

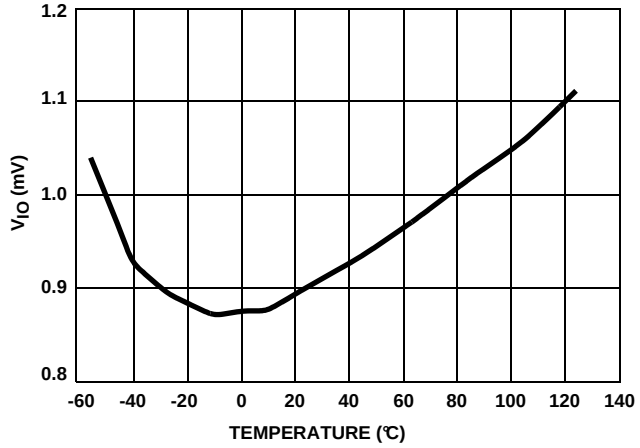


FIGURE 38. INPUT OFFSET VOLTAGE CHANGE BETWEEN CHANNELS vs TEMPERATURE

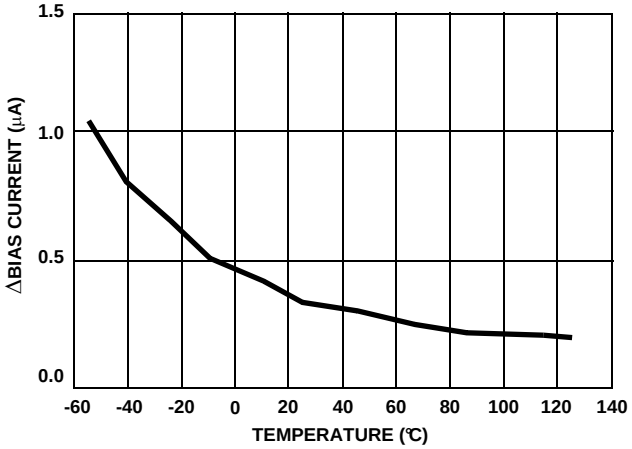


FIGURE 39. INPUT BIAS CURRENT CHANGE BETWEEN CHANNELS vs TEMPERATURE

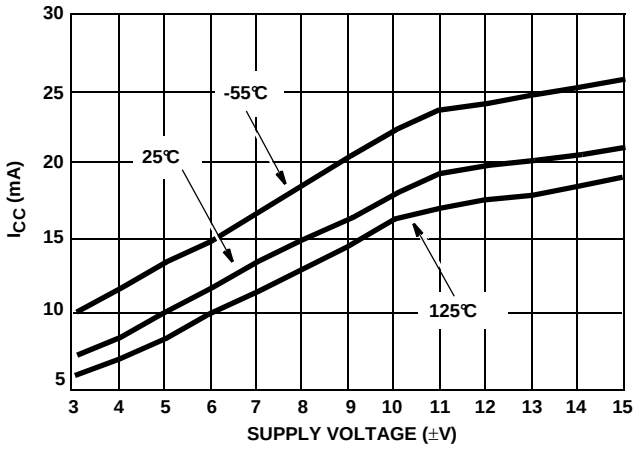


FIGURE 40. DISABLE SUPPLY CURRENT vs SUPPLY VOLTAGE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, $A_V = +1$, $R_F = 1k\Omega$, $R_L = 400\Omega$, $T_A = 25°C$, Unless Otherwise Specified **(Continued)**

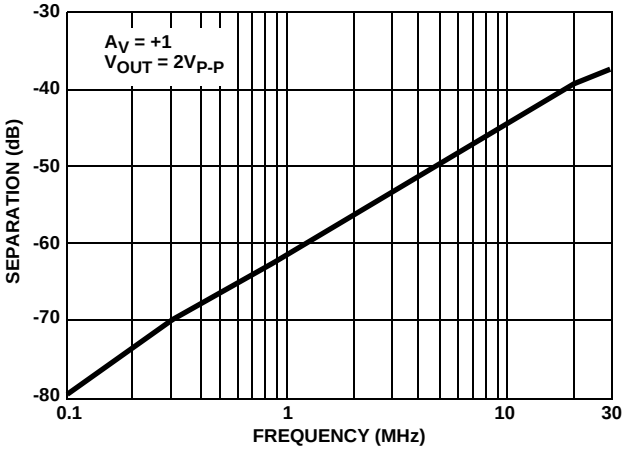


FIGURE 41. CHANNEL SEPARATION vs FREQUENCY

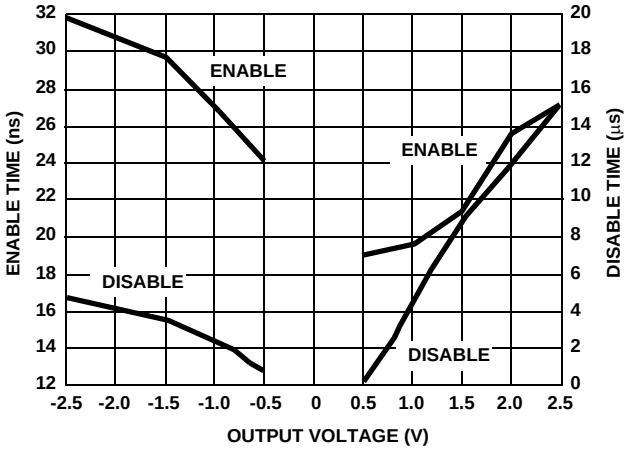


FIGURE 42. ENABLE/DISABLE TIME vs OUTPUT VOLTAGE

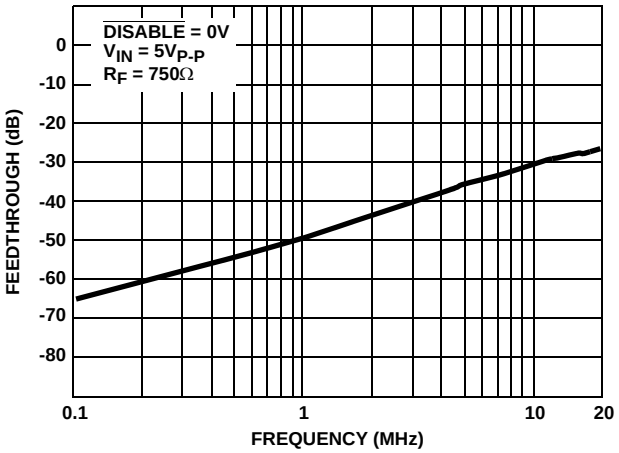


FIGURE 43. DISABLE FEEDTHROUGH vs FREQUENCY

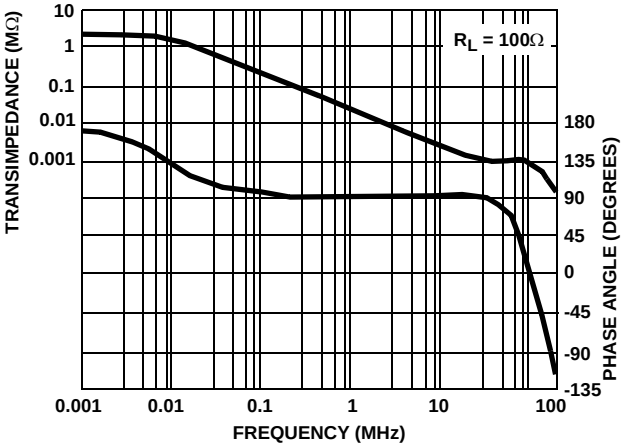


FIGURE 44. TRANSIMPEDANCE vs FREQUENCY

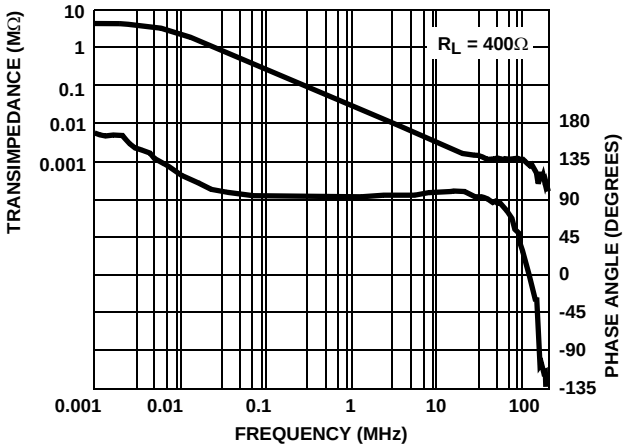


FIGURE 45. TRANSIMPEDENCE vs FREQUENCY

Die Characteristics

DIE DIMENSIONS:

2680µm x 2600µm x 483µm

METALLIZATION:

Type: Metal 1: AlCu (1%)
Thickness: Metal 1: 8kÅ ±0.4kÅ

Type: Metal 2: AlCu (1%)
Thickness: Metal 2: 16kÅ ±0.8kÅ

SUBSTRATE POTENTIAL (Powered Up):

V-

PASSIVATION:

Type: Nitride
Thickness: 4kÅ ±0.4kÅ

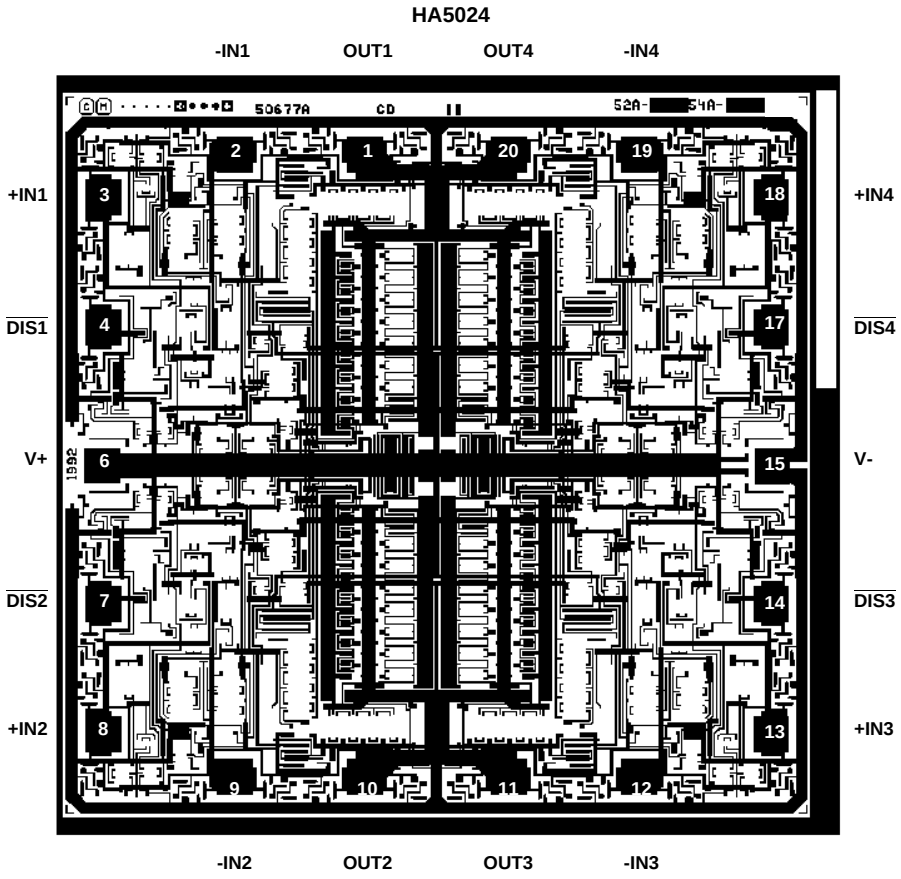
TRANSISTOR COUNT:

248

PROCESS:

High Frequency Bipolar Dielectric Isolation

Metallization Mask Layout



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Intersil Corporation's quality certifications can be viewed at www.intersil.com/design/quality