Data Sheet | October 30, 2007 | FN6513.2

Integrated Audio Amplifier Systems

The Intersil ISL54004 device is an integrated audio power amplifier system that combines a mono BTL amplifier and stereo headphone amplifiers in a single device. It can operate from a single +2.7V to +5V power supply and is offered in a 20 Ld 4x4 TQFN package. Targeted applications include handheld equipment such as cell-phones, MP3 players, and games/toys.

The ISL54004 part contains one class AB BTL type power amplifier for driving an 8Ω mono speaker and two class AB headphone amplifiers for driving 16Ω or 32Ω headphone speakers.

The BTL when using a 5V supply is capable of delivering 800mW (typ) with 0.4% THD+N and 941mW (typ) with 1% THD+N of continuous average power into an 8Ω BTL speaker load.

Each headphone amplifier when using a 5V supply is capable of delivering 50mW (typ) with 0.3% THD+N and 94mW (typ) with 1% THD+N of continuous average power into a 32Ω headphone speaker.

When in Mono mode the part automatically mixes the left and right audio inputs and sends the combined signal to the BTL driver. In Headphone Mode, the active right channel input is sent to the right headphone speaker and the active left channel is sent to the left headphone speaker.

The ISL54004 has a four-level programmable gain stage to boost the audio signal. The part requires no external gain setting resistors.

The ISL54004 part features headphone sense input circuitry that detects when a headphone jack has been inserted and automatically switches the audio inputs from the mono BTL output driver to the headphone drivers. The part also has a logic control pin that can override the headphone sense input circuitry.

The part also features low power shutdown, thermal overload protection and click and pop suppression. The click and pop circuitry prevents click and pops at the speakers when transitioning in and out of shutdown.

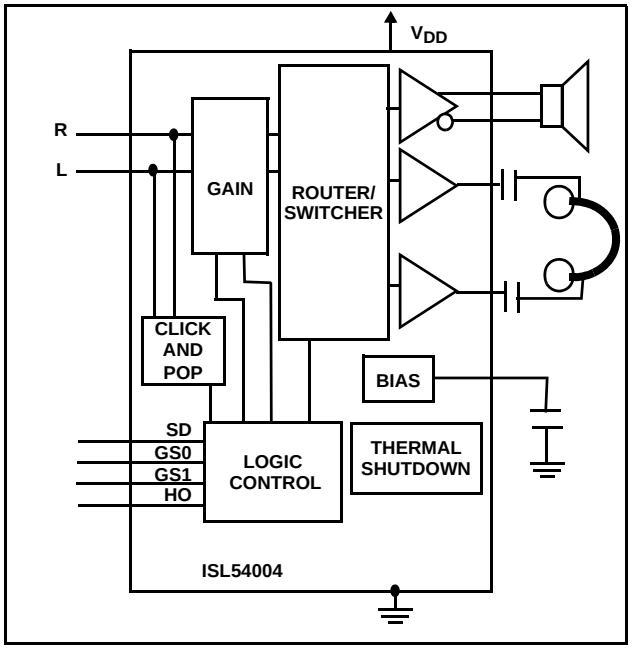
Features

- Class AB 94mW Headphone Amplifiers and 941mW Mono BTL Speaker Amplifier
- THD+N at 1kHz, 800mW into 8Ω BTL 0.4%
- THD+N at 1kHz, 15mW into 32Ω Headphone 0.07%
- THD+N at 1kHz, 50mW into 32Ω Headphone 0.3%
- Single Supply Operation . . . . . .+2.7V to +5.5V
- Headphone Sense Input and Low Power Shutdown
- Thermal Shutdown Protection
- “Click and Pop” Suppression Circuitry
- Selectable Gain Settings
- TTL Logic-Compatible
- Available in 20 Ld 4x4 TQFN
- Pb-Free (RoHS Compliant)

Applications

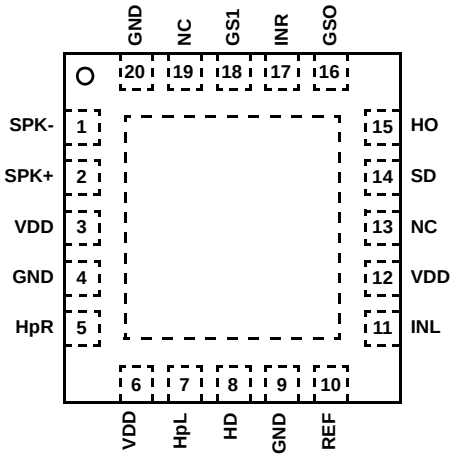
- Battery-powered, Handheld, and Portable Equipment
  - Cellular/mobile Phones
  - PDA’s, MP3 Players, DVD Players, Cameras
  - Laptops, Notebooks, Palmtops
  - Handheld Games and Toys
- Desktop Computers

Simplified Block Diagram



Pinout

ISL54004
(20 LD 4X4 TQFN)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL54004IRTZ* (Note)	540 04IRTZ	-40 to +85	20 Ld 4x4 TQFN Tape and Reel (Pb-free)	L20.4x4A

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pin Descriptions

PIN	NAME	FUNCTION
3, 6, 12	VDD	System Power Supply
4, 9, 20	GND	Ground Connection
11	INL	Left Channel Audio Input 1
17	INR	Right Channel Audio Input 1
5	HpR	Headphone Right Ouput
7	HpL	Headphone Left Ouput
2	SPK+	Positive Speaker Output
1	SPK-	Negative Speaker Output
14	SD	Shutdown, High to disable amplifiers, Low for normal operation.
8	HD	Headphone Detection, Internally pulled up to V_{DD}, Low in Mono Mode, High in Headphone Mode if HO = Low
15	HO	Headphone Override, High in Mono Mode, Low in Headphone Mode if HD = High
16, 18	GS_	Gain Select
10	REF	Common-mode Bias Voltage, By-pass with a 1µF capacitor to GND.
13, 19	NC	No Connect

ISL54004 Truth Table

SD	GS1	GS0	HD	HO	SPK+/SPK-	HpR	HpL
1	X	X	X	X	Disabled	Disabled	Disabled
0	0	0	0	X	$IN_R + IN_L$	-	-
0	0	0	1	0	-	IN_R	IN_L
0	0	0	1	1	$IN_R + IN_L$	-	-
0	0	1	0	X	$1.2 \times (IN_R + IN_L)$	-	-
0	0	1	1	0	-	$1.2 \times IN_R$	$1.2 \times IN_L$
0	0	1	1	1	$1.2 \times (IN_R + IN_L)$	-	-
0	1	0	0	X	$2 \times (IN_R + IN_L)$	-	-
0	1	0	1	0	-	$2 \times IN_R$	$2 \times IN_L$
0	1	0	1	1	$2 \times (IN_R + IN_L)$	-	-
0	1	1	0	X	$4 \times (IN_R + IN_L)$	-	-
0	1	1	1	0	-	$4 \times IN_R$	$4 \times IN_L$
0	1	1	1	1	$4 \times (IN_R + IN_L)$	-	-

Absolute Maximum Ratings

VDD to GND . . . . . -0.3V to +6.5V
Input Voltages
InR, InL, SD, HD, HO, GSO, GS1. . . . . -0.3V to (VDD + 0.3V)
Output Voltages
SPK+, SPK-, HpL, HpR . . . . . -0.3V to (VDD + 0.3V)
Continuous Current (VDD, SPK_, Hp_, GND) 750mA
ESD Rating
Human Body Model . . . . . >2kV
Machine Model . . . . . >200kV
Charged Device Model . . . . . >1kV

Operating Conditions

Temperature Range . . . . . -40℃ to +85℃

Thermal Information

Thermal Resistance (Typical, Note 1, 2)	θ_{JA} (℃/W)	θ_{JC} (℃/W)
20 Ld 4x4 TQFN Package	45	6.5

Maximum Junction Temperature . . . . . +150℃
Maximum Storage Temperature Range . . . . . -65℃ to +150℃
Pb-free reflow profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTE:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.

Electrical Specifications - 5V Supply

Test Conditions: V_{DD} = +5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, SD = GSO = GS1 = V_{INL}, C_{REF} = 1µF, R_L is terminated between SPK+ and SPK- for BTL driver and between Hp_ and GND for SE drivers, Unless Otherwise Specified (Note 3).

PARAMETER	TEST CONDITIONS		TEMP (℃)	MIN (Notes 4, 5)	TYP	MAX (Notes 4, 5)	UNITS
GENERAL							
Power Supply Range, V_{DD}			Full	2.7	-	5.5	V
Quiescent Supply Current, I_{DD}	HO = V_{INL} or V_{INH}, HD = V_{INL}, R_L = None, Inputs AC coupled to GND (0.1µF)		25	-	4.6	12	mA
			Full	-	5.5	-	mA
Shutdown Supply Current, I_{SD}	SD = V_{INH}, HO = V_{INL} or V_{INH}, HD = V_{INL}, R_L = 8Ω (BTL) and R_L = 32Ω (SE), Inputs AC coupled to GND (0.1µF)		25	-	28	50	mA
			Full	-	31	-	mA
Input Resistance, R_{IN}	INS = 0V or V_{DD}		25	-	100	-	kΩ
Thermal Shutdown, T_{SD}	INS = MIX = 0V or V_{DD}		25	-	150	-	℃
Thermal Shutdown Hysteresis			25	-	10	-	℃
SD to Full Operation, $t_{SD(ON)}$			Full	-	1	-	ms
Gain Selection Range	Input referred minimum gain GS0 = GS1 = V_{INL}, R_L = 32Ω	SE Amplifiers HD = V_{INH} HO = V_{INL}	25	-0.4	0	0.6	dB
	Input referred maximum gain GS0 = GS1 = V_{INH}, R_L = 32Ω		25	11.4	12	12.6	dB
	Input referred minimum gain GS0 = GS1 = V_{INL}, R_L = 8Ω	BTL Amplifier HD = V_{INH} HO = V_{INH}	25	5.2	6	6.6	dB
	Input referred maximum gain GS0 = GS1 = V_{INH}, R_L = 8Ω		25	17.2	18	18.6	dB
BTL AMPLIFIER DRIVER, HD = V_{INH}, HO = V_{INH}, UNLESS OTHERWISE SPECIFIED							
Output Offset Voltage, V_{OS}	Measured between SPK+ and SPK-, Inputs AC coupled to GND (0.1µF)		25	-	38	-	mV
			Full	-	49	-	mV
Power Supply Rejection Ratio, PSRR	V_{RIPPLE} = 200MV_{P-P}, HD = V_{INL}, RL = 8Ω, Inputs AC coupled to GND (0.1µF)	F_{RIPPLE} = 217Hz	25	-	49	-	dB
		F_{RIPPLE} = 1kHz	25	-	47	-	dB
Output Power, P_{OUT}	R_L = 8Ω, THD+N = 1%, f = 1kHz		25	-	941	-	mW
	R_L = 8Ω, THD+N = 10%, f = 1kHz		25	-	1.23	-	W

Electrical Specifications - 5V Supply

Test Conditions: V_{DD} = +5V, GND = 0V, V_{INH} = 2.4V, V_{INL} = 0.8V, SD = GSO = GS1 = V_{INL}, C_{REF} = 1µF, R_L is terminated between SPK+ and SPK- for BTL driver and between Hp_ and GND for SE drivers, Unless Otherwise Specified (Note 3). **(Continued)**

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Notes 4, 5)	TYP	MAX (Notes 4, 5)	UNITS
Total Harmonic Distortion + Noise, THD+N	R_L = 8Ω, P_{OUT} = 800mW, f = 1kHz		25	-	0.4	-	%
	R_L = 8Ω, P_{OUT} = 800mW, f = 20Hz to 20kHz		25	-	0.7	-	%
Max Output Voltage Swing, V_{OUT}	R_L = 8Ω, V_{SIGNAL} = $5V_{P-P}$, f = 1kHz		25	7.2	7.7	-	V_{P-P}
Signal to Noise Ratio, SNR	R_L = 8Ω, P_{OUT} = 900mW, f = 1kHz		25	-	85	-	dB
Output Noise, N_{OUT}	A - Weight filter, BW = 22Hz to 22kHz		25	-	140	-	mV_{RMS}
Crosstalk R_{CH} to L_{CH}, L_{CH} to R_{CH}	R_L = 8Ω, P_{OUT} = 800mW, f = 1kHz, Signal coupled from the input of active amplifier to the output of an adjacent amplifier with its input AC coupled to GND.		25	-	80	-	dB
Off-Isolation	SD = V_{DD}, P_{OUT} = 800mW, f = 10kHz, Signal coupled from input to output of a disabled amplifier.		25	-	130	-	dB
SINGLE ENDED AMPLIFIER DRIVERS, HD = V_{INH}, HO = V_{INL}, UNLESS OTHERWISE SPECIFIED							
Power Supply Rejection Ratio, PSRR	V_{RIPPLE} = $200MV_{P-P}$, HD = 0V, R_L = 32Ω, Input AC coupled to GND (0.1µF)	F_{RIPPLE} = 217Hz	25	-	48	-	dB
		F_{RIPPLE} = 1kHz	25	-	47	-	dB
Output Power, P_{OUT}	R_L = 16Ω, THD+N = 1%, f = 1kHz		25	-	170	-	mW
	R_L = 32Ω, THD+N = 1%, f = 1kHz		25	-	94	-	mW
	R_L = 16Ω, THD+N = 10%, f = 1kHz		25	-	215	-	mW
	R_L = 32Ω, THD+N = 10%, f = 1kHz		25	-	116	-	mW
Total Harmonic Distortion + Noise, THD+N	R_L = 32Ω, P_{OUT} = 15mW, f = 1kHz		25	-	0.07	-	%
	R_L = 32Ω, P_{OUT} = 15mW, f = 20Hz to 20kHz		25	-	0.09	-	%
	R_L = 32Ω, P_{OUT} = 50mW, f = 1kHz		25	-	0.3	-	%
	R_L = 32Ω, P_{OUT} = 50mW, f = 20Hz to 20kHz		25	-	0.4	-	%
Max Output Voltage Swing, V_{OUT}	R_L = 32Ω, V_{SIGNAL} = $5V_{P-P}$, f = 1kHz		25	3.6	4.7	-	V_{P-P}
Crosstalk R_{CH} to L_{CH}, L_{CH} to R_{CH}	R_L = 32Ω, P_{OUT} = 15mW, f = 1kHz		25	-	75	-	dB
Off-Isolation	SD = V_{DD}, R_L = 32W, P_{OUT} = 15mW, f = 10kHz		25	-	120	-	dB
Signal to Noise Ratio, SNR	R_L = 32Ω, P_{OUT} = 50mW, f = 1kHz		25	-	83	-	dB
Channel Gain Matching R_{CH} to L_{CH}	R_L = 32Ω, VINR = VINL = $1.3V_{RMS}$ (Connect to the same source)		25	-	±0.2	-	dB
Channel Phase Matching R_{CH} to L_{CH}	R_L = 32Ω, VINR = VINL = $1.3V_{RMS}$ (Connect to the same source)		25	-	1.3	-	°
LOGIC INPUT							
Input Leakage Current, I_{SD}, I_{HD}, I_{GSx}, I_{HO}	V_{DD} = 5V, SD = 0V, INS = 0V, GSx = 0V, HD = 0V, HO = 0V		25	-3	1.9	3	µA
			Full	-	1.9	-	µA
Input Leakage Current, I_{SD}, I_{GSx}, I_{HD}, I_{HO}	V_{DD} = 5V, SD = V_{DD}, INS = V_{DD}, GSx = V_{DD}, HD = V_{DD}, HO = V_{DD}		25	-1	0.02	1	µA
			Full	-	0.02	-	µA
V_{INH}			Full	2.4	-	-	V
V_{INL}			Full	-	-	0.8	V

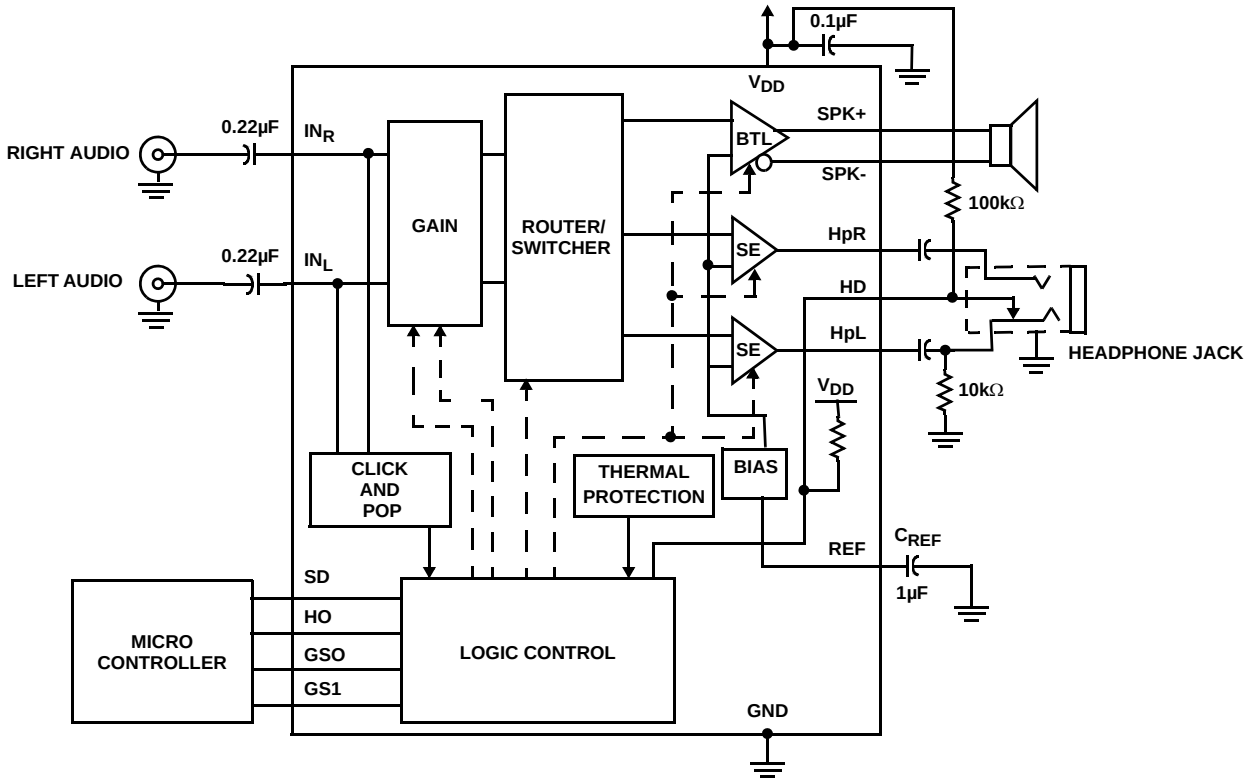
Electrical Specifications - 3.6V Supply Test Conditions: V_{DD} = +3.6V, GND = 0V, V_{INH} = 1.4V. V_{INL} = 0.4V, SD = GSO = GS1 = V_{INL}, C_{REF} = 1µF, R_L is terminated between SPK+ and SPK- for BTL driver and between Hp_ and GND for SE drivers, Unless Otherwise Specified (Note 3)

PARAMETER	TEST CONDITIONS		TEMP (°C)	MIN (Notes 4, 5)	TYP	MAX (Notes 4, 5)	UNITS
GENERAL							
Quiescent Supply Current, I_{DD}	HO = V_{INL} or V_{INH}, HD = V_{INL}, RL = None, Input AC coupled to GND (0.1µF)		25	-	2.7	12	mA
			Full	-	3	-	mA
Shutdown Supply Current, I_{SD}	SD = V_{INH}, HO = V_{INL} or V_{INH}, HD = V_{INL}, R_L = 8Ω (BTL) and R_L = 32Ω (SE), Input AC coupled to GND (0.1µF)		25	-	13	50	mA
			Full	-	15	-	mA
BTL AMPLIFIER DRIVER, HD = V_{INH}, HO = V_{INH}, UNLESS OTHERWISE SPECIFIED							
Output Offset Voltage, V_{OS}	Measured between SPK+ and SPK-, Input AC coupled to GND (0.1µF)		25	-	25	-	mV
			Full	-	40	-	mV
Power Supply Rejection Ratio, PSRR	V_{RIPPLE} = 200mV_{P-P} HD = 0V, R_L = 8Ω, Input AC coupled to GND (0.1µF)	F_{RIPPLE} = 217Hz	25	-	49	-	dB
		F_{RIPPLE} = 1kHz	25	-	47	-	dB
Output Power, P_{OUT}	R_L = 8Ω, THD+N = 1%, f = 1kHz		25	-	310	-	mW
	R_L = 8Ω, THD+N =10%, f = 1kHz		25	-	528	-	mW
Total Harmonic Distortion + Noise, THD+N	R_L = 8Ω, P_{OUT} = 200mW, f = 1kHz		25	-	0.4	-	%
	R_L = 8Ω, P_{OUT} = 200mW, f = 20Hz to 20kHz		25	-	0.4	-	%
Max Output Voltage Swing, V_{OUT}	R_L = 8Ω, V_{SIGNAL} = 3.6V_{P-P}, f = 1kHz		25	-	5.8	-	V_{P-P}
SINGLE ENDED AMPLIFIER DRIVERS, HD = V_{INH}, HO = V_{INL}, UNLESS OTHERWISE SPECIFIED							
Power Supply Rejection Ratio, PSRR	V_{RIPPLE} = 200MV_{P-P}, HD = 0V, R_L = 32Ω, Input AC coupled to GND (0.1µF)	F_{RIPPLE} = 217Hz	25	-	48	-	dB
		F_{RIPPLE} = 1kHz	25	-	47	-	dB
Output Power, P_{OUT}	R_L = 16Ω, THD+N =1%, f = 1kHz		25	-	80	-	mW
	R_L = 32Ω, THD+N =1%, f = 1kHz		25	-	47	-	mW
	R_L = 16Ω, THD+N = 10%, f = 1kHz		25	-	107	-	mW
	R_L = 32Ω, THD+N = 10%, f =1kHz		25	-	58	-	mW
Total Harmonic Distortion + Noise, THD+N	R_L = 32Ω, P_{OUT} = 15mW, f = 1kHz		25	-	0.15	-	%
	R_L = 32Ω, P_{OUT} = 15mW, f = 20Hz to 20kHz		25	-	0.15	-	%
Max Output Voltage Swing, V_{OUT}	R_L = 32Ω, V_{SIGNAL} = 3.6V_{P-P}, f = 1kHz		25	-	3.2	-	V_{P-P}
LOGIC INPUT							
Input Leakage Current, I_{SD}, I_{GSx}, I_{HD}, I_{HO}	V_{DD} = 3.6V, SD = 0V, GSx = 0V, HD = 0V , HO = 0V,		25	-	1.9	-	µA
			Full	-	1.9	-	µA
Input Leakage Current, I_{SD}, I_{GSx}, I_{HD}, I_{HO}	V_{DD} = 3.6V, SD = V_{DD}, GSx = V_{DD}, HD = V_{DD}, HO = V_{DD}		25	-	0.02	-	µA
			Full	-	0.02	-	µA
V_{INH}			Full	1.4	-	-	V
V_{INL}			Full	-	-	0.4	V

NOTES:

3. V_{IN} = input voltage to perform proper function.
4. The algebraic convention, whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
5. Parts are 100% tested at +25°C. Over-temperature limits established by characterization and are not production tested

ISL54004 Typical Application Circuit and Block Diagram



Detailed Description

The Intersil ISL54004 device is an integrated audio power amplifier system designed to provide quality audio, while requiring minimal external components. Low 0.4% THD+N ensures clean, low distortion amplification of the audio signals. It is designed to operate from a single +2.7V to +5V power supply. It is offered in a 20 Ld 4x4 TQFN package. Targeted applications include battery powered equipment such as cell-phones, MP3 players, and games/toys.

The ISL54004 part contains one class AB BTL type power amplifier for driving an 8Ω mono speaker and two class AB single-ended (SE) type amplifiers for driving 16Ω or 32Ω headphones.

The BTL when using a 5V supply is capable of delivering 800mW (typ) with 0.4% THD+N and 941mW (typ) with 1% THD+N of continuous average power into a stereo 8Ω BTL speaker load. When the speaker load is connected across the positive and negative terminals of the BTL driver the voltage is doubled across the load and the power is quadrupled.

Each SE amplifier when using a 5V supply is capable of delivering 15mW (typ) with 0.07% THD+N and 50mW (typ) with 0.3% THD+N of continuous average power into a 32Ω headphone speaker.

When in Mono Mode (BTL driver active) the part automatically mixes the left and right audio inputs and sends the combined signal to the BTL driver. In Headphone Mode the right channel input is sent to the right headphone speaker and the left channel is sent to the left headphone speaker.

The ISL54004 features headphone sense input circuitry that detects when a headphone jack has been inserted and automatically switches the audio inputs from the mono BTL output driver to the headphone drivers. It also has a logic control pin (HO) that can override the sense input circuitry.

The ISL54004 has a four-level programmable gain stage to boost the audio signal. The part requires no external gain setting resistors. When GSO = GS1 = Low a driver will have a gain of 1V/V (0dB). When GSO = High, GS1 = Low a driver will have a gain of 1.2V/V (1.5dB). When GSO = Low, GS1 = High a driver will have a gain of 2V/V (6dB). When GSO = High, GS1 = High a driver will have a gain of 4V/V (12dB). When the speaker is connected across the SPK+ terminal and SPK- terminal of the mono BTL driver you get an additional gain of 2V/V (6dB) due to the BTL configuration. The overall gain will be 2 times the values discussed above. For example with GS1 = GS0 = High the overall gain will be 2 x 4 = 8V/V (18dB).

The part features low power shutdown, thermal overload protection and click and pop suppression. The click and pop circuitry prevents click and pops at the speakers when transitioning in and out of shutdown.

The “Typical Application Circuit and Block Diagram” for this device is provided on page 6. The “Truth Table” for the device is provided on page 2.

DC Bias Voltage

The ISL54004 has internal DC bias circuitry which DC offsets the incoming audio signal at $V_{DD}/2$. When using a 5V supply, the DC offset will be 2.5V. When using a 3.6V supply the DC offset will be 1.8V.

Since the signal gets biased internally at $V_{DD}/2$ the audio signals need to be AC coupled to the inputs of the device. The value of the AC coupling capacitor depends on the low frequency range required for the application. A capacitor of 0.22µF will pass a signal as low as 7.2Hz. The formula required to calculate the capacitor value is shown in Equation 1:

$$C \geq \frac{1}{[(6.28)(f)(100k)]} \quad \text{(EQ. 1)}$$

The 100kΩ is the impedance looking into the input of the ISL54004 device.

BTL Speaker Amplifier

The ISL54004 contains one bridge-tied load (BTL) amplifier designed to drive an 8Ω speaker load differentially. The output to the BTL amplifier are SPK+ and SPK-. The speaker load gets connected across these terminals.

A single BTL driver consists of an inverting and non-inverting power op amps. The AC signal out of each op amp are equal in magnitude but 180° out-of-phase, so the AC signal at SPK+ and SPK- have the same amplitude but are 180° out-of-phase.

Driving the load differentially using a BTL configuration doubles the output voltage across the speaker load and quadruples the power to the load. In effect you get a gain of two due to this configuration at the load as compared to driving the load with a single-ended amplifier with its load connected between a single amplifier’s output and GND.

The outputs of the BTL are biased at $V_{DD}/2$. When the load gets connected across the + and - terminal of the BTL the mid supply DC bias voltage at each output gets cancelled out eliminating the need for large bulky output coupling capacitors.

Headphone (Single-Ended) Amplifiers

The ISL54004 contains two single-ended (SE) headphone amplifiers for driving the left and right channels of a 32Ω or 16Ω headphone speakers.

One SE amplifier drives the right speaker of the headphone and other SE amplifier drives the left speaker of the headphone. The speaker load gets connected between the output of the amplifier and ground.

The audio signal at the output of each SE driver is biased at $V_{DD}/2$ and unlike the BTL driver that cancels this offset due to its differential connection, a capacitor is required at the output of each SE drivers to remove this DC voltage from the headphone load.

This coupling capacitor along with the resistance of the speaker load creates a high pass filter that sets the amplifier’s lower bandpass frequency limit. The value of this AC coupling capacitor depends on the low frequency range required for the application. The formula required to calculate the capacitor value is shown in Equation 2:

$$C \geq \frac{1}{[(6.28)(f)(Rspeaker)]} \quad \text{(EQ. 2)}$$

For an application driving a 32Ω headphone with a lower frequency requirement of 150Hz the required capacitor value is shown in Equation 3:

$$C \geq \frac{1}{[(6.28)(150)(32)]} = 33\mu F \quad \text{(EQ. 3)}$$

Use the closest standard value.

Headphone Sense Function

With a logic “1” at the HP control pin while the HO control pin is low will activate the headphone drivers and disable the BTL driver.

The “ISL54004 Typical Application Circuit and Block Diagram” on page 6 shows the implementation of the headphone control function using a common headphone jack.

The HP pin gets connected to the mechanical wiper blade of the headphone jack. Two external resistors are required for proper operation. A 100kΩ pull-up resistor from the HP pin to VDD and a 10kΩ pull-down resistor from the jack’s audio signal pin to GND of the jack signal pin to which the wiper is connected. See “ISL54004 Typical Application Circuit and Block Diagram” on page 6.

When no headphone plug is inserted into the jack the voltage at the HP pin gets set at a low voltage level due to the 10kΩ resistor and 100kΩ resistor divider network connection to V_{DD}.

When a headphone is inserted into the jack the 10kΩ resistor gets disconnected from the HP control pin and the HP pin gets pulled up to V_{DD}. Since the HP pin is now high the headphone drivers are activated.

A microprocessor or a switch can be used to drive the HP pin rather than using the headphone jack contact pin.

Note: With a logic “1” at the HO pin the BTL driver remains active regardless of the voltage level at the HD pin. This allows a headphone to be plugged into the headphone jack without activating the HP drivers. Music will continue to play through the internal 8Ω speaker rather than the headphones.

Low Power Shutdown

With a logic “1” at the SD control pin the device enters the low power shutdown state. When in shutdown the BTL and headphone amplifiers go into an high impedance state and I_{DD} supply current is reduced to 26µA (typ).

In shutdown mode before the amplifiers enter the high impedance/low current drive state, the bias voltage of $V_{DD}/2$ remains connected at the output of the amplifiers through a 100kΩ resistor.

This resistor is not present during active operation of the drivers but gets switched in when the SD pin goes high. It gets removed when the SD pin goes low.

Leaving the DC bias voltage connected through a 100kΩ resistor while going into and out of shutdown reduces the transient at the speakers to a small level preventing clicking or popping in the speakers.

Note: When the SD pin is High it overrides all other logic pins.

QFN Die Attach Paddle Considerations

The QFN package features an exposed thermal pad on its underside. This pad lowers the package’s thermal resistance by providing a direct heat conduction path from the die to the PCB. Connect the exposed thermal pad to GND by using a large copper pad and multiple vias to the GND plane. The vias should be plugged and tented with plating and solder mask to ensure good thermal conductivity.

Best thermal performance is achieved with the largest practical copper ground plane area.

PCB Layout Considerations and Power Supply Bypassing

To maintain the highest load dissipation and widest output voltage swing the power supply PCB traces and the traces that connect the output of the drivers to the speaker loads should be made as wide as possible to minimize losses due to parasitic trace resistance.

Proper supply bypassing is necessary for high power supply rejection and low noise performance. A filter network consisting of a 10µF capacitor in parallel with a 0.1µF capacitor is recommended at the voltage regulator that is providing the power to the ISL54004 IC.

Local bypass capacitors of 0.1µF should be put at each V_{DD} pin of the ISL54004 device. They should be located as close as possible to the pin, keeping the length of leads and traces as short as possible.

A 1µF capacitor from the REF pin (pin 10) to GND is needed for optimum PSRR and internal bias voltage stability.

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified

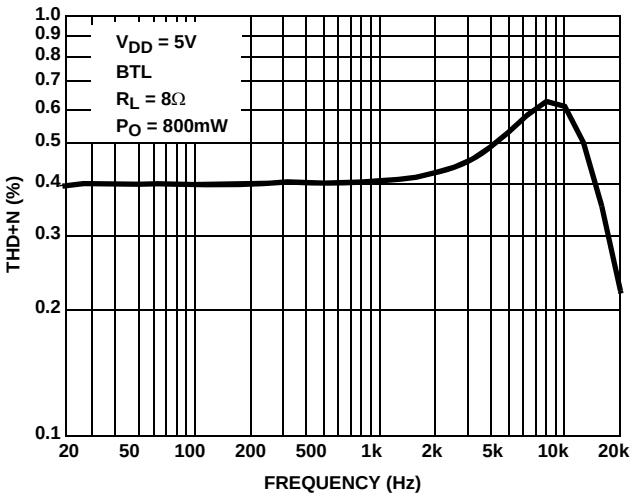


FIGURE 1. THD+N vs FREQUENCY

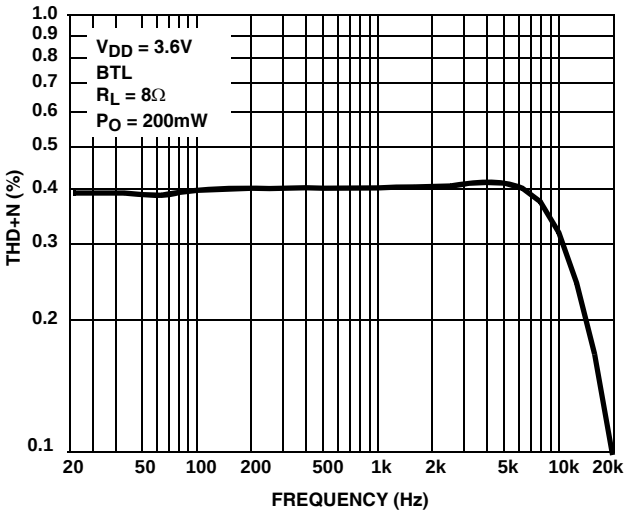


FIGURE 2. THD+N vs FREQUENCY

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

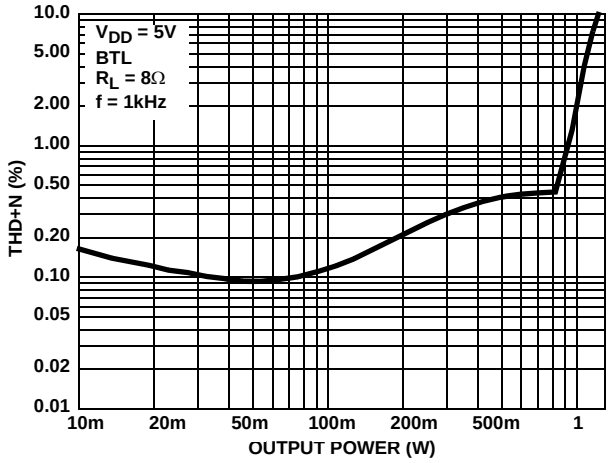


FIGURE 3. THD+N vs OUTPUT POWER

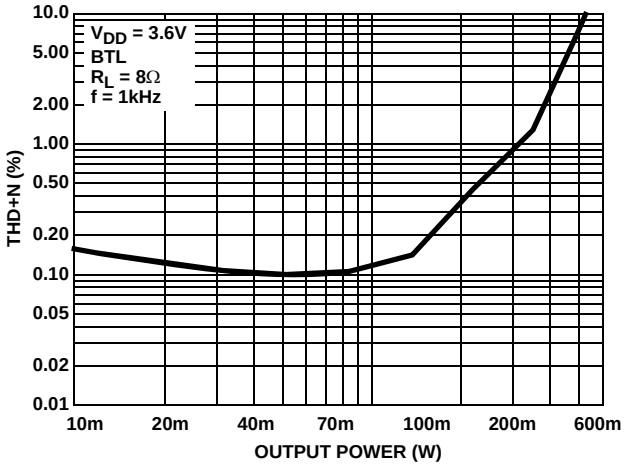


FIGURE 4. THD+N vs OUTPUT POWER

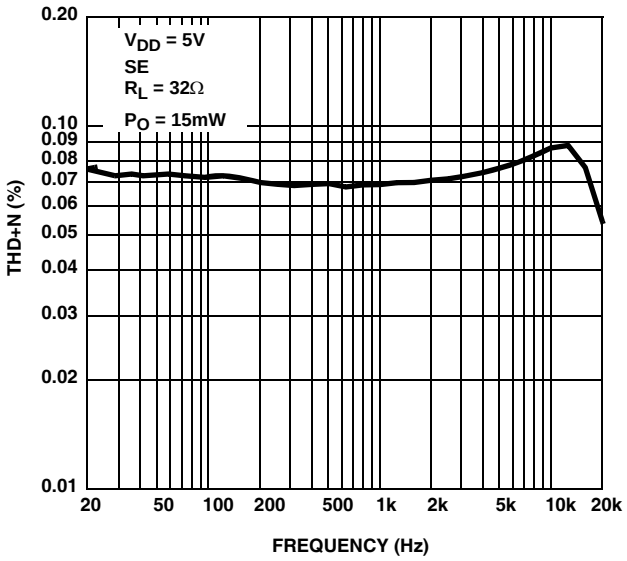


FIGURE 5. THD+N vs FREQUENCY

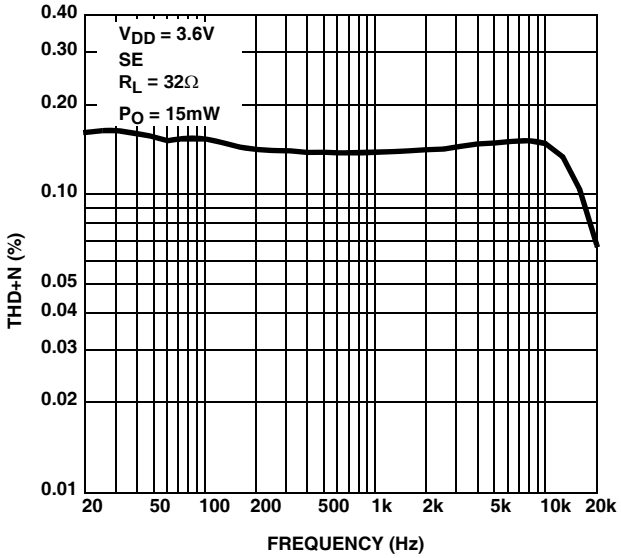


FIGURE 6. THD+N vs FREQUENCY

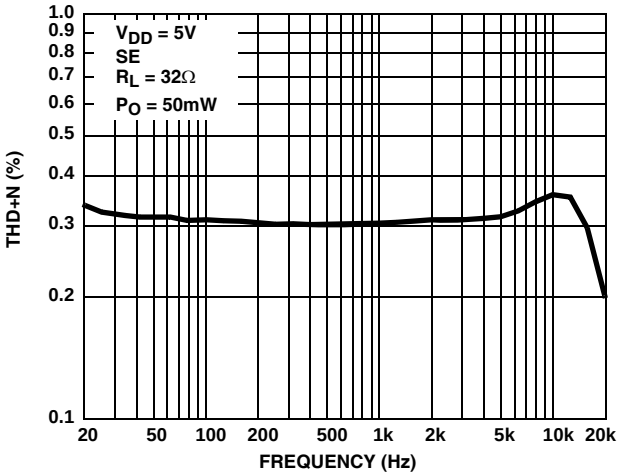


FIGURE 7. THD+N vs FREQUENCY

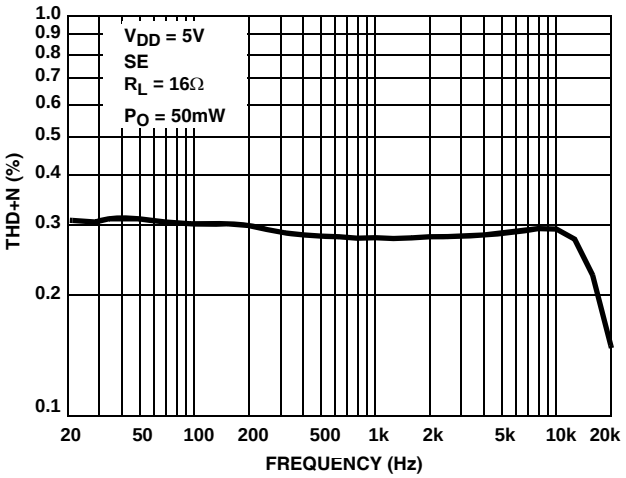


FIGURE 8. THD+N vs FREQUENCY

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

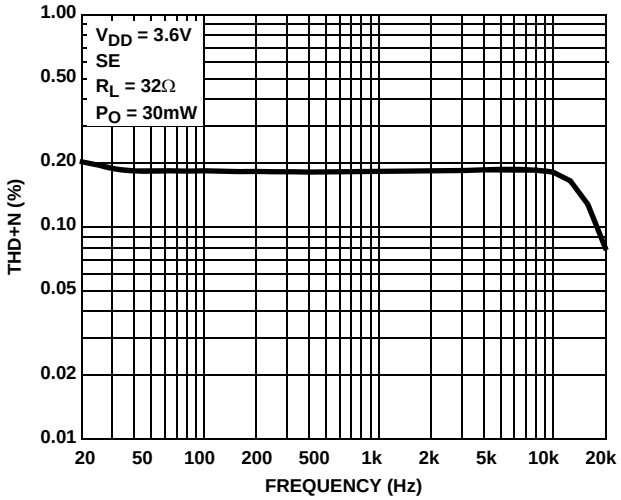


FIGURE 9. THD+N vs FREQUENCY

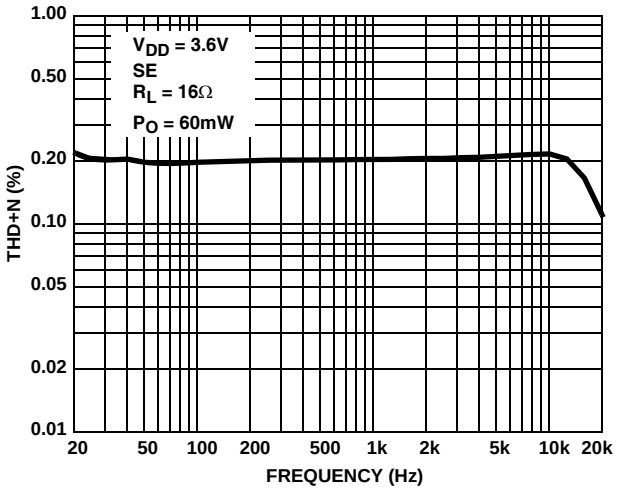


FIGURE 10. THD+N vs FREQUENCY

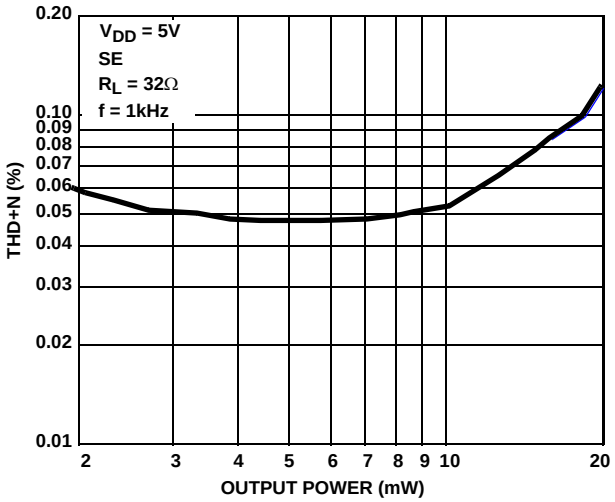


FIGURE 11. THD+N vs OUTPUT POWER

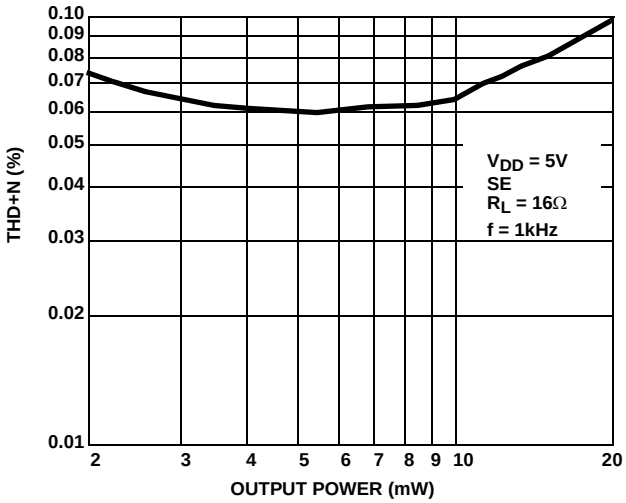


FIGURE 12. THD+N vs OUTPUT POWER

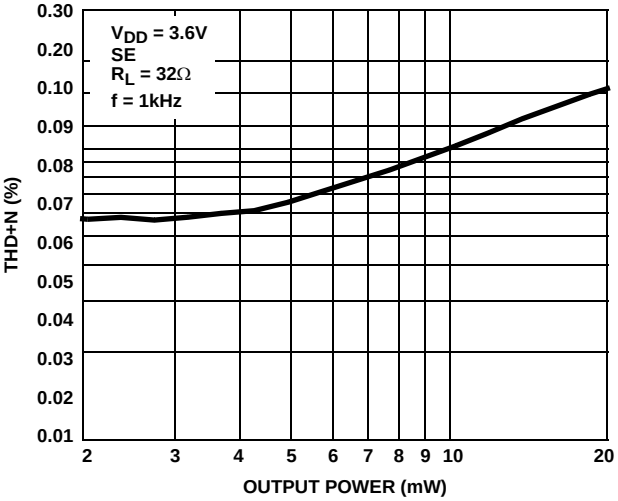


FIGURE 13. THD+N vs OUTPUT POWER

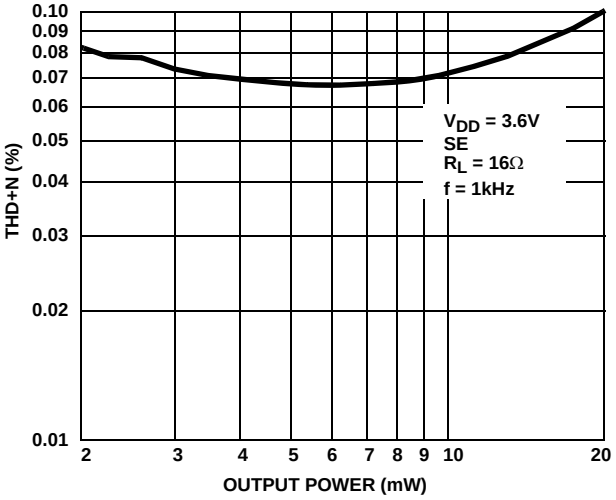


FIGURE 14. THD+N vs OUTPUT POWER

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

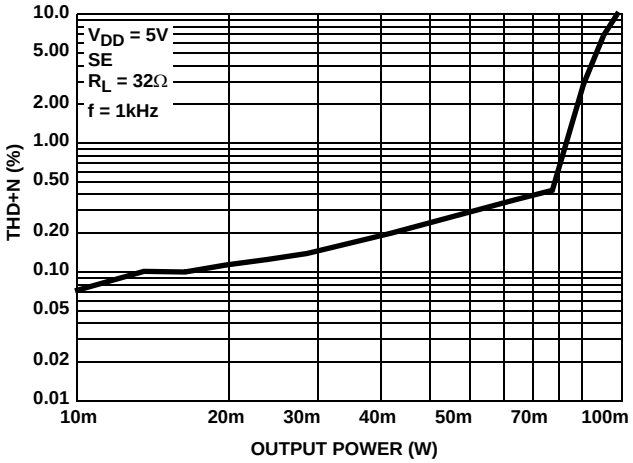


FIGURE 15. THD+N vs OUTPUT POWER

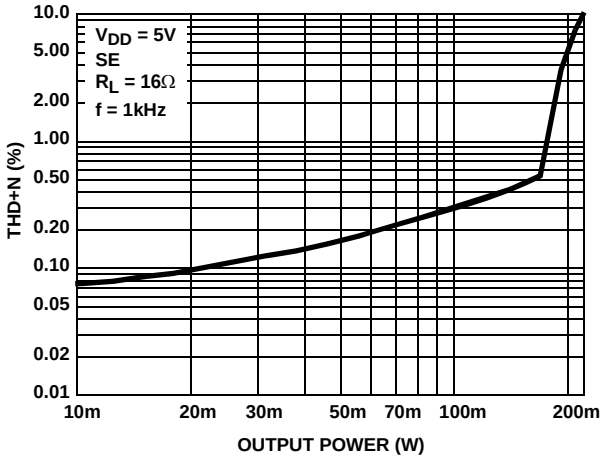


FIGURE 16. THD+N vs OUTPUT POWER

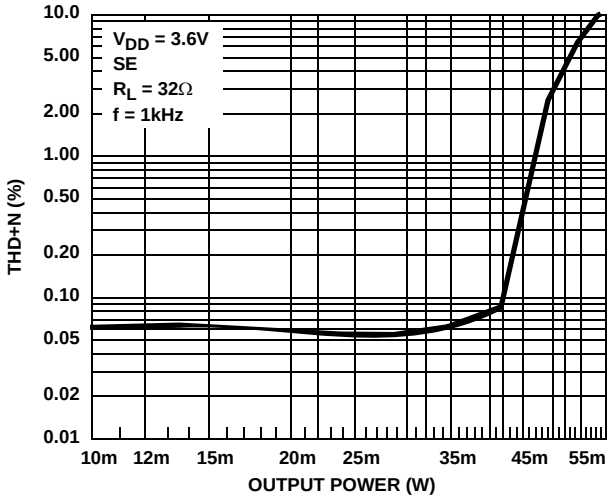


FIGURE 17. THD+N vs OUTPUT POWER

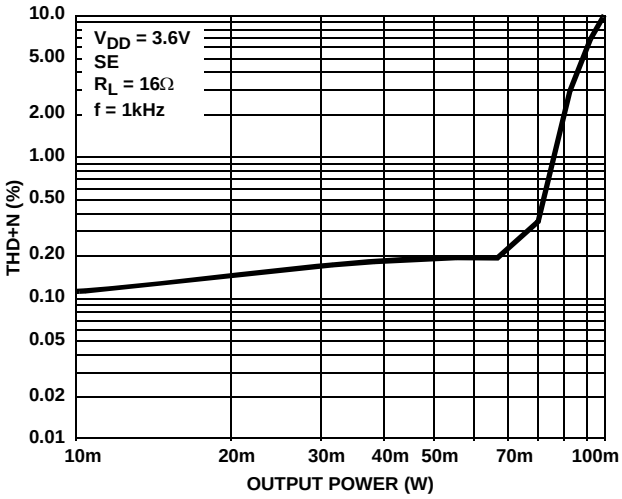


FIGURE 18. THD+N vs OUTPUT POWER

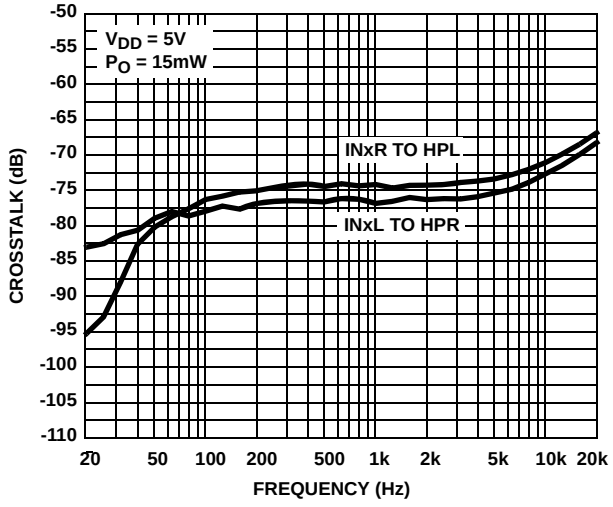


FIGURE 19. CROSSTALK vs FREQUENCY

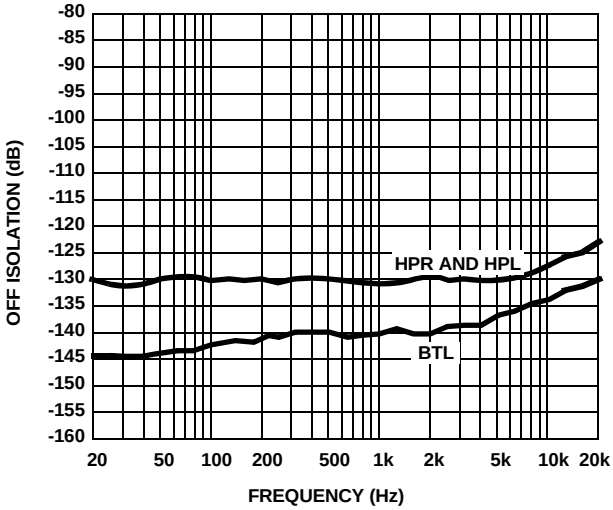


FIGURE 20. OFF ISOLATION vs FREQUENCY

Typical Performance Curves T_A = +25°C, Unless Otherwise Specified **(Continued)**

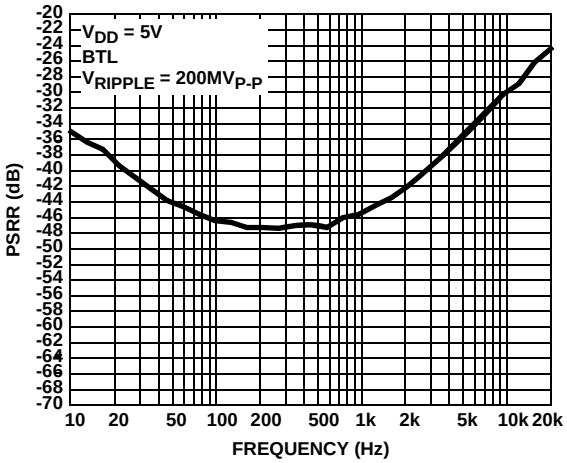


FIGURE 21. PSRR vs FREQUENCY

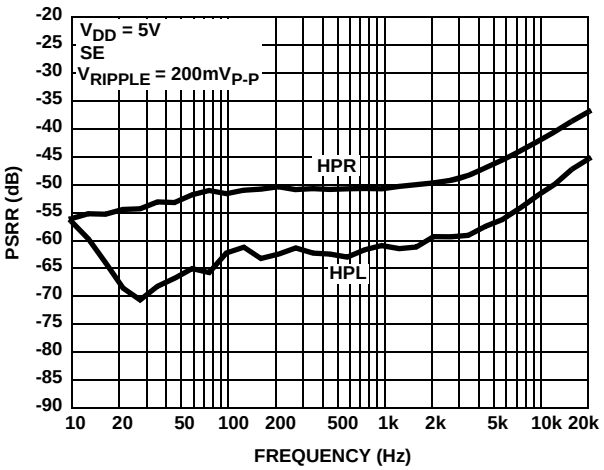


FIGURE 22. PSRR vs FREQUENCY

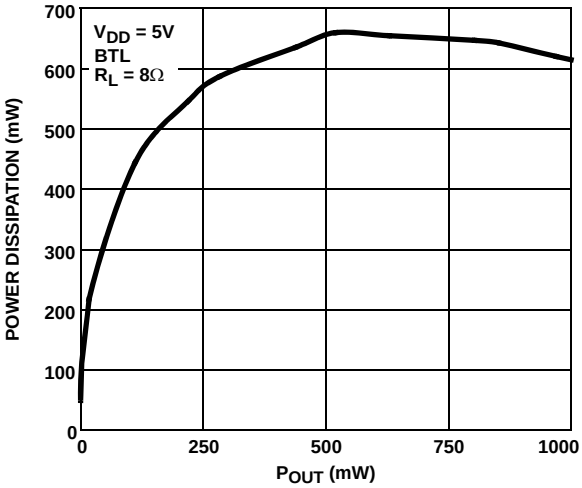


FIGURE 23. POWER DISSIPATION vs OUTPUT POWER

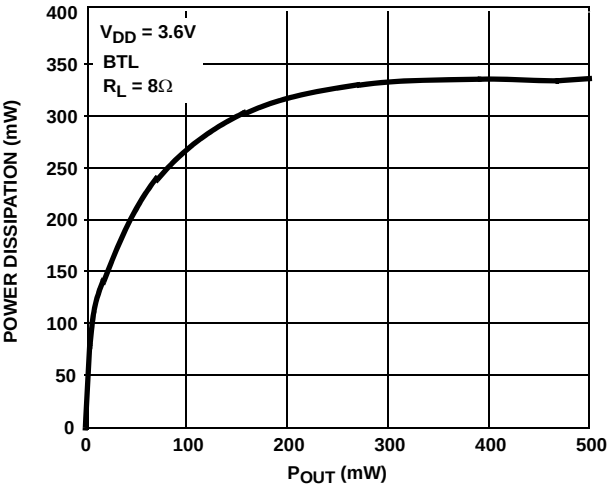


FIGURE 24. POWER DISSIPATION vs OUTPUT POWER

Die Characteristics

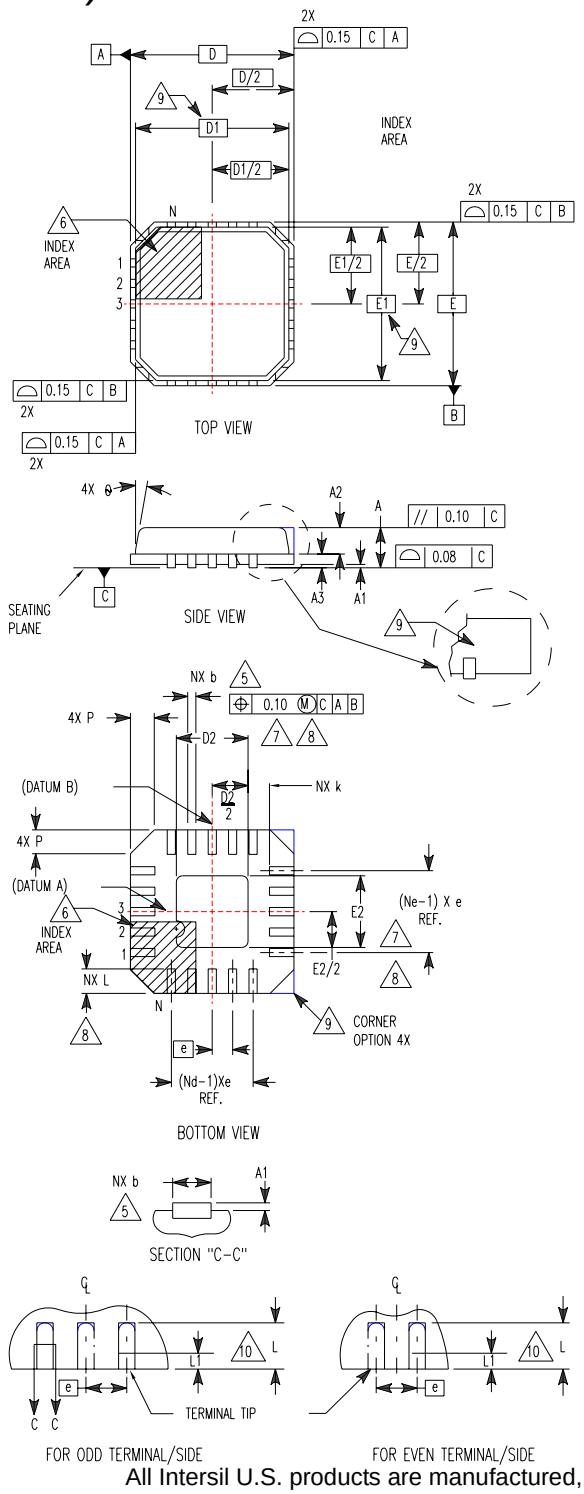
SUBSTRATE POTENTIAL (POWERED UP):

GND

PROCESS:

Submicron CMOS

Thin Quad Flat No-Lead Plastic Package (TQFN)
Thin Micro Lead FramePlastic Package (TMLFP)



L20.4x4A

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220WGGD-1 ISSUE I)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.70	0.75	0.80	-
A1	-	0.02	0.05	-
A2	-	0.55	0.80	9
A3		0.20 REF		9
b	0.18	0.25	0.30	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.50 BSC		-
k	0.20	-	-	-
L	0.35	0.60	0.75	8
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 0 11/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.