Data Sheet | June 28, 2012 | FN2855.5

Precision Quad Comparators

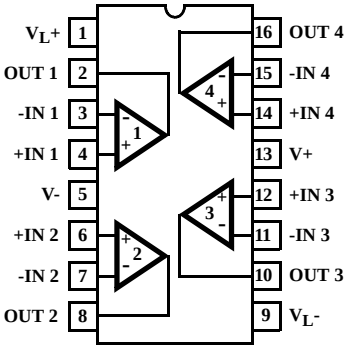
The HA-4900 series are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5V supply (digital systems) or from dual supplies (analog networks) up to ±15V. The HA-4900 series contains a unique current driven output stage which can be connected to logic system supplies (V_{LOGIC}^+ and V_{LOGIC}^-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900 series input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

These comparators' combination of features make them ideal components for signal detection and processing in data acquisition systems, test equipment and microprocessor/analog signal interface networks.

For military grade product, refer to the HA-4902/883 data sheet.

Pinout

HA-4900, HA-4902 (CERDIP)
HA-4905 (PDIP, CERDIP, SOIC)
TOP VIEW



Features

- Fast Response Time 130ns
- Low Offset Voltage 2.0mV
- Low Offset Current 10nA
- Single or Dual Voltage Supply Operation
- Selectable Ouput Logic Levels
- Active Pull-Up/Pull-Down OutputCircuit. No External Resistors Required
- Pb-Free Plus Anneal Available (RoHS Compliant)

Applications

- Threshold Detector
- Zero Crossing Detector
- Window Detector
- Analog Interfaces for Microprocessors
- High Stability Oscillators
- Logic System Interfaces

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (^{0}C)	PACKAGE	PKG. DWG. #
HA1-4900-2	HA1-4900-2	-55 to 125	16 Ld CERDIP	F16.3
HA1-4902-2	HA1-4902-2	-55 to 125	16 Ld CERDIP	F16.3
HA1-4905-5	HA1-4905-5	0 to 75	16 Ld CERDIP	F16.3
HA3-4905-5	HA3-4905-5	0 to 75	16 Ld PDIP	E16.3
HA9P4905-5	HA9P4905-5	0 to 75	16 Ld SOIC	M16.3
HA9P4905-5Z (See Note)	HA9P4905-5Z	0 to 75	16 Ld SOIC (Pb-free)	M16.3

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage (Between V+ and V- Terminals) 33V
Differential Input Voltage 15V
Voltage Between V_{LOGIC}^+ and V_{LOGIC}^- 18V
Output Current 50mA
Power Dissipation (Notes 1, 2)

Operating Conditions

Temperature Range
HA-4900-2, HA-4902-2 . . . . . -55^oC to 125^oC
HA-4905-5 . . . . . 0^oC to 75^oC

Thermal Information

Thermal Resistance (Typical, Note 3)	θ_{JA} ($^oC/W$)	θ_{JC} ($^oC/W$)
CERDIP Package	85	25
PDIP Package	90	N/A
SOIC Package	100	N/A

Maximum Junction Temperature (Ceramic Package) . . . . . 175^oC
Maximum Junction Temperature (Plastic Package) . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(SOIC - Lead Tips Only)

Die Characteristics

Back Side Potential . . . . . V-
Number of Transistors 137
Die Size . . . . . 95 mils x 105 mils

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. Maximum power dissipation, including output load, must be designed to maintain the junction temperature below 175^oC for ceramic packages, and below 150^oC for plastic packages.
2. Total Power Dissipation (T.P.D.) is the sum of individual dissipation contributions of V+, V- and V_{LOGIC} shown in curves of Power Dissipation vs Supply Voltages (see Performance Curves). The calculated T.P.D. is then located on the graph of Maximum Allowable Package Dissipation vs Ambient Temperature to determine ambient temperature operating limits imposed by the calculated T.P.D. (See Performance Curves). For instance, the combination of +15V, -15V, +5V, 0V (V+, V-, V_{LOGIC}^+, V_{LOGIC}^-) gives a T.P.D. of 350mW, the combination +15V, -15V, +15V, 0V gives a T.P.D. of 450mW.
3. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

$V_{SUPPLY} = \pm15V$, $V_{LOGIC}^+ = 5V$, $V_{LOGIC}^- = GND$

PARAMETER	TEMP (^oC)	HA-4900-2 -55^oC to 125^oC			HA-4902-2 -55^oC to 125^oC			HA-4905-5 0^oC to 75^oC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS											
Offset Voltage (Note 4)	25	-	2	3	-	2	5	-	4	7.5	mV
	Full	-	-	4	-	-	8	-	-	10	mV
Offset Current	25	-	10	25	-	10	35	-	25	50	nA
	Full	-	-	35	-	-	45	-	-	70	nA
Bias Current (Note 5)	25	-	50	75	-	50	150	-	100	150	nA
	Full	-	-	150	-	-	200	-	-	300	nA
Input Sensitivity (Note 6)	25	-	-	V_{IO} + 0.3	-	-	V_{IO} + 0.5	-	-	V_{IO} + 0.5	mV
	Full	-	-	V_{IO} + 0.4	-	-	V_{IO} + 0.6	-	-	V_{IO} + 0.7	mV
Common Mode Range	Full	V-	-	(V+) - 2.4	V-	-	(V+) - 2.6	V-	-	(V+) - 2.4	V
Differential Input Resistance	25	-	250	-	-	250	-	-	250	-	MΩ
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain	25	-	400	-	-	400	-	-	400	-	kV/V
Response Time ($t_{PD}(0)$) (Note 7)	25	-	130	200	-	130	200	-	130	200	ns
Response Time ($t_{PD}(1)$) (Note 7)	25	-	180	215	-	180	215	-	180	215	ns
OUTPUT CHARACTERISTICS											
Output Voltage Level											

Electrical Specifications V_{SUPPLY} = ±15V, V_{LOGIC}^+ = 5V, V_{LOGIC}^- = GND **(Continued)**

PARAMETER	TEMP (^oC)	HA-4900-2 -55^{o}C to 125^{o}C			HA-4902-2 -55^{o}C to 125^{o}C			HA-4905-5 0^{o}C to 75^{o}C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Logic "Low State" (V_{OL}) (Note 8)	Full	-	0.2	0.4	-	0.2	0.4	-	0.2	0.4	V
Logic "High State" (V_{OH}) (Note 8)	Full	3.5	4.2	-	3.5	4.2	-	3.5	4.2	-	V
Output Current											
I_{SINK}	Full	3.0	-	-	3.0	-	-	3.0	-	-	mA
I_{SOURCE}	Full	3.0	-	-	3.0	-	-	3.0	-	-	mA
POWER SUPPLY CHARACTERISTICS											
Supply Current, I_{PS} (+)	25	-	6.5	20	-	6.5	20	-	7	20	mA
Supply Current, I_{PS} (-)	25	-	4	8	-	4	8	-	5	8	mA
Supply Current, I_{PS} (Logic)	25	-	3.5	4	-	3.5	4	-	3.5	4	mA
Supply Voltage Range											
V_{LOGIC}^+ (Note 2)	Full	0	-	+15.0	0	-	+15.0	0	-	+15.0	V
V_{LOGIC}^- (Note 2)	Full	-15.0	-	0	-15.0	-	0	-15.0	-	0	V

NOTES:

4. Minimum differential input voltage required to ensure a defined output state.
5. Input bias currents are essentially constant with differential input voltages up to ±9V. With differential input voltages from ±9V to ±15V, bias current on the more negative input can rise to approximately 500µA. This will also cause higher supply currents.
6. V_{CM} = 0V. Input sensitivity is the worst case minimum differential input voltage required to guarantee a given output logic state. This parameter includes the effects of offset voltage and voltage gain.
7. For $t_{PD}(1)$; 100mV input step, -10mV overdrive. For $t_{PD}(0)$; -100mV input step, 10mV overdrive. Frequency ≈ 100Hz; Duty Cycle ≈ 50%; Inverting input driven. See Figure 1 for Test Circuit. All unused inverting inputs tied to +5V.
8. For V_{OH} and V_{OL}: I_{SINK} = I_{SOURCE} = 3.0mA. For other values of V_{LOGIC}; V_{OH} (Min) = V_{LOGIC} + -1.5V.

Test Circuit and Waveform

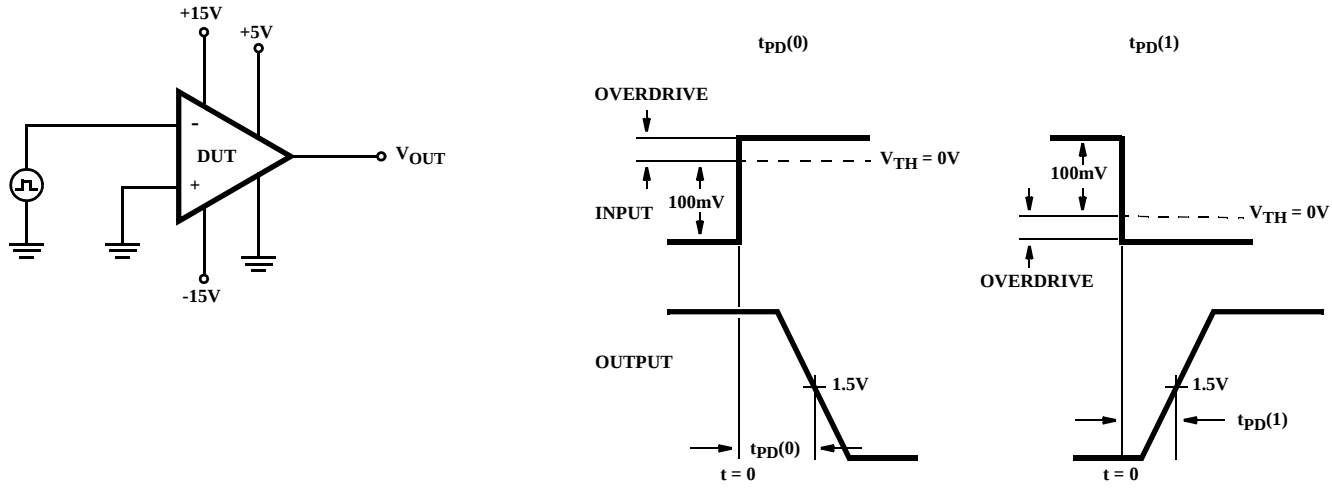
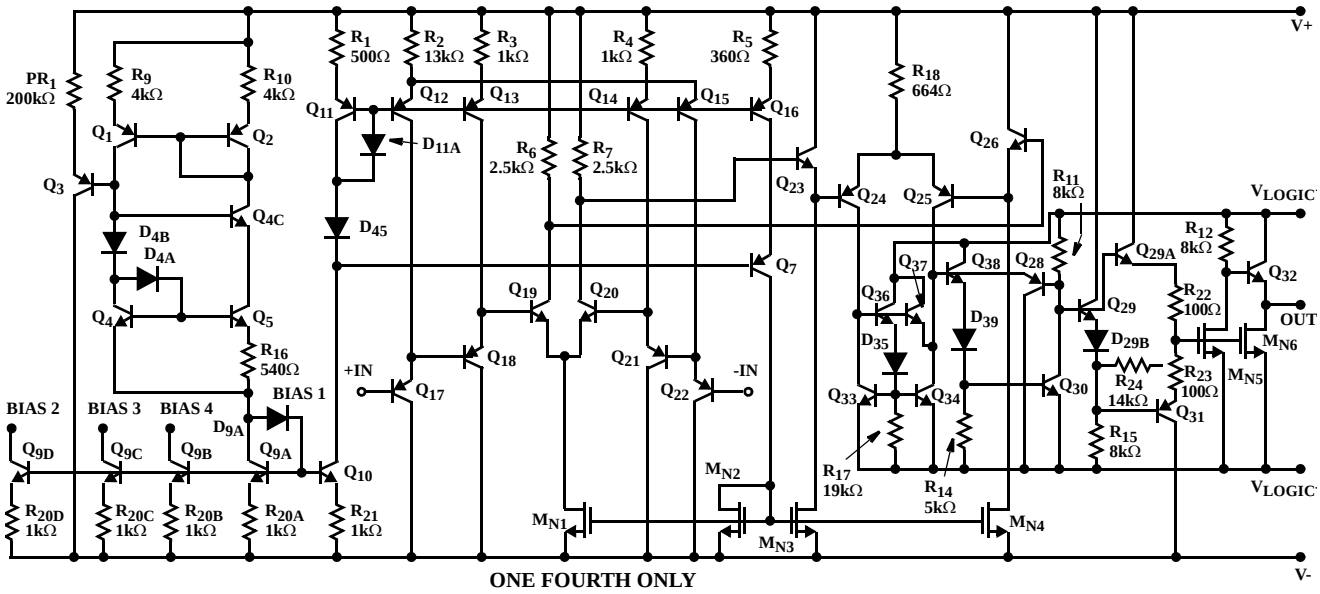


FIGURE 1.

Schematic Diagram



Applying the HA-4900 Series Comparators

Supply Connections

This device is exceptionally versatile in working with most available power supplies. The voltage applied to the V+ and V- terminals determines the allowable input signal range; while the voltage applied to the V_L+ and V_L- determines the output swing. In systems where dual analog supplies are available, these would be connected to V+ and V-, while the logic supply and return would be connected to V_{LOGIC}+ and V_{LOGIC}-. The analog and logic supply commons can be connected together at one point in the system, since the comparator is immune to noise on the logic supply ground. A negative output swing may be obtained by connecting V_L+ to ground and V_L- to a negative supply. Bipolar output swings ($15V_{P-P}$, Max) may be obtained using dual supplies. In systems where only a single logic supply is available (+5V to 15V), V+ and V_{LOGIC}+ may be connected together to the positive supply while V- and V_{LOGIC}- are grounded. If an input signal could swing negative with respect the V- terminal, a resistor should be connected in series with the input to limit input current to < 5mA since the C-B junction of the input transistor would be forward biased.

Unused Inputs

Inputs of unused comparator sections should be tied to a differential voltage source to prevent output "chatter."

Crosstalk

Simultaneous high frequency operation of all other channels in the package will not affect the output logic state of a given channel, provided that its differential input voltage is sufficient to define a given logic state ($\Delta V_{IN} \geq \pm V_{OS}$). Low level or high impedance input lines should be shielded from other signal sources to reduce crosstalk and interference.

Power Supply Decoupling

Decouple all power supply lines with 0.01µF ceramic capacitors to ground line located near the package to reduce coupling between channels or from external sources.

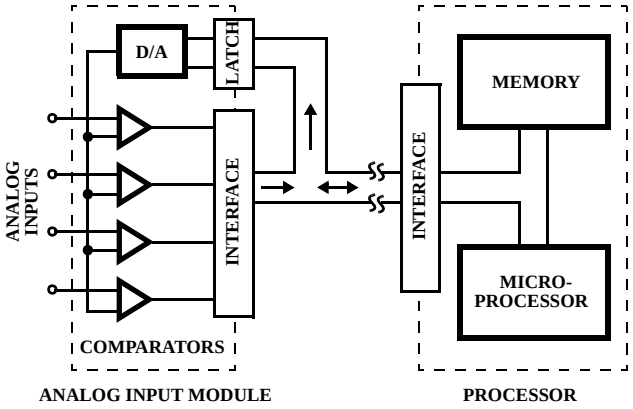
Response Time

Fast rise time (<200ns) input pulses of several volts amplitude may result in delay times somewhat longer than those illustrated for 100mV steps. Operating speed is optimized by limiting the maximum differential input voltage applied, with resistor-diode clamping networks.

Typical Applications

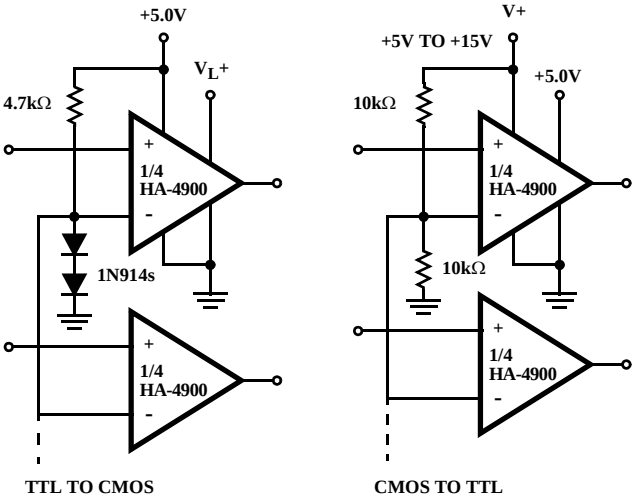
Data Acquisition System

In this circuit the HA-4900 series is used in conjunction with a D to A converter to form a simple, versatile, multi-channel analog input for a data acquisition system. In operation the processor first sends an address to the D to A, then the processor reads the digital word generated by the comparator outputs. To perform a simple comparison, the processor sets the D to A to a given reference level, then examines one or more comparator outputs to determine if their inputs are above or below the reference. A window comparison consists of two such cycles with 2 reference levels set by the D to A. One way to digitize the inputs would be for the processor to increment the D to A in steps. The D to A address, as each comparator switches, is the digitized level of the input. While stairstepping the D to A is slower than successive approximation, all channels are digitized during one staircase ramp.



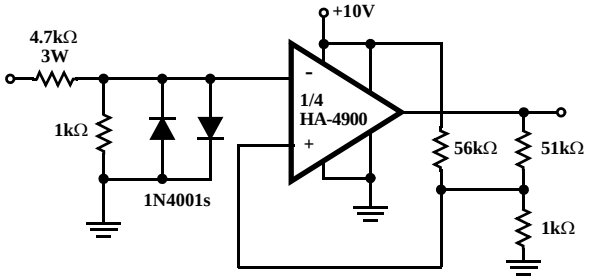
Logic Level Translators

The HA-4900 series comparators can be used as versatile logic interface devices as shown in the circuits above. Negative logic devices may also be interfaced with appropriate supply connections. If separate supplies are used for V- and V_{LOGIC}-, these logic level translators will tolerate several volts of ground line differential noise.



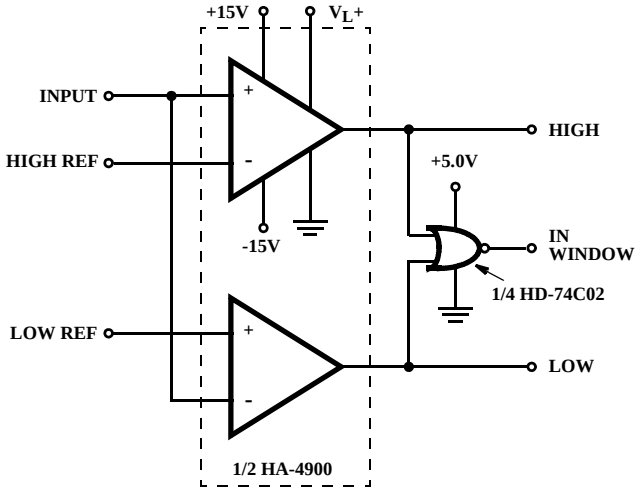
RS-232 To CMOS Line Receiver

This RS-232 type line receiver to drive CMOS logic uses a Schmitt trigger feedback network to give about 1V input hysteresis for added noise immunity. A possible problem in an interface which connects two equipments, each plugged into a different AC receptacle, is that the power line voltage may appear at the receiver input when the interface connection is made or broken. The two diodes and a 3W input resistor will protect the inputs under these conditions.



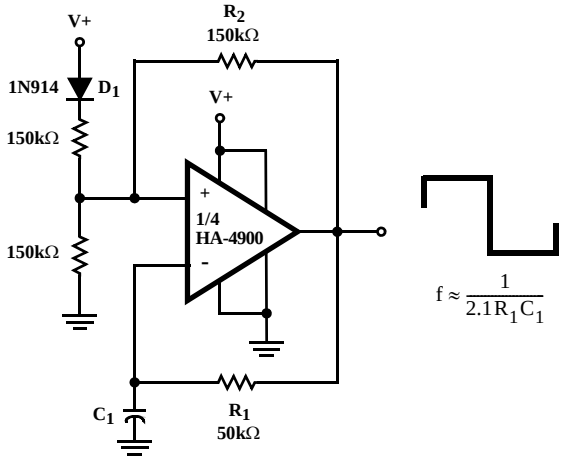
Window Detector

The high switching speed, low offset current and low offset voltage of the HA-4900 series makes this window detector circuit extremely well suited to applications requiring fast, accurate, decision-making. The circuit above is ideal for industrial process system feedback controllers or “out-of-limit” alarm indicators.



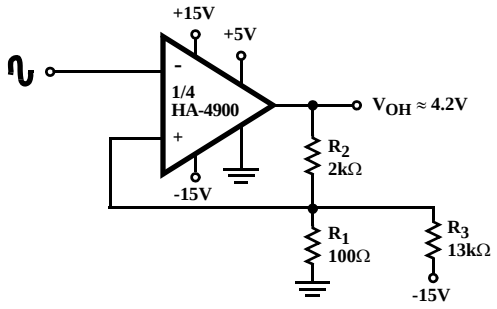
Oscillator/Clock Generator

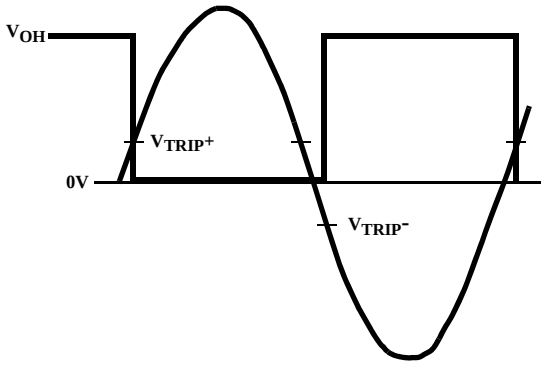
This self-starting fixed frequency oscillator circuit gives excellent frequency stability. R_1 and C_1 comprise the frequency determining network while R_2 provides the regenerative feedback. Diode D_1 enhances the stability by compensating for the difference between V_{OH} and V_{SUPPLY}. In applications where a precision clock generator up to 100kHz is required, such as in automatic test equipment, C_1 may be replaced by a crystal.



Schmitt Trigger (Zero Crossing Detector With Hysteresis)

This circuit has a 100mV hysteresis which can be used in applications where very fast transition times are required at the output even though the signal input is very slow. The hysteresis loop also reduces false triggering due to noise on the input. The waveforms below show the trip points developed by the hysteresis loop.





INPUT TO OUTPUT WAVEFORM SHOWING HYSTERESIS TRIP POINTS

Typical Performance Curves $T_A = 25^oC$, $V_S = \pm15V$, $V_{LOGIC}^+ = 5V$, $V_{LOGIC}^- = 0V$, Unless Otherwise Specified

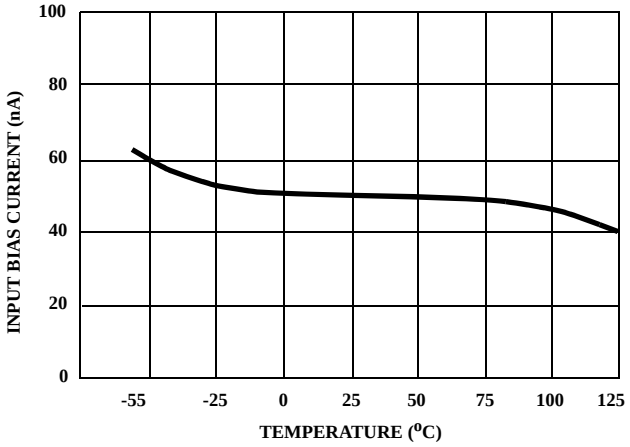


FIGURE 2. INPUT BIAS CURRENT vs TEMPERATURE

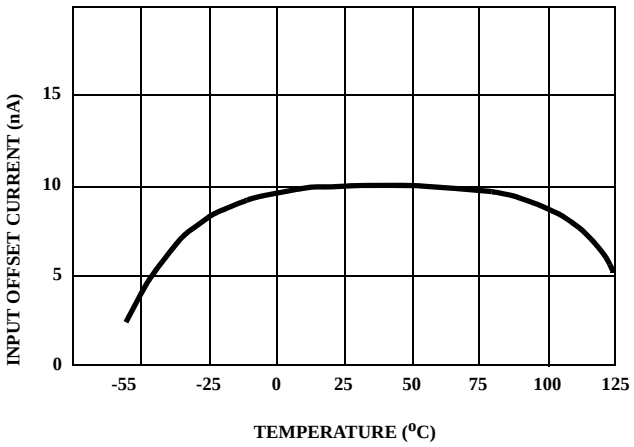


FIGURE 3. INPUT OFFSET CURRENT vs TEMPERATURE

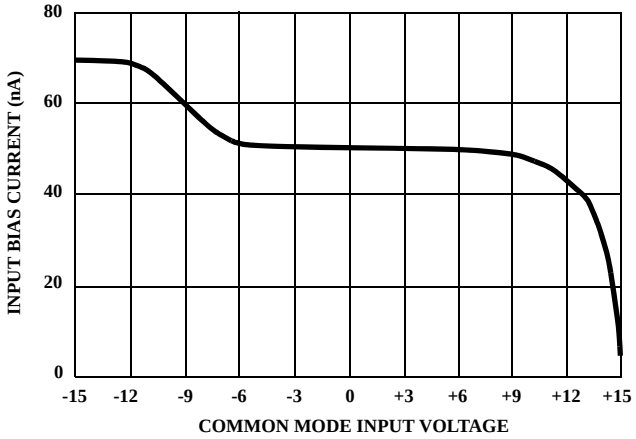


FIGURE 4. INPUT BIAS CURRENT vs COMMON MODE INPUT VOLTAGE (V_{DIFF} = 0V)

Typical Performance Curves $T_A = 25^oC$, $V_S = \pm15V$, $V_{LOGIC}^+ = 5V$, $V_{LOGIC}^- = 0V$, Unless Otherwise Specified **(Continued)**

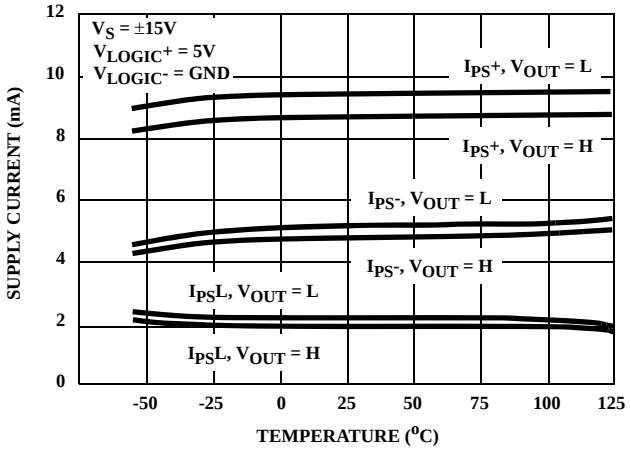


FIGURE 5. SUPPLY CURRENT vs TEMPERATURE (FOR ±15V SUPPLIES AND +5V LOGIC SUPPLY)

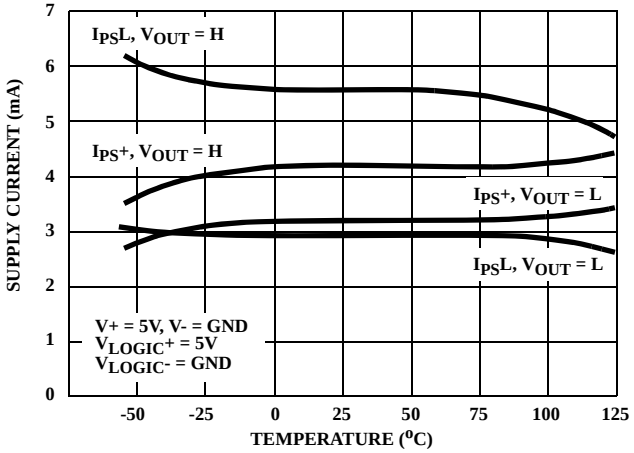
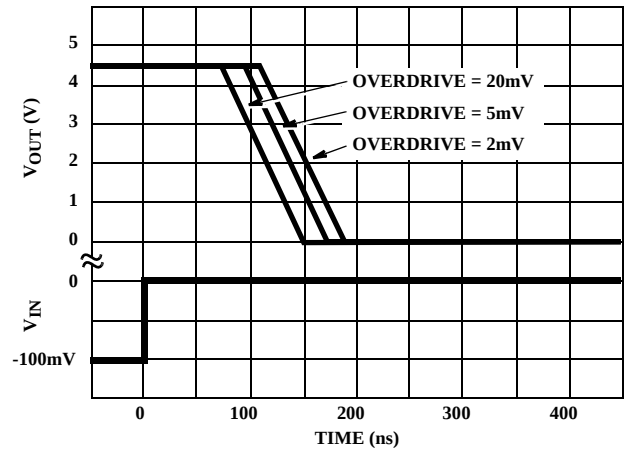


FIGURE 6. SUPPLY CURRENT vs TEMPERATURE (FOR SINGLE +5V OPERATION)



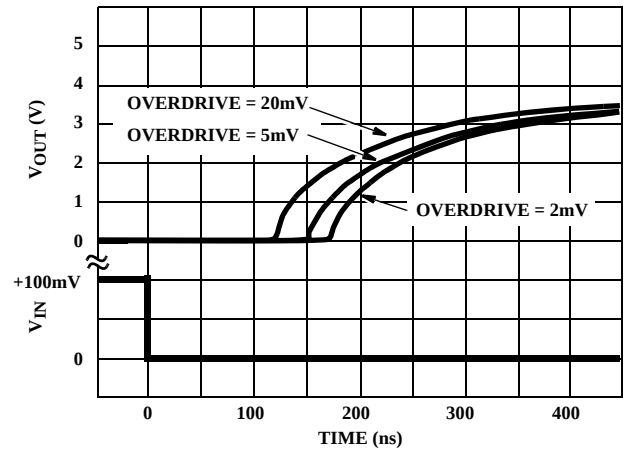


FIGURE 7. RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

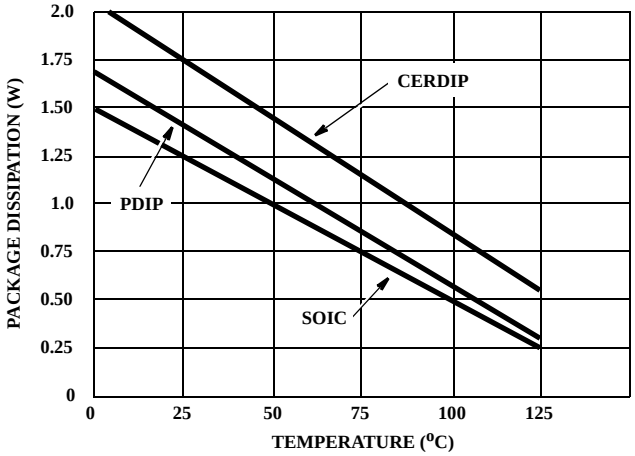


FIGURE 8. MAXIMUM PACKAGE DISSIPATION vs AMBIENT TEMPERATURE

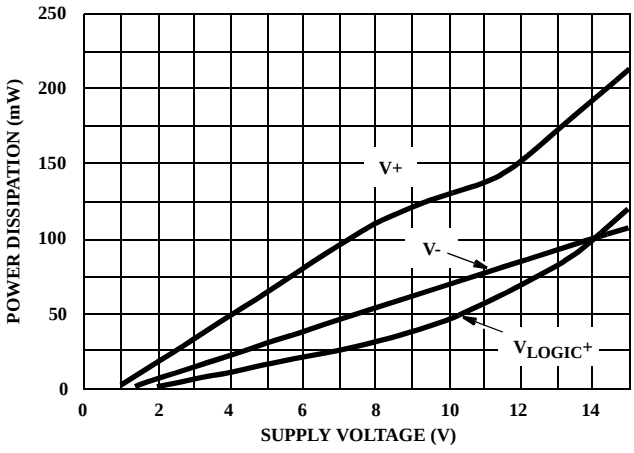
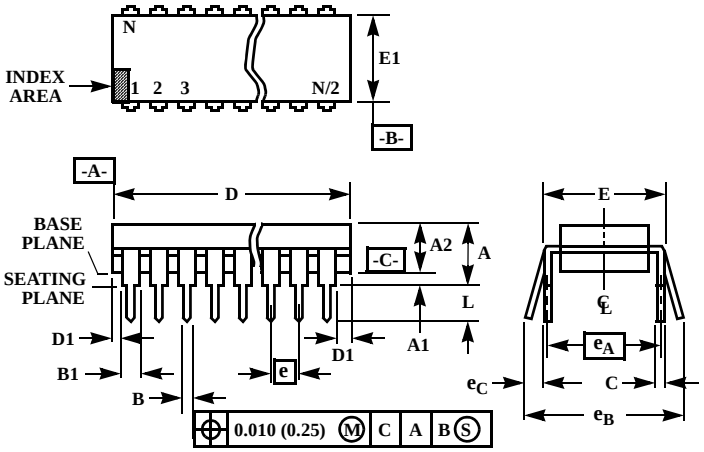


FIGURE 9. POWER DISSIPATION vs SUPPLY VOLTAGE (NO LOAD CONDITION)

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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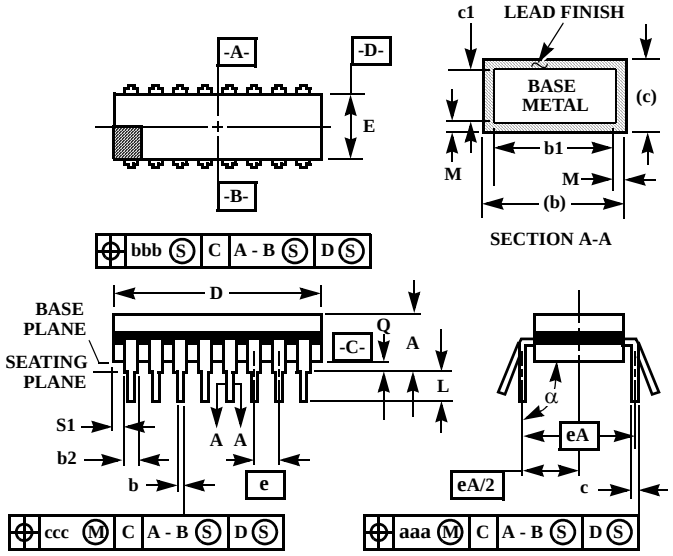
Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F16.3 MIL-STD-1835 GDIP1-T16 (D-2, CONFIGURATION A)
16 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.840	-	21.34	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	16		16		8

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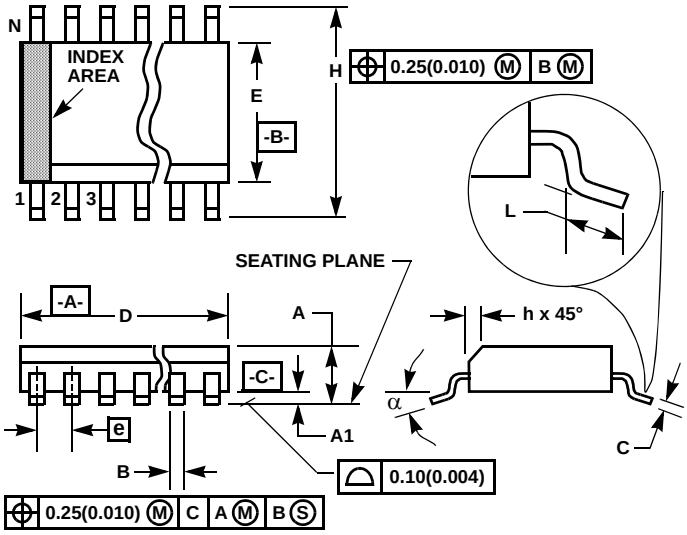
Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0°	8°	0°	8°	-

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