KMA7D0NP30Q

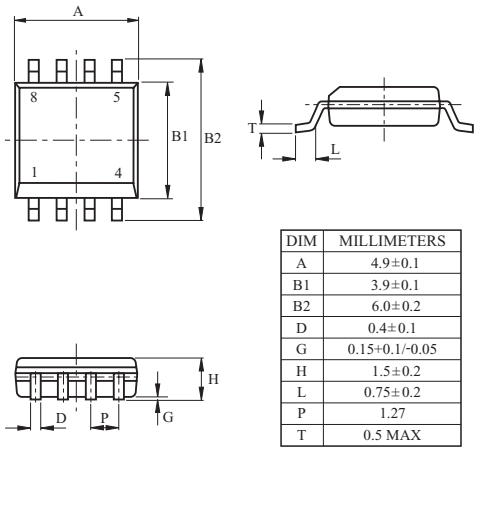
N and P-CH Trench MOSFET

General Description

Switching regulator and DC-DC converter applications.
It s mainly suitable for power management in notebook, portable equipment and battery powered systems.

FEATURES

· N-Channel
: V_{DSS}=30V, I_D=7A.
: $R_{DS(ON)}$=17m Ω(Typ.) @ V_{GS}=10V.
: $R_{DS(ON)}$=22m Ω(Typ.) @ V_{GS}=4.5V.
· P-Channel
: V_{DSS}=-30V, I_D=-5.5A.
: $R_{DS(ON)}$=35m Ω(Typ.) @ V_{GS}=-10V.
: $R_{DS(ON)}$=51m Ω(Typ.) @ V_{GS}=-4.5V.
· Super high dense cell design for extermely low $R_{DS(ON)}$.
· Reliable and rugged.



DIM	MILLIMETERS
A	4.9±0.1
B1	3.9±0.1
B2	6.0±0.2
D	0.4±0.1
G	0.15+0.1/-0.05
H	1.5±0.2
L	0.75±0.2
P	1.27
T	0.5 MAX

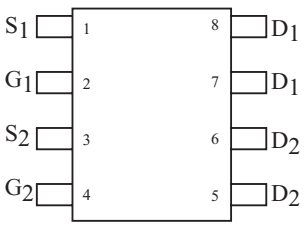
FLP-8

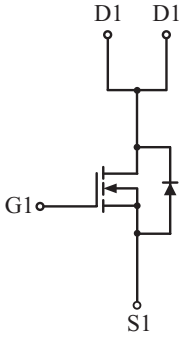
MAXIMUM RATING (Ta=25℃)

CHARACTERISTIC		SYMBOL	N-Ch	P-Ch	UNIT
Drain-Source Voltage		V_{DSS}	30	-30	V
Gate-Source Voltage		V_{GSS}	±20	±20	V
Drain Curren	DC	I_D *	7	-5.5	A
	Pulsed	I_{DP}	28	-20	
Drain Power Dissipation	Ta=25℃	P_D *	2		W
	Ta=100℃		0.8		
Maximum Junction Temperature		T_j	150		℃
Storage Temperature Range		T_{stg}	-55 ~ 150		℃
Thermal Resistance, Junction to Case		R_{thJA} *	62.5		℃/W

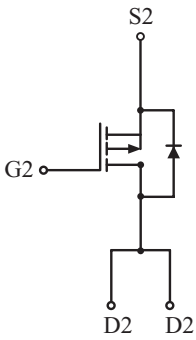
* : Surface Mounted on FR4 Board, t ≤ 10sec.

PIN CONNECTION (TOP VIEW)





N-Channel MOSFET



P-Channel MOSFET

ELECTRICAL CHARACTERISTICS (Ta=25℃)

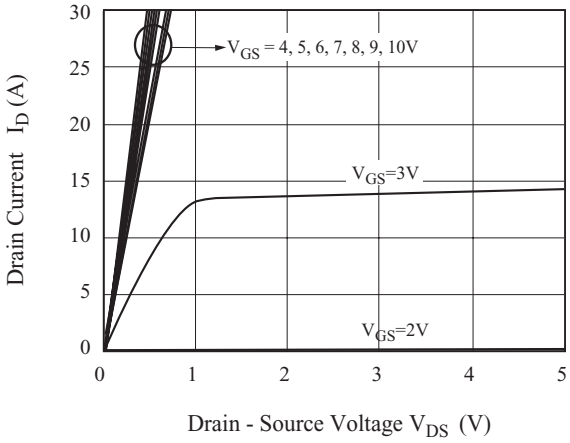
CHARACTERISTIC	SYMBOL	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	BV_{DSS}	I_D= ±250㎂, V_{GS}=0V	N-Ch	30	-	-	V
			P-Ch	-30	-	-	
Drain Cut-off Current	I_{DSS}	V_{DS}=24V, V_{GS}=0V	N-Ch	-	-	1	㎂
		V_{DS}=-24V, V_{GS}=0V	P-Ch	-	-	-1	
Gate Threshold Voltage	V_{th}	V_{DS}=V_{GS}, I_D= ±250㎂	N-Ch	1	1.5	2	V
			P-Ch	-1	-1.5	-2	
Gate Leakage Current	I_{GSS}	V_{GS}= ±20V, V_{DS}=0V	N-Ch P-Ch	-	-	±100	nA
Drain-Source ON Resistance	$R_{DS(ON)}$ (Note 1)	V_{GS}=10V, I_D=7A	N-Ch	-	17	24	mΩ
		V_{GS}=4.5V, I_D=5A		-	22	30	
		V_{GS}=-10V, I_D=-5.5A	P-Ch	-	35	56	
		V_{GS}=-4.5V, I_D=-4A		-	51	78	
Source-Drain Diode Forward Voltage	V_{SD} (Note 1)	I_{DR}=2A, V_{GS}=0V	N-Ch	-	0.7	1.3	V
		I_{DR}=-2.3A, V_{GS}=0V	P-Ch	-	-0.7	-1.3	
Dynamic (Note 2)							
Total Gate Charge	Q_g	N-Channel V_{DS}=15V, I_D=7A V_{GS}=10V P-Channel V_{DS}=-15V, I_D=-5.5A V_{GS}=-10V (Fig.1)	N-Ch	-	19	28	nC
			P-Ch	-	33	43	
Gate-Source Charge	Q_{gs}		N-Ch	-	1.6	-	
			P-Ch	-	5	-	
Gate-Drain Charge	Q_{gd}		N-Ch	-	3.6	-	
			P-Ch	-	4	-	
Turn-on Delay time	$t_{d(on)}$	N-Channel V_{DD}=15V, I_D=2A V_{IN}=10V, R_G=6Ω R_L=7.5Ω P-Channel V_{DD}=-15V, I_D=-2A V_{IN}=-10V, R_G=6Ω R_L=7.5Ω (Fig.2)	N-Ch	-	11	20	ns
			P-Ch	-	12	24	
Turn-on Rise time	t_r		N-Ch	-	17	28	
			P-Ch	-	15	29	
Turn-off Delay time	$t_{d(off)}$		N-Ch	-	36	62	
			P-Ch	-	35	60	
Turn-off Fall time	t_f		N-Ch	-	20	36	
			P-Ch	-	15	30	
Input Capacitance	C_{iss}	N-Channel V_{DS}=25V, V_{GS}=0V f=1.0MHz P-Channel V_{DS}=-25V, V_{GS}=0V f=1.0MHz	N-Ch	-	835	-	pF
			P-Ch	-	950	-	
Reverse Transfer Capacitance	C_{rss}		N-Ch	-	15	-	
			P-Ch	-	110	-	
Output Capacitance	C_{oss}		N-Ch	-	145	-	
			P-Ch	-	160	-	

Note 1) Pulse test : Pulse width ≤300㎲, duty cycle ≤2%

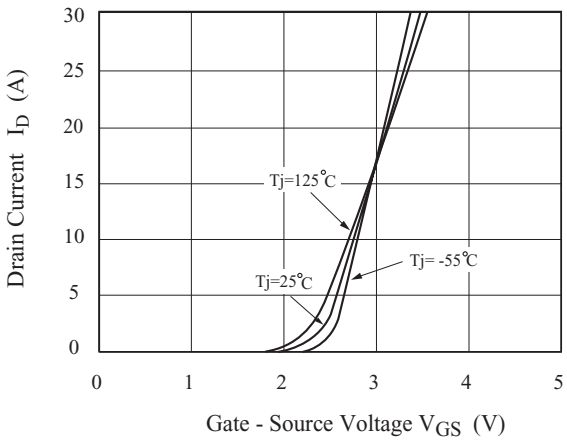
Note 2) Guaranteed by design, not subject to production testing.

N-Channel

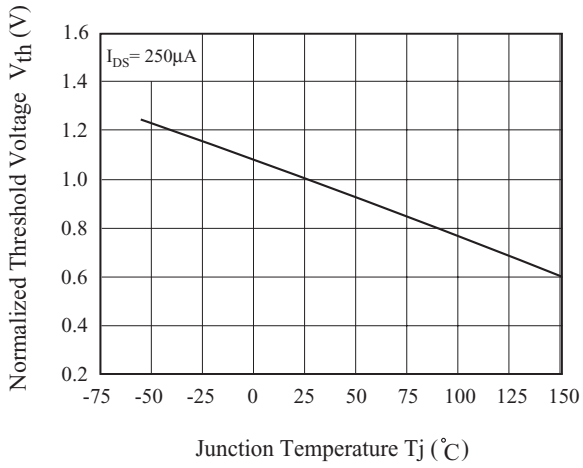
I_D - V_{DS}



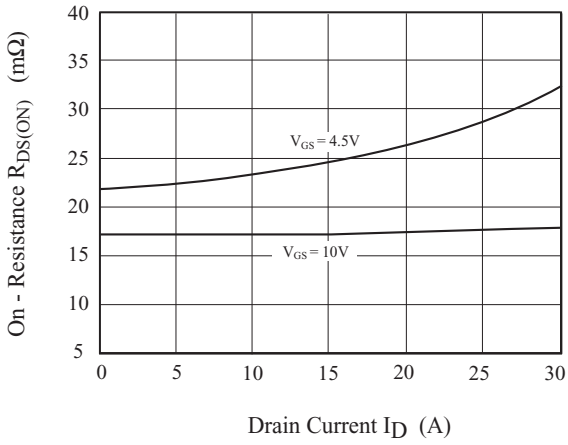
I_D - V_{GS}



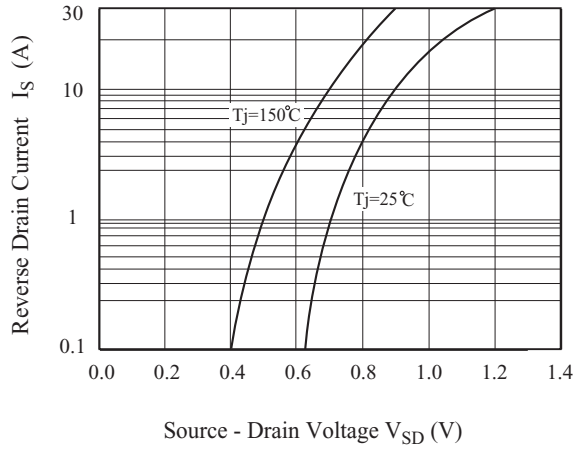
V_{th} - T_j



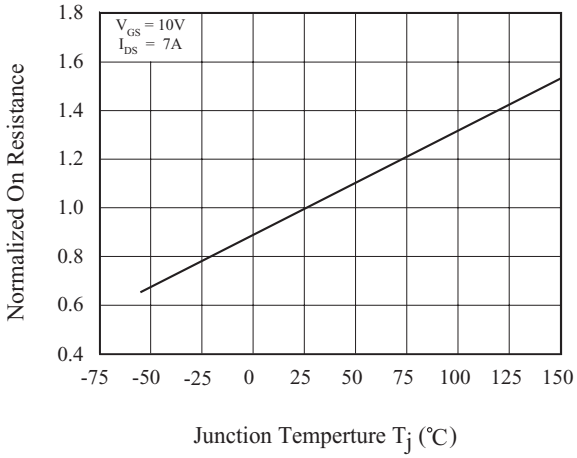
$R_{DS(ON)}$ - I_D



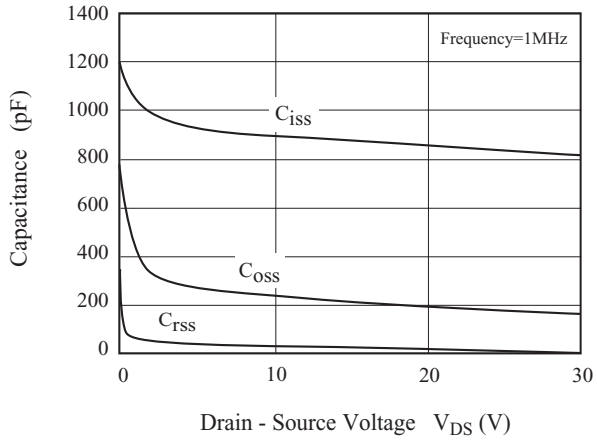
I_S - V_{SD}



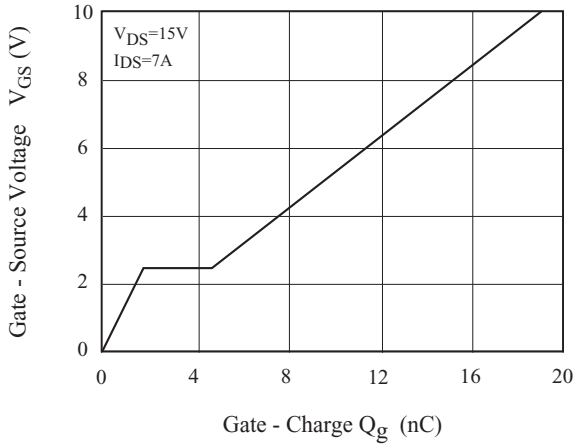
$R_{DS(ON)}$ - T_j



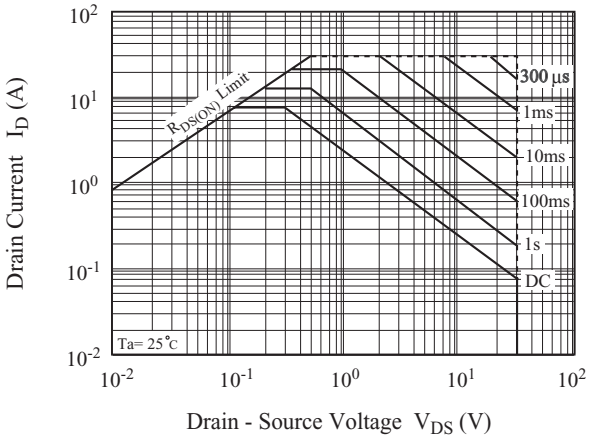
C - V_{DS}



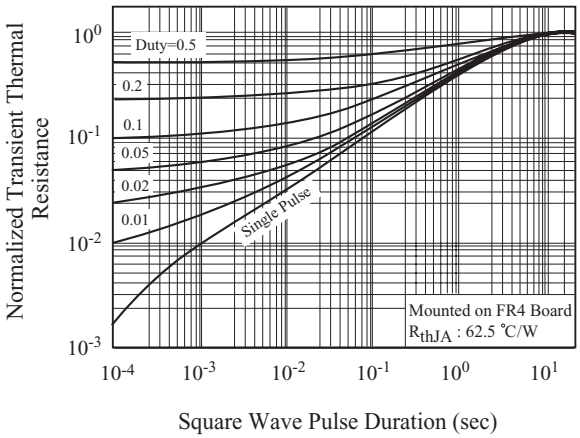
Q_g- V_{GS}



Safe Operation Area

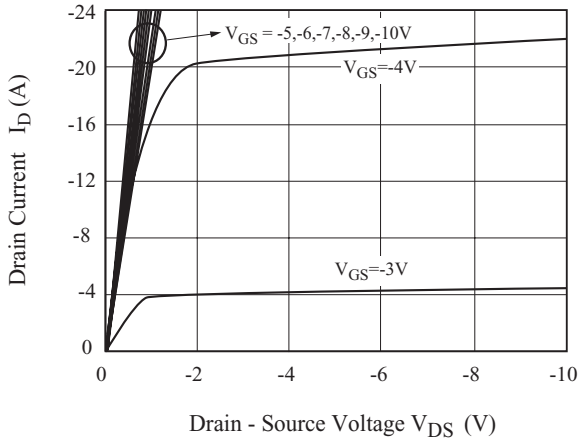


Rth

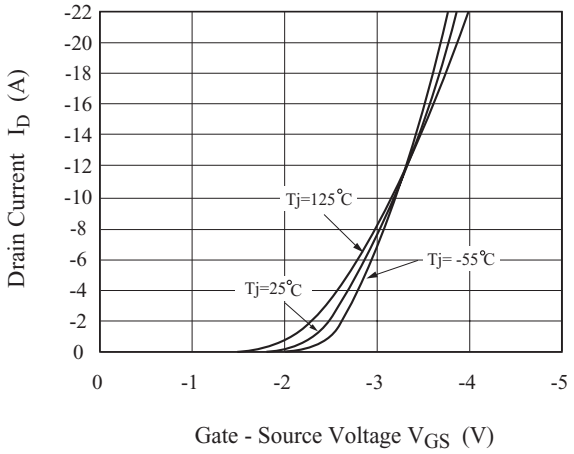


P-Channel

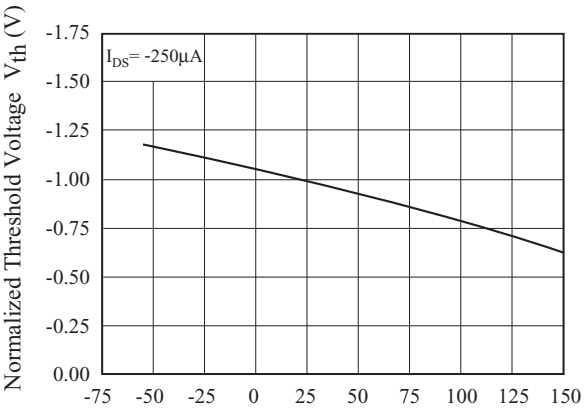
I_D - V_{DS}



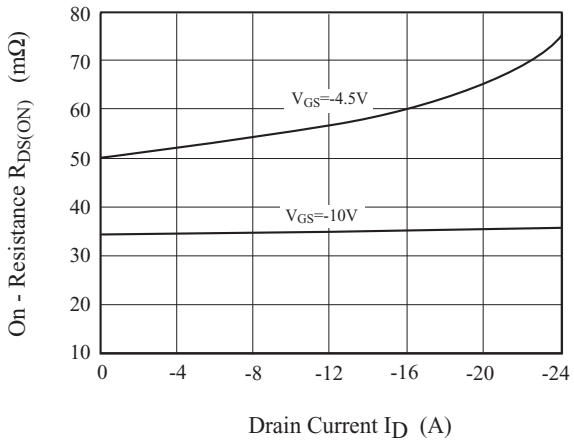
I_D - V_{GS}



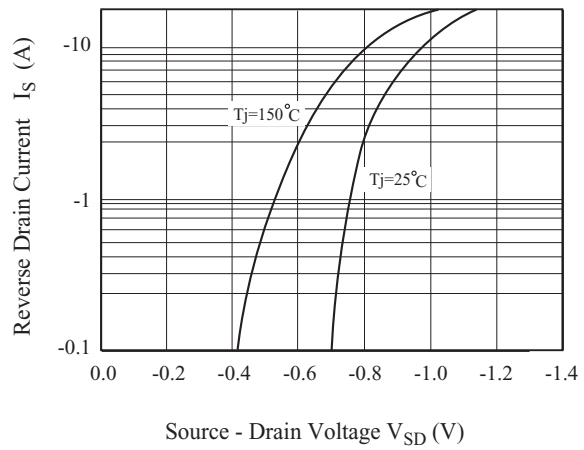
V_{th} - T_j



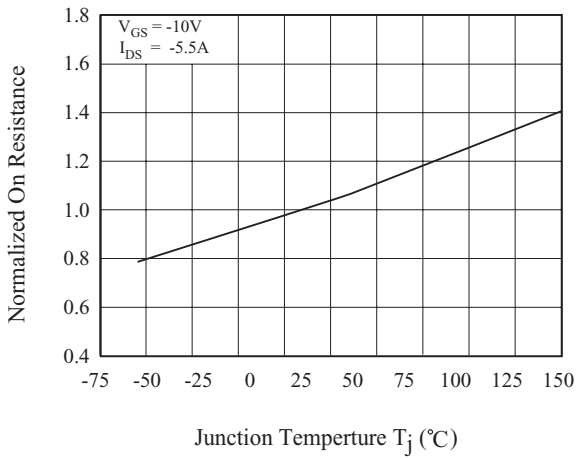
$R_{DS(ON)}$ - I_D



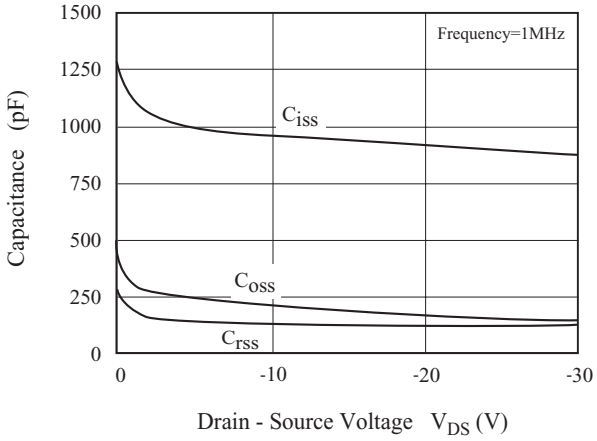
I_S - V_{SD}



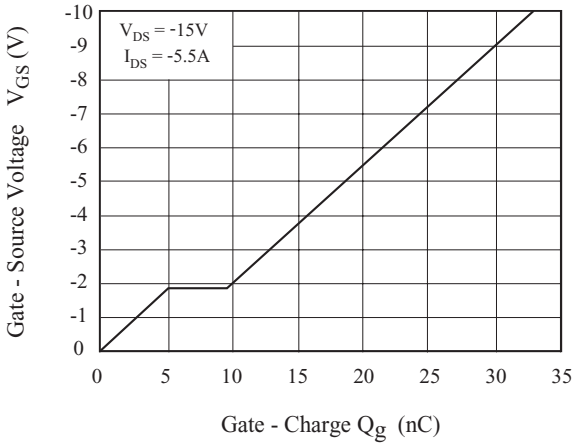
$R_{DS(ON)}$ - T_j



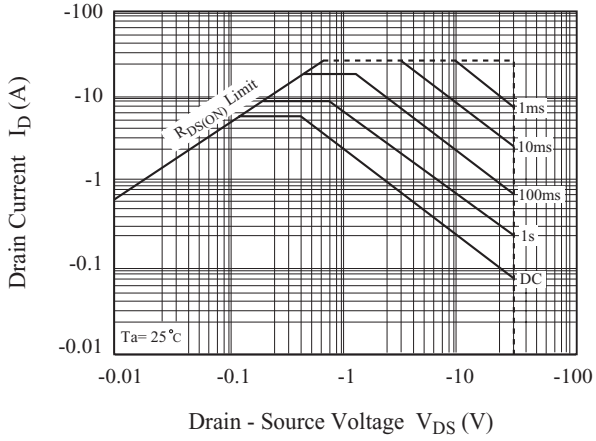
C - V_{DS}



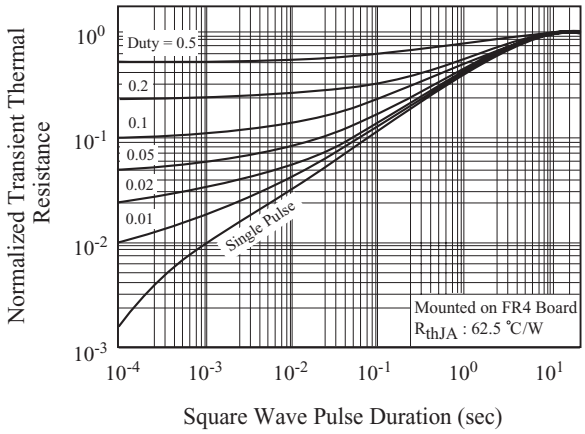
Q_g- V_{GS}



Safe Operation Area



Rth



N -Channel

Fig. 1 Gate Charge

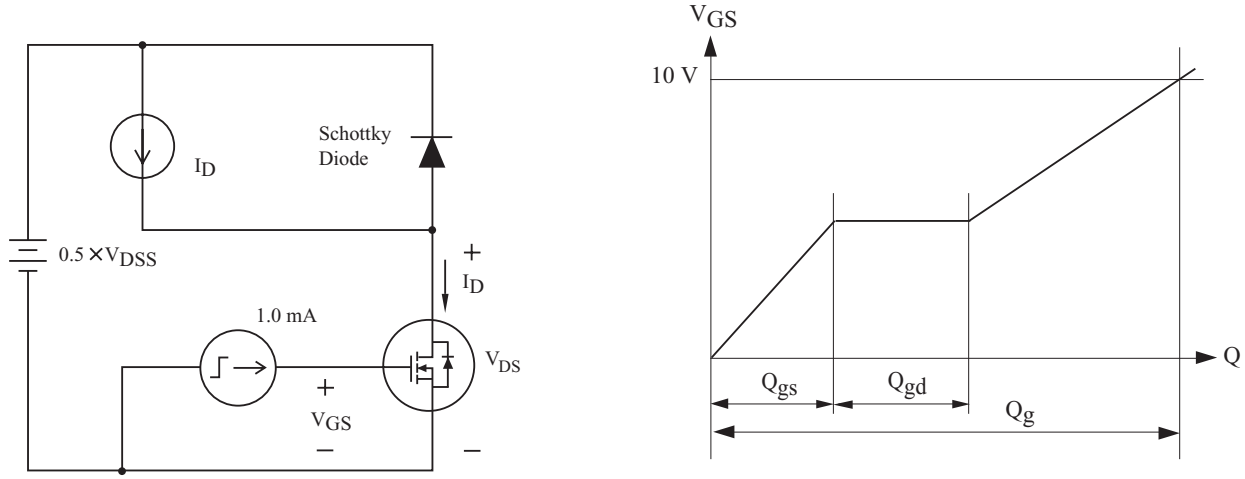
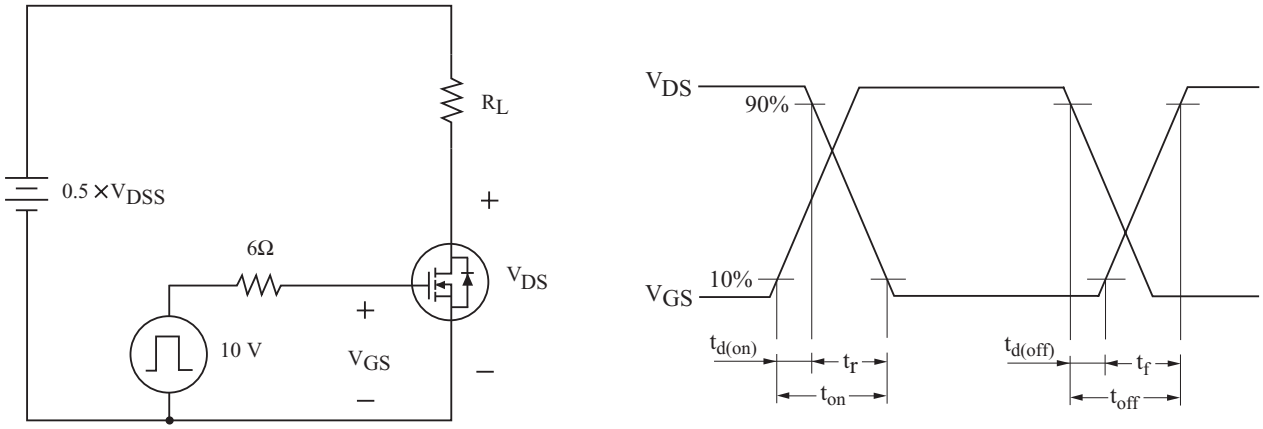
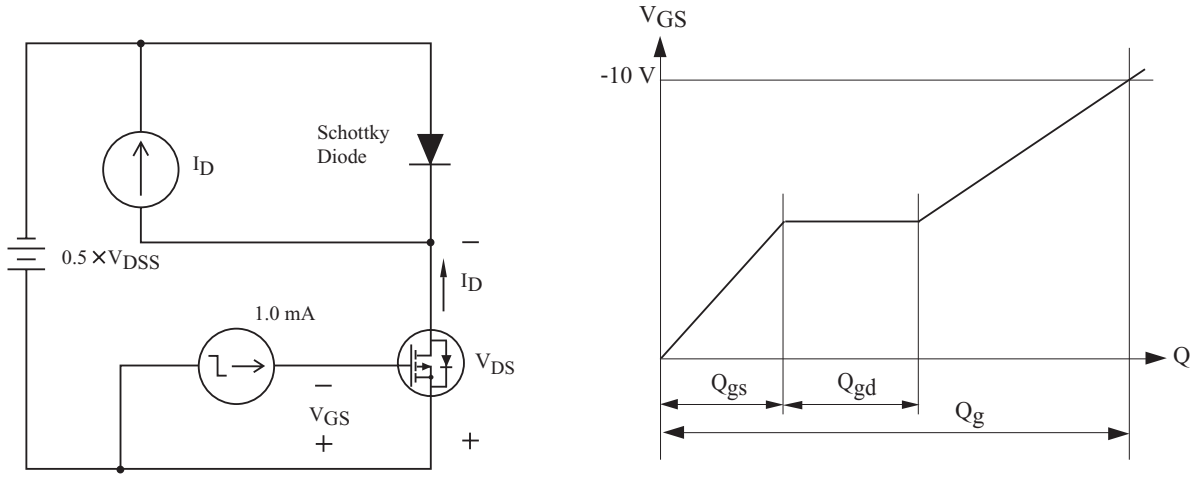


Fig. 2 Resistive Load Switching



P -Channel

Fig. 1 Gate Charge



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