Datasheet

Linear/PWM Constant Current VCM Driver

BU64291GWZ

●General Description

The BU64291GWZ is designed to drive voice coil motors (VCM) and operate with PWM to improve system power efficiency or switch to linear control to improve system noise. The driver includes ISRC (intelligent slew rate control) to reduce mechanical ringing to optimize the camera's auto focus capabilities.

●Features

- 2.3 V (Min.) driver power supply
- Selectable linear and PWM operational modes
- Current source and sink output
- 10 bit resolution current control
- ISRC mechanical ringing compensation
- 2-wire serial interface
- Integrated current sense resistor

●Applications

- Auto focus of Cell Phone
- Auto focus of Digital still camera
- Camera Modules
- Lens Auto focus
- Web, Tablet and PC cameras

●Key Specifications

PWM frequency:	0.5 to 2 MHz
Master clock:	400 kHz(Typ.)
Output ON resistance:	2.5 Ω (Typ.)
Maximum output current:	100 mA (Typ.)
Operating temperature range:	- 25 to + 85 °C

●Package(s)

Package	W(Typ.) x D(Typ.) x H(Max.)
UCSP30L1	0.77 mm x 1.37 mm x 0.33 mm

●Typical Application Circuit

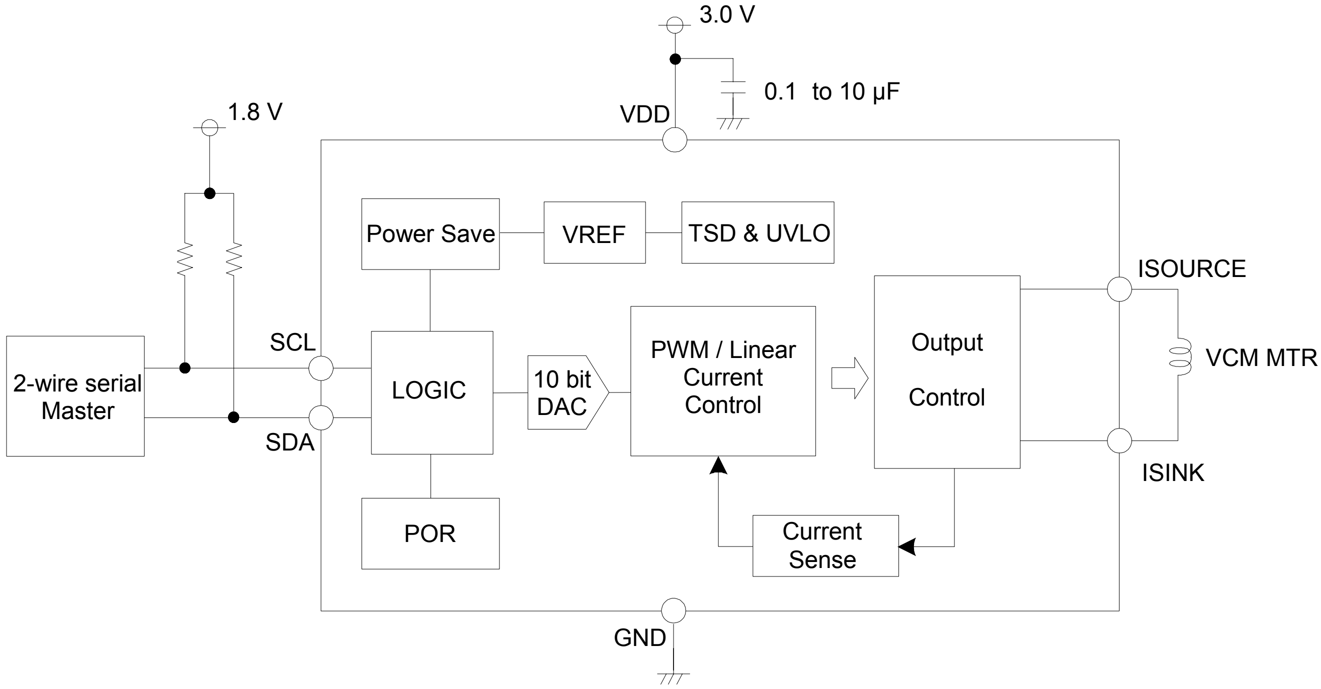


Figure.1 Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays

●Pin Configuration

	1	2
A	GND	VDD
B	ISINK	ISOURCE
C	SDA	SCL

Figure.2 Pin configuration (TOP VIEW)

●Pin Description

BALL No.	BALL Name	Function
A1	GND	Ground
A2	VDD	Power supply voltage
B1	ISINK	Current sink output
B2	ISOURCE	Current source output
C1	SDA	Serial data input
C2	SCL	Serial clock input

●Block Diagram

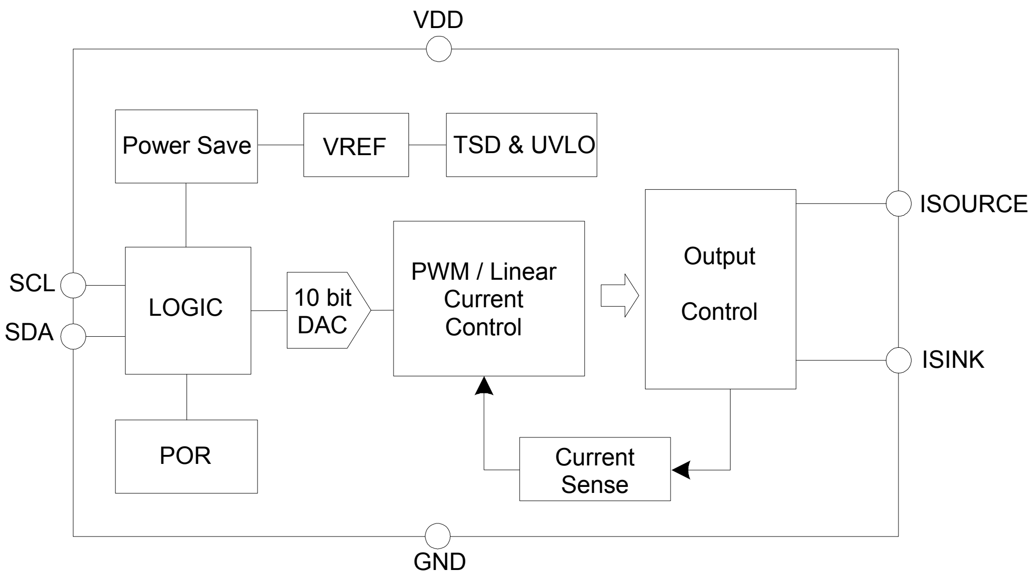


Figure 3. Block diagram

●Absolute Maximum Ratings

Parameter	Symbol	Limit	Unit
Power supply voltage	VDD	- 0.5 to + 5.5	V
Control input voltage (SCL, SDA)*1	VIN	- 0.5 to + 5.5	V
Power dissipation	Pd	390*2	mW
Operating temperature range	Topr	- 25 to + 85	°C
Junction temperature	Tjmax	125	°C
Storage temperature range	Tstg	- 55 to + 125	°C
Output current	IOUT	+ 200*3	mA

*1 VIN are 2-wire serial interface input pins (SCL, SDA)
*2 Reduced by 3.9 mW / °C over 25 °C when mounted on a glass epoxy board (50 mm × 58 mm × 1.75 mm; 8 layers)
*3 Must not exceed Pd, ASO, or Tjmax of 125 °C

●Recommended Operating Ratings

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	VDD	2.3	3.0	4.8	V
Control input voltage*1	VIN	0	-	4.8	V
2-wire serial interface frequency	FCLK	-	-	400	kHz
Output current	IOUT	-	-	100*4	mA

*1 VIN are 2-wire serial interface input pins (SCL, SDA)
*4 Must not exceed Pd, ASO

●Electrical Characteristics (Unless otherwise specified Ta = 25 °C, VDD = 3.0 V)

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
Power Consumption						
Standby current 1	ICCST1	-	70	100	μA	PS bit = 0
Standby current 2	ICCST2	-	70	100	μA	DAC code = 0x000
Circuit current	ICC	-	1.0	1.5	mA	
Control Input (VIN = SCL, SDA)						
High level input voltage	VINH	1.5	-	4.8	V	
Low level input voltage	VINL	0	-	0.5	V	
Low level output voltage	VINOL	-	-	0.4	V	IIN = + 3 mA (SDA)
High level input current	IINH	- 10	-	10	μA	Input voltage = 0.9 x VIN
Low level input current	IINL	- 10	-	10	μA	Input voltage = 0.1 x VIN
Under Voltage Lock Out						
UVLO voltage	VUVLO	1.6	-	2.2	V	
Master Clock						
MCLK frequency	MCLK	- 5	-	5	%	MCLK = 400 kHz
PWM Operation						
PWM frequency range	FPR	0.5	-	2	MHz	2-wire serial adjustable Default = 1 MHz*5
10 Bit D/A Converter (for Controlling Output Current)						
Resolution	DRES	-	10	-	bits	
Differential nonlinearity	DDNL	- 1	-	1	LSB	
Integral nonlinearity 1	DINL1	- 4	-	4	LSB	Linear operation
Integral nonlinearity 2	DINL2	- 4	-	4	LSB	PWM operation
Output Current Performance						
Output maximum current	IOMAX	95	100	105	mA	DAC code = 0x3FF
Zero code offset current	IOOFS	-	0	5	mA	DAC code = 0x000
Output resistance	ROUT	-	2.5	3.5	Ω	Ron_Pch + RNF or Ron_Nch + RNF

*5 PWM frequency range : 500 kHz to 2 MHz. (50 kHz step)

●Typical Performance Curves

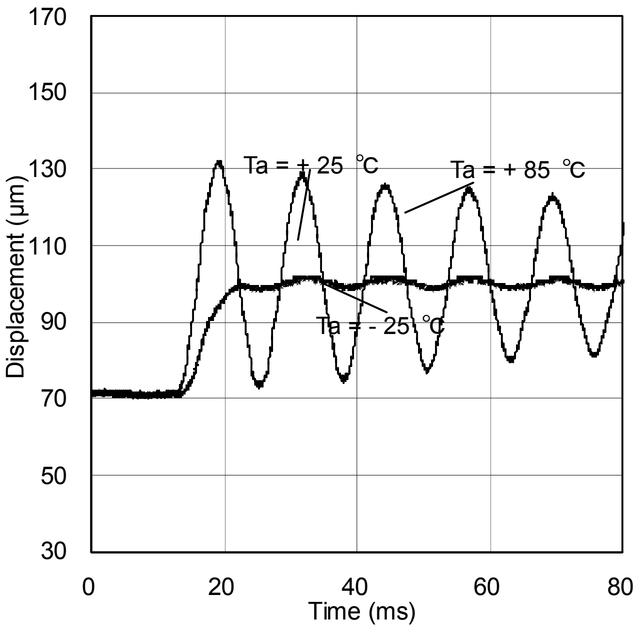


Figure 4. Output resistance (Ron_Pch + RNF)

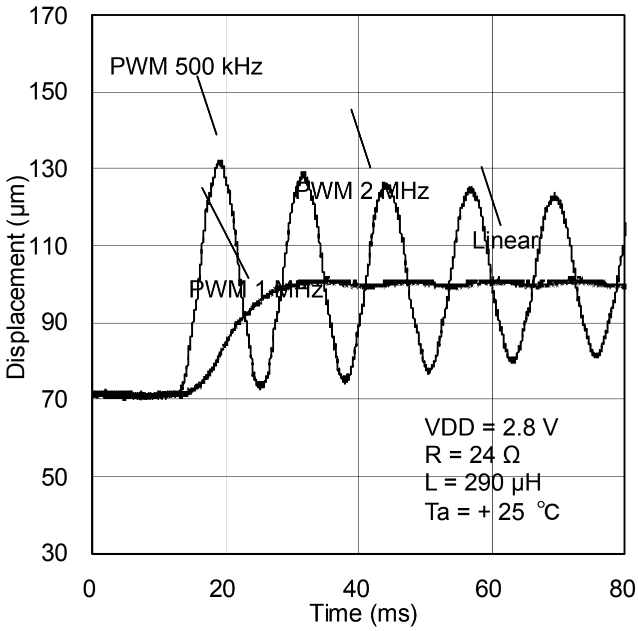


Figure 5. Efficiency vs. Output current

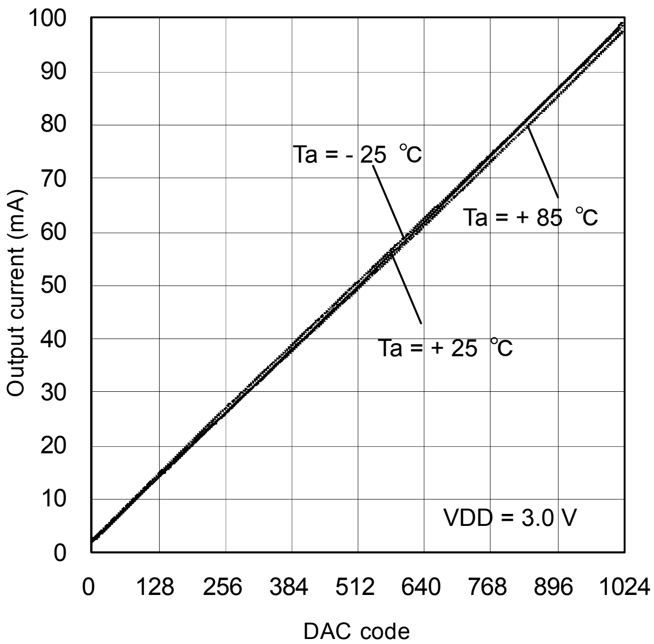


Figure 6. Output current vs. DAC code

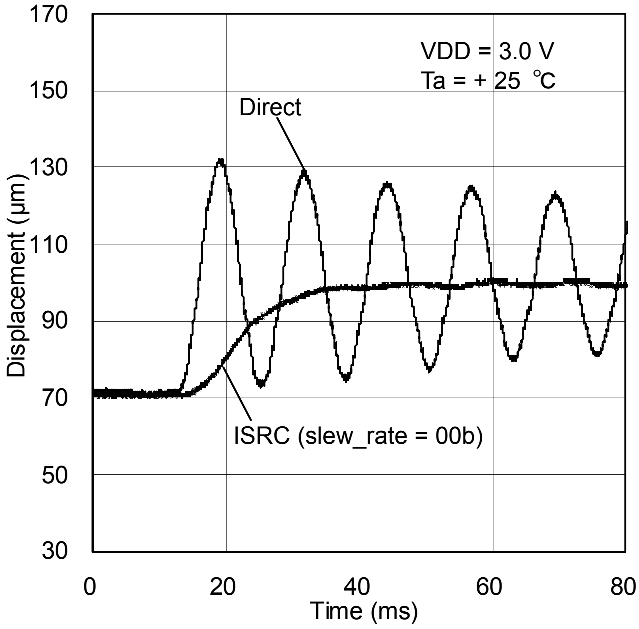


Figure 7. Displacement vs. settling time (slew_rate = 00b)

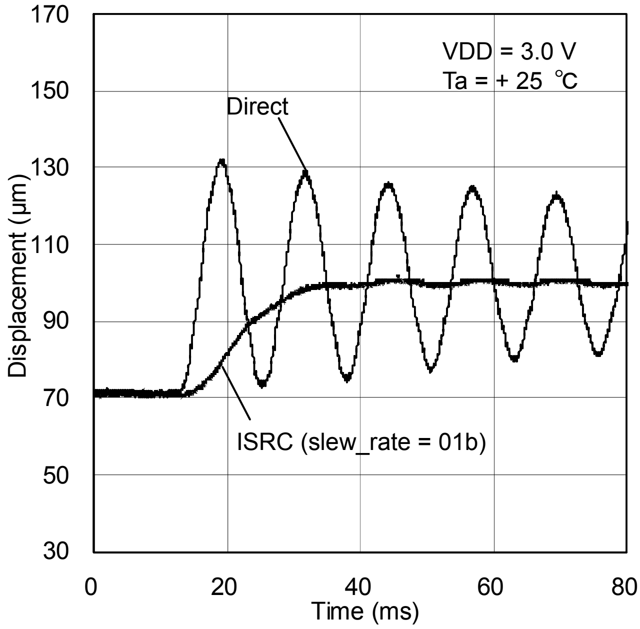


Figure 8. Displacement vs. settling time (slew_rate = 01b)

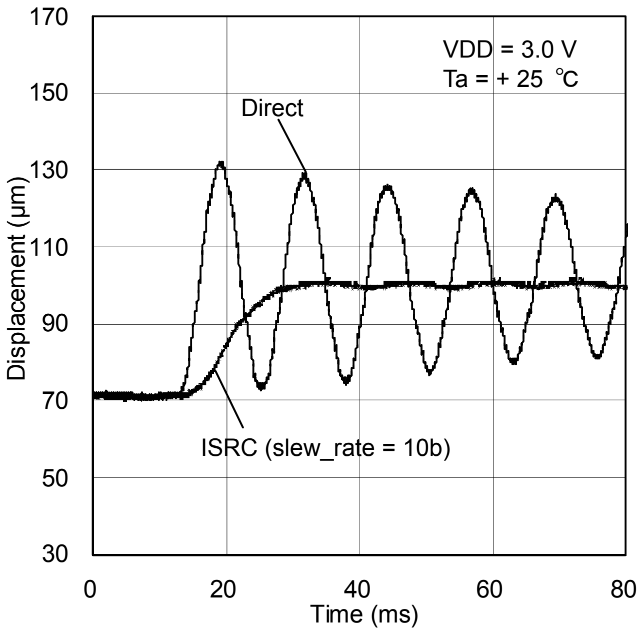


Figure 9. Displacement vs. settling time (slew_rate = 10b)

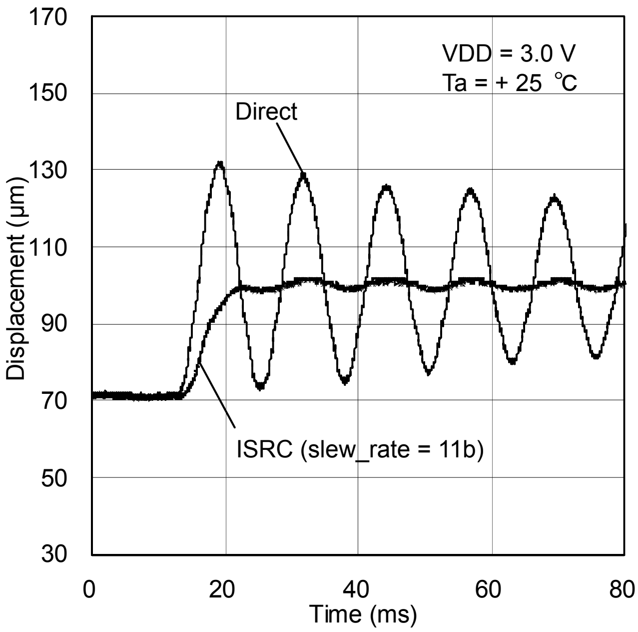


Figure 10. Displacement vs. settling time (slew_rate = 11b)

●2-wire serial interface Format (Fast mode SCL = 400 kHz)

S : start signal P : stop signal
A : acknowledge nA : non acknowledge ※ : Don't care

Register name	Setting item	Description
R/W	Read/write mode	0 = Write mode (0x18 address), 1 = Read mode (0x19 address)
PS	Serial power save	0 = Driver in standby mode(ISOURCE is Low), 1 = Driver in operating mode
EN	Driver output status	0 = ISOURCE output is Low. 1 = Current output is active.
M	Mode select	If W2 W1 W0 ≠ 110b, then M = 0 = ISRC mode disabled, M = 1 = ISRC mode enabled If W2 W1 W0 = 110b, then M = 0 = PWM output operation, M = 1 = linear output operation
W2W1W0	Register address	000b = Point C target DAC
		001b = Actuator frequency settings/slew rate settings
		010b = Point A target DAC
		011b = Point B target DAC
		100b = Step mode settings
		101b = PWM settings
		110b = Point C target DAC
D9 to D0	Data bits	Register data

●Register Update Timing

PS : Register is updated during the 2nd ACK response during a 3 byte 2-wire serial command
EN : Register is updated during the 3rd ACK response during a 3 byte 2-wire serial command
Wx : Register is updated during the 2nd ACK response during a 3 byte 2-wire serial command
M : Register is updated during the 3rd ACK response during a 3 byte 2-wire serial command
Dx : Register is updated during the 3rd ACK response during a 3 byte 2-wire serial command

●**Register Map**

Address	Bit	Bit Name	Function
000	D[9:0]	C_DAC1[9:0]	Point C DAC code setting 1[9:0]
001	D[9:8]		
	D[7:3]	rf[4:0]	Resonant frequency setting[4:0]
	D2		
	D[1:0]	slew_rate[1:0]	Slew rate speed setting[1:0]
010	D[9:0]	A_DAC[9:0]	Point A DAC code setting[9:0]
011	D[9:0]	B_DAC[9:0]	Point B DAC code setting[9:0]
100	D[9:8]		
	D[7:5]	str[2:0]	Step resolution setting[2:0]
	D[4:0]	stt[4:0]	Step time setting[4:0]
101	D[9:8]		
	D[7:2]	PWM_f[5:0]	PWM frequency setting[5:0]
	D[1:0]	slew_slope[1:0]	Output voltage slope setting[1:0]
110	D[9:0]	C_DAC2[9:0]	Point C DAC code setting 2[9:0]

●**Characteristics of the SDA and SCL Bus Lines for 2-wire Serial Interface** (Ta = 25 °C, VDD = 2.3 to 4.8 V)

Parameter	Symbol	STANDARD-MODE*6		FAST-MODE*6		Unit
		Min.	Max.	Min.	Max.	
Pulse width of spikes which must be suppressed by the input filter	tSP	0	50	0	50	ns
Hold time (repeated) start condition. The first clock pulse is generated after this period.	tHD;STA	4.0	-	0.6	-	μs
Low period of the SCL clock	tLOW	4.7	-	1.3	-	μs
High period of the SCL clock	tHIGH	4.0	-	0.6	-	μs
Set-up time for repeated START condition	tSU;STA	4.7	-	0.6	-	μs
Data hold time	tHD;DAT	0	3.45	0	0.9	μs
Data set-up time	tSU;DAT	250	-	100	-	ns
Set-up time for stop condition	tSU;STO	4.0	-	0.6	-	μs
Bus free time between a stop and start condition	tBUF	4.7	-	1.3	-	μs

*6 STANDARD-MODE and FAST-MODE 2-wire serial interface devices must be able to transmit or receive at the designated speed.
The maximum bit transfer rates are 100 kHz for STANDARD-MODE devices and 400 kHz for FAST-MODE devices.
This transfer rates is based on the maximum transfer rate. For example the bus is able to drive 100 kHz clocks with FAST-MODE.

●**2-wire Serial Interface Timing**

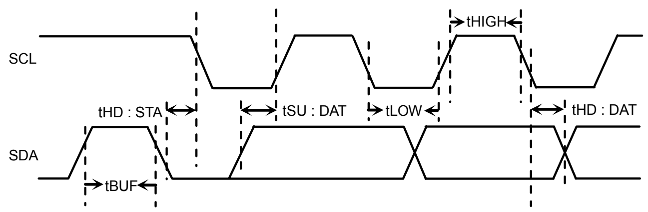


Figure 11. Serial Data Timing

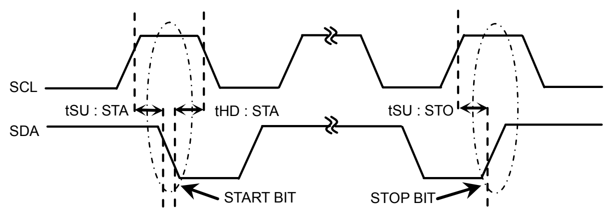


Figure 12. Start and Stop Bit Timing

●**Initialization Sequence** (Ta = 25 °C, VDD = 2.3 to 4.8 V)

Item	Symbol	Min.	Typ.	Max.	Unit
2-wire serial data start time	ti2c;s	15	-	-	μs
2-wire serial data stop time	ti2c;p	1.3	-	-	μs

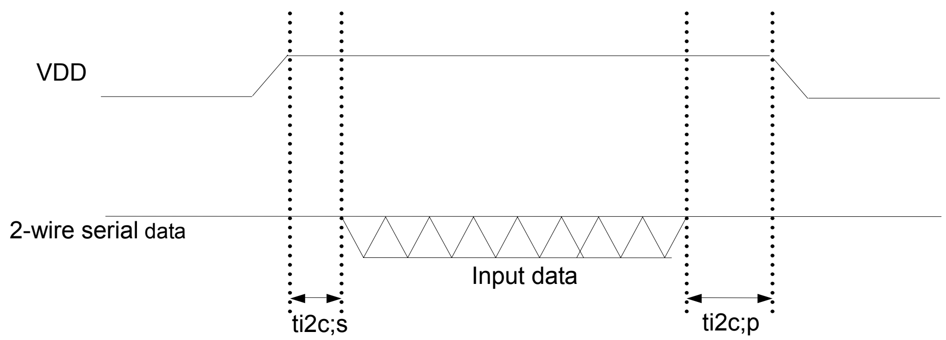
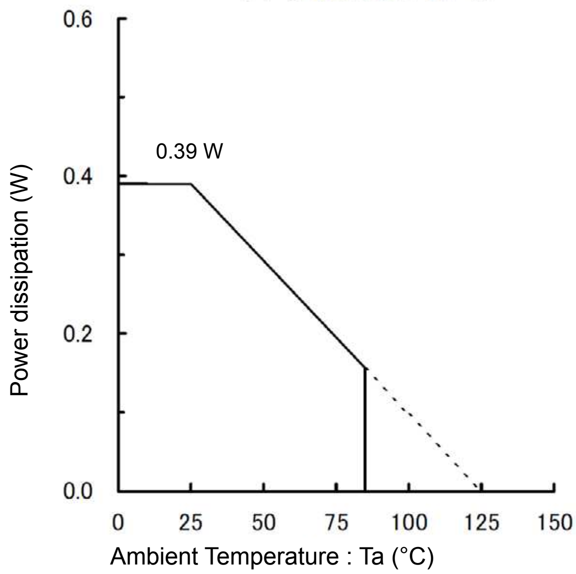


Figure 13. Timing Waveform Applying Power (VDD) Until Input of Serial Data

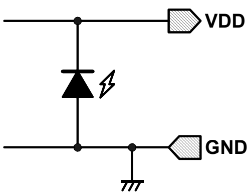
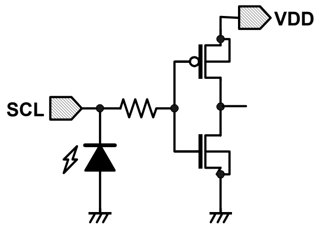
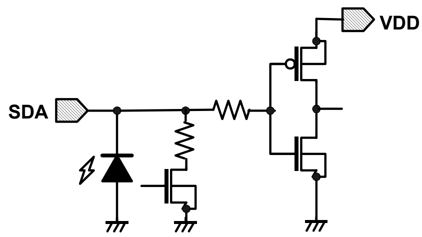
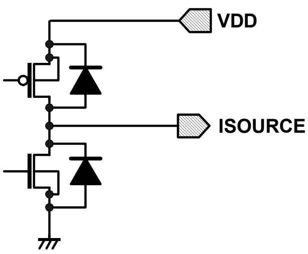
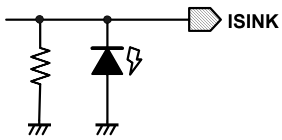
●Power Dissipation



(This value is not guaranteed value.)

Figure 14. Power dissipation Pd [W]

●I/O equivalence circuit

VDD	SCL	SDA
		
ISOURCE	ISINK	
		

●**Description of Functions**

1) **Controlling Mechanical Ringing**

A voice coil motor (VCM) is an actuator technology that is intrinsically noisy due to the properties of the mechanical spring behavior. As current passes through the VCM, the lens moves and oscillates until the system reaches a steady state. The BU64291GWZ lens driver is able to control mechanical oscillations by using the integrated ISRC (intelligent slew rate control) function. ISRC is operated by setting multiple control parameters that are determined by the intrinsic characteristics of the VCM. The following steps illustrate how to best utilize ISRC to minimize mechanical oscillations.

Step A1 – Determining the Resonant Frequency of the VCM

Each VCM has a resonant frequency that can either be provided by the manufacturer or measured. The resonant frequency of an actuator determines the amount of ringing (mechanical oscillation) experienced after the lens as been moved to a target position and the driver output current held constant. To determine the resonant frequency, f_0, input a target DAC code by modifying the 10 bit C_DAC1[9:0] value in register W2W1W0 = 000b that will target a final lens position approximately half of the actuator's full stroke. Take care to not apply too much current so that the lens does not hit the mechanical end of the actuator as this will show an incorrect resonant period. In order to start movement of the lens to the DAC code that was set in C_DAC1[9:0], the EN bit must be set to 1.

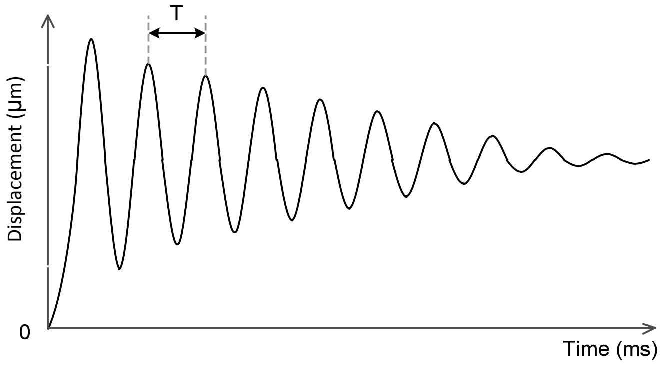


Figure 15. Actuator Displacement Waveform (ISRC Disabled)

The resonant frequency (Hz) of the actuator can be calculated with Equation 1 using the resonant period observed in Figure 15.

$$f_0 = (T)^{-1} \ldots (1)$$

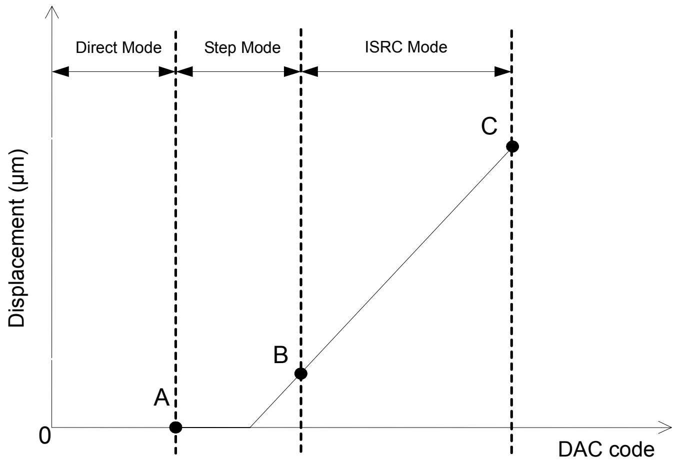
After calculating the correct resonant frequency, program the closest value in the W2W1W0 = 001b register using the 5 bit rf[4:0] values from Table 1. When calculating the resonant frequency take care that different actuator samples' resonant frequencies might vary slightly and that the frequency tolerance should be taken into consideration when selecting the correct driver resonant frequency value.

Table 1. f_0 Settings (rf[4:0])

rf[4:0]	f_0	rf[4:0]	f_0	rf[4:0]	f_0	rf[4:0]	f_0
00000	-	01000	85 Hz	10000	125 Hz	11000	-
00001	50 Hz	01001	90 Hz	10001	130 Hz	11001	-
00010	55 Hz	01010	95 Hz	10010	135 Hz	11010	-
00011	60 Hz	01011	100 Hz	10011	140 Hz	11011	-
00100	65 Hz	01100	105 Hz	10100	145 Hz	11100	-
00101	70 Hz	01101	110 Hz	10101	150 Hz	11101	-
00110	75 Hz	01110	115 Hz	10110	-	11110	-
00111	80 Hz	01111	120 Hz	10111	-	11111	-

Step A2 – Selecting the Autofocus Algorithm's Target DAC Codes

The ISRC algorithm is a proprietary technology developed to limit the ringing of an actuator by predicting the magnitude of ringing created by an actuator and intelligently controlling the output signal of the driver to minimize the ringing effect. Due to the ringing control behavior of ISRC, it is unable to operate properly unless the lens is floating (lens lifted off of the mechanical end of the actuator). As such the ringing control behavior is broken into three separate operational areas in order to provide the most optimally controlled autofocus algorithm.



A: lens displacement = 0 µm
B: all lenses floating
C: final lens position

Figure 16. Lens Displacement vs. DAC Code

Figure 16 illustrates the different operational modes that control the autofocus algorithm. Due to ISRC requiring a floating lens, points A and B need to bet set in order to create a floating condition. In order to simplify the code sequence, it is possible to skip setting point A and instead only set point B, however if an optimized ringing control method is preferred, point A corresponds to the maximum amount of current that can be applied to all VCM units without floating the lens. Point B corresponds to the minimum amount of current that can be applied to the VCM so that all actuator units are floating. It should be noted that the target DAC codes could vary between different actuator units and that sufficient evaluation should be performed before selecting the point A and B target DAC codes. Point C is the final lens target position determined by the level of focus required for the image capture.

The actuator manufacturer should be able to provide the required current for points A and B, however it is possible to test these points by slowly increasing the 10 bit value of C_DAC1[9:0] and measuring the lens movement using a laser displacement meter or some other device to measure lens displacement.

2) **Controlling the Driver**

After following steps A1 and A2 to characterize the VCM performance, the following steps should be followed in order to properly control the driver settings for optimized autofocus performance.

Step B1 – Setting Point A, B, and C DAC Codes

Points A, B, and C are defined by 10 bit DAC codes set with the following registers:

Location	W2W1W0 Register	DAC Code Location	Description
Point C	000	C_DAC1[9:0]	Final lens position before image capture
Point A	010	A_DAC[9:0]	Maximum output current without floating the lens
Point B	011	B_DAC[9:0]	Minimum output current required to float the lens
Point C	110	C_DAC2[9:0]	Final lens position before image capture

Although both C_DAC1[9:0] and C_DAC2[9:0] control the point C DAC code, the driver will only operate using the most recently programmed point C DAC code from either C_DAC1[9:0] or C_DAC2[9:0]. Updating the point C DAC code with two separate registers was implemented to help simply the coding process by allowing simple toggling of the M bit to enable/disable ISRC as well as PWM operation.

Step B2 – Controlling Direct Mode

Direct mode is when the driver outputs the desired amount of output current with no output current control. The time in which the lens reaches the position that corresponds to the amount of output current set by the 10 bit DAC code is ideally instant, ignoring the ringing effects. If the driver is set so that the lens is moved from a resting position to point C with direct mode, ringing and settling time will be at a maximum.

Direct mode is used either when M = 0 or when M = 1 and the present DAC code is less than the DAC code of point A.

M = 0 = ISRC mode disabled
When ISRC mode is disabled by setting the M bit equal to 0, the lens will traverse to the DAC code set for point C when the EN bit is set equal to 1.

M = 1 = ISRC mode enabled
The driver automatically uses direct mode if the present DAC code is less than the target DAC code corresponding to point A. Therefore during ISRC operation when the autofocus sequence has been started by setting the EN bit equal to 1, the driver will automatically decide to use direct mode to output current up to point A and then switch to step mode before continuing the autofocus sequence.

Step B3 – Controlling Step Mode

Step mode is the control period in which the lens is moved by small output current steps. During step mode it is possible to control the step resolution and step time in order to generate just enough output current to float the lens with minimal ringing effects. Ringing can be better controlled by choosing a large value for the step time and a small value for the step resolution with the trading off of a greater settling time. The step time and step resolution should be chosen depending on the acceptable system limits of ringing vs. settling time.

Step mode is used when M = 1 and the present DAC code is in between point A and point B. Typically this mode is only used during ISRC operation between point A and B, however it is possible to move the lens to point C using only step mode if point B is set such that point C is only 1 DAC code greater than point B.

Step mode is controlled by the 5 bit step time, stt[4:0], and 3 bit step resolution, str[2:0], values stored in register W2W1W0 = 100b.

Table 2. Step Time Settings (stt[4:0])

stt[4:0]	Step Time	stt[4:0]	Step Time	stt[4:0]	Step Time	stt[4:0]	Step Time
00000	-	01000	400 µs	10000	800 µs	11000	1200 µs
00001	50 µs	01001	450 µs	10001	850 µs	11001	1250 µs
00010	100 µs	01010	500 µs	10010	900 µs	11010	1300 µs
00011	150 µs	01011	550 µs	10011	950 µs	11011	1350 µs
00100	200 µs	01100	600 µs	10100	1000 µs	11100	1400 µs
00101	250 µs	01101	650 µs	10101	1050 µs	11101	1450 µs
00110	300 µs	01110	700 µs	10110	1100 µs	11110	1500 µs
00111	350 µs	01111	750 µs	10111	1150 µs	11111	1550 µs

Table 3. Step Resolution Settings (str[2:0])

str[2:0]	Step Resolution	str[2:0]	Step Resolution	str[2:0]	Step Resolution	str[2:0]	Step Resolution
000	-	010	2 LSB	100	4 LSB	110	6 LSB
001	1 LSB	011	3 LSB	101	5 LSB	111	7 LSB

As mentioned in step A2, it is possible to skip step mode during ISRC operation if a simpler autofocus code sequence is desired. If there is no issue with moving the lens to point B using direct mode, then the DAC code for point A should be left equal to 0. Additionally if the point A register is not set after the driver is initialized, then the driver will automatically move the lens to point B with direct mode since the default value for point A is 0.

Step B4 – Controlling ISRC Mode

ISRC mode is the control period in which the lens is already floating and the driver smoothly moves the lens based on the proprietary behavior of the ISRC algorithm. ISRC operation keeps ringing at a minimum while achieving the fastest possible settling time based on the ISRC operational conditions.

ISRC mode is used when M = 1 and the present DAC code is greater than the DAC code for point B. If the target DAC code for point C is set so that the value is too large and will cause excess ringing, the point C DAC code is automatically updated with a driver pre-determined value to minimize the ringing effect. When M = 1, the driver will automatically switch between direct mode, step mode, and ISRC mode when the point A, B, and C DAC code conditions are met. The condition for this automatic transitioning to occur is when the register values for point B and point C are set to values other than 0 and then the sequence will start when the EN bit is set equal to 1.

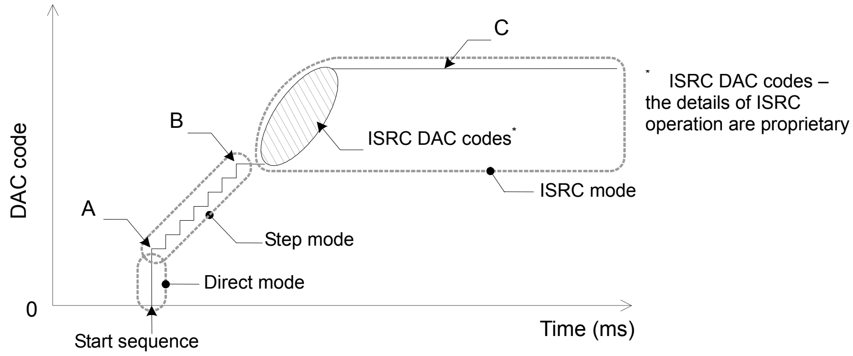


Figure 17. Three Mode Sequential Operation (Shown as DAC Codes)

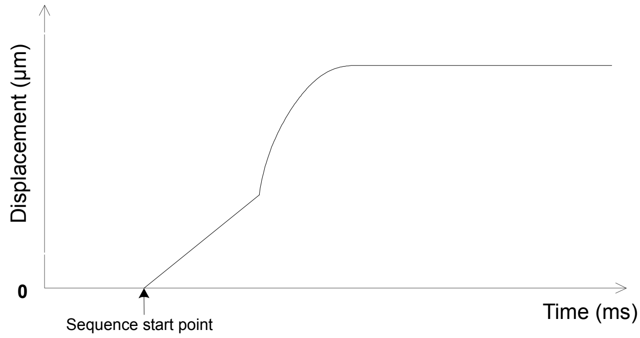


Figure 18. Three Mode Sequential Operation (Shown as Lens Displacement)

Step B5 – Controlling the ISRC Settling Time

The settling time of an actuator is the time it takes for ringing to cease. The BU64291GWZ is able to control the settling time by modifying the slew rate speed parameter, however care must be taken to balance settling time vs. acceptable ringing levels. By increasing the slew rate speed there is the possibility to decrease the settling time but the ability to control ringing is also decreased. Likewise if less ringing is desired then there is a possibility to reduce the ringing levels by using a slower slew rate speed setting at the cost of longer settling times. The slew rate speed can be set by modifying the 2 bit slew_rate[1:0] value in register W2W1W0 = 001b. Figure 19 shows the relationship of slew rate speed vs. settling time.

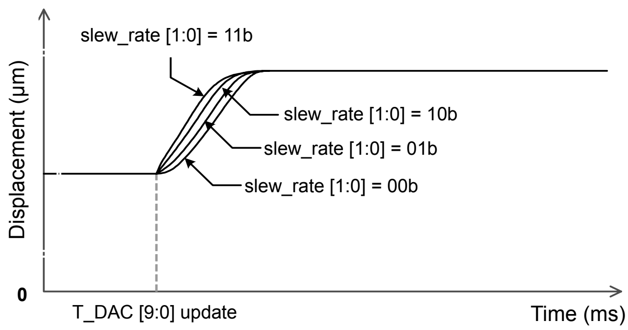


Figure 19. Displacement vs. Settling Time

Table 4. Slew Rate Speed Settings (slew rate [1:0])

slew_rate[1:0]	Slew Rate Speed	slew_rate[1:0]	Slew Rate Speed	slew_rate[1:0]	Slew Rate Speed	slew_rate[1:0]	Slew Rate Speed
00	Slowest	01	Slow	10	Fast	11	Fastest

Step B6 – DAC Code Update Timing Considerations

Settling time is controlled by the resonant frequency of the actuator and the driver's slew rate speed setting. Depending on the combination of these parameters, the settling time can be such that updating point C with a new DAC code before the lens has settled at the original point C DAC code can adversely affect the settling time due to increased ringing effects. Utilize the slew rate speed parameter in order to modify the settling time so that any updates to the point C DAC code do not occur before the lens has settled.

Please review the following example based on an actuator with a resonant frequency of 100 Hz:

Table 5. Relationship Between Slew Rate Speed and Settling Time Based on a 100 Hz Actuator

f_0	slew_rate[1:0]	Settling Time
100 Hz	00	40 ms
	01	24 ms
	10	16 ms
	11	12 ms

In this example the settling time of the actuator can vary by up to ± 5 % due to the internal oscillator (MCLK) having a variance of ± 5 %. The settling time has a proportionally inverse relationship to the resonant frequency and therefore the settling time can be estimated as:

Table 6. Relationship Between Slew Rate Speed and Settling Time Based on a General Resonant Frequency f_0'

f_0'	slew_rate[1:0]	Settling Time
f_0' Hz	00	$40 \times (100 / f_0')$ ms
	01	$24 \times (100 / f_0')$ ms
	10	$16 \times (100 / f_0')$ ms
	11	$12 \times (100 / f_0')$ ms

Note that the orientation of the camera module can affect the settling time due to the influence of gravity on the lens.

3) **PWM Operation**

The BU64291GWZ supports PWM operation with selectable 50 kHz PWM frequencies steps as well as PWM waveform slope control. Traditional VCM drivers operate with constant current drive and as the market moves more towards constant autofocus application use with video recording, camera power consumption concerns are becoming apparent. It should be noted that implementing PWM control in a camera module subsystem is difficult due to the noise generated by the PWM signal and the effect on image quality noise. As such there should be careful consideration when designing a camera module subsystem for use with PWM signals and that the designer should closely consult with the module maker, actuator manufacturer, and ROHM for design assistance. ROHM is able to provide design suggestions as well as driver operational guidelines to help minimize the influence of PWM noise on image quality.

Step C1 – Operating the Driver with PWM

The driver is set to default operate in PWM mode with a switching frequency of 1 MHz and a PWM waveform slope (slew slope) of MAX. The W2W1W0 = 110b register controls PWM or linear operation by modifying the M bit. When modifying the W2W1W0 = 110b M bit, it is also possible to update the point C DAC code in register W2W1W0 = 110b for quick autofocus target position changes.

M = 1 = linear operation

The point C DAC code is updated with the 10 bit C_DAC2[9:0] value stored in W2W1W0 = 110b. The driver will either operate with direct mode or ISRC mode depending on the M bit value stored in any register W2W1W0 ≠ 110b after the EN bit is set equal to 1.

M = 0 = PWM operation

The point C DAC code is updated with the 10 bit C_DAC2[9:0] value stored in W2W1W0 = 110b. The driver will either operate with direct mode or ISRC mode depending on the M bit value stored in any register W2W1W0 ≠ 110b after the EN bit is set equal to 1.

During driver operation it is possible to switch between linear and PWM operation by modifying the M bit and setting the same or a new point C DAC code with the W2W1W0 = 110b register without resetting the lens to a resting position. Values of the M bit which control direct mode or ISRC mode set by registers W2W1W0 ≠ 110b will not be affected when updating the M bit for PWM or linear operation with W2W1W0 = 110b. The driver will begin the autofocus sequence using either direct mode or ISRC mode when the EN bit is set to 1.

Step C2 – Setting the PWM Frequency

Although lower PWM frequencies result in optimized power efficiency, the BU64291GWZ allows for selectable PWM frequencies to help minimize any image quality noise issues created by PWM operation. Generally higher PWM frequencies result in slightly lower power efficiencies, however please choose the best PWM frequency for power efficiency vs. image quality noise vs. RF desense performance.

The PWM frequency is set by modifying the 6 bit PWM_f[5:0] value in register W2W1W0 = 101b. Please note that shaded cells in Table 7 are approximate reference values to be used for image noise evaluation. Only PWM frequencies from 500 kHz to 2 MHz are guaranteed for PWM frequency accuracy. The default PWM frequency after driver initialization is 1 MHz.

Table 7. PWM Frequency Settings (PWM_f [5:0])

PWM_f[5:0]	PWM Frequency	PWM_f[5:0]	PWM Frequency	PWM_f[5:0]	PWM Frequency	PWM_f[5:0]	PWM Frequency
000000	1000 kHz	001100	600 kHz	011000	1200 kHz	100100	1800 kHz
000001	50 kHz	001101	650 kHz	011001	1250 kHz	100101	1850 kHz
000010	100 kHz	001110	700 kHz	011010	1300 kHz	100110	1900 kHz
000011	150 kHz	001111	750 kHz	011011	1350 kHz	100111	1950 kHz
000100	200 kHz	010000	800 kHz	011100	1400 kHz	101000	2000 kHz
000101	250 kHz	010001	850 kHz	011101	1450 kHz	101001	1000 kHz
000110	300 kHz	010010	900 kHz	011110	1500 kHz	↑	
000111	350 kHz	010011	950 kHz	011111	1550 kHz		
001000	400 kHz	010100	1000 kHz	100000	1600 kHz		1000 kHz
001001	450 kHz	010101	1050 kHz	100001	1650 kHz		
001010	500 kHz	010110	1100 kHz	100010	1700 kHz	↓	
001011	550 kHz	010111	1150 kHz	100011	1750 kHz	111111	1000 kHz

Step C3 – Setting the PWM Waveform Slope

The slew slope parameter is used to modify the slope of the driver's PWM voltage output signal. The slew slope parameter is set by modifying the 2 bit slew_slope[1:0] value in register W2W1W0 = 101b. The default slew slope setting after driver initialization is the High slope value.

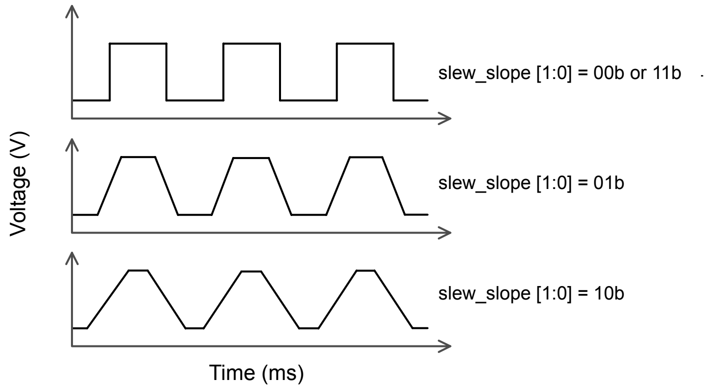


Figure 20. PWM Waveform Slope Comparison

It is possible to help improve image quality noise by limiting the voltage overshoot of the PWM signal by setting the slew slope value equal to 10b (Low) for the shallowest slope; however this is detrimental to power efficiency. For optimum power efficiency the slew slope should be set equal to 00b or 11b (High). Please choose the best setting for power efficiency vs. image quality noise.

Table 8. Slew Slope Settings (slew_slope [1:0])

slew_slope [1:0]	Output Voltage Slope	slew_slope [1:0]	Output Voltage Slope	slew_slope [1:0]	Output Voltage Slope	slew_slope [1:0]	Output Voltage Slope
00	High	01	Middle	10	Low	11	High

●Operational Notes

1) Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings such as the applied voltage or operating temperature range (Topr) may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is incurred. The implementation of a physical safety measure such as a fuse should be considered when there is use of the IC in a special mode where it's anticipated that the absolute maximum ratings may be exceeded.

2) Power supply lines
Regenerated current may flow as a result of the motor's back electromotive force. Insert capacitors between the power supply and ground pins to serve as a route for regenerated current. Determine the capacitance based on of all the characteristics of an electrolytic capacitor due to the electrolytic capacitor possibly losing some capacitance at low temperatures. If the connected power supply does not have sufficient current absorption capacity, regenerative current will cause the voltage on the power supply line to rise, which combined with the product and its peripheral circuitry may exceed the absolute maximum ratings. It is recommended to implement a physical safety measure such as the insertion of a voltage clamp diode between the power supply and GND pins.

3) Ground potential
Ensure a minimum GND pin potential in all operating conditions.

4) Heat dissipation
Use a thermal design that allows for a sufficient margin regarding the power dissipation (Pd) during actual operating conditions.

5) Use in strong magnetic fields
Use caution when using the IC in the presence of a strong magnetic field as doing so may cause the IC to malfunction.

6) ASO
When using the IC, set the output transistor for the motor so that it does not exceed absolute maximum ratings or ASO.

7) Thermal shutdown circuit
This IC incorporates a TSD (thermal shutdown) circuit. If the temperature of the chip reaches the below temperature, the motor coil output will be opened. The thermal shutdown circuit (TSD circuit) is designed only to shut off the IC to prevent runaway thermal operation. It is not designed to protect the IC or to guarantee its operation. Do not continue to use the IC after use of the TSD feature or use the IC in an environment where the its assumed that the TSD feature will be used.

TSD ON temperature [°C] (Typ.)	Hysteresis temperature [°C] (Typ.)
150	20

8) Ground Wiring Pattern
When using GND patterns for both small signal and large currents, it is recommended to isolate the two ground patterns by placing a single ground point at the application's reference point. This will help to alleviate noise in the small signal ground voltage due to noise created by the ground pattern wiring resistance for large current blocks. Be careful not to change the GND wiring pattern of any external components.

Status of this document
The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document formal version takes priority

●Ordering Information

B	U	6	4	2	9	1	G	W	Z		TR

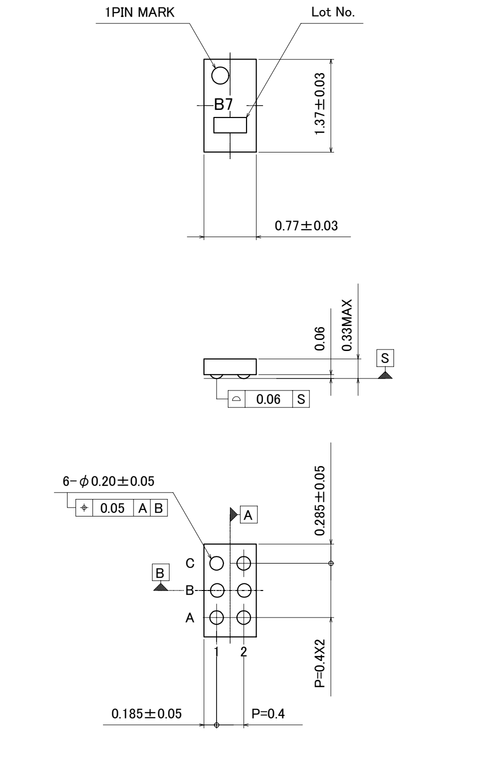
Part Number

Package
GWZ: UCSP30L1

Packaging and forming specification
TR: Embossed carrier tape

●Physical Dimension Tape and Reel Information

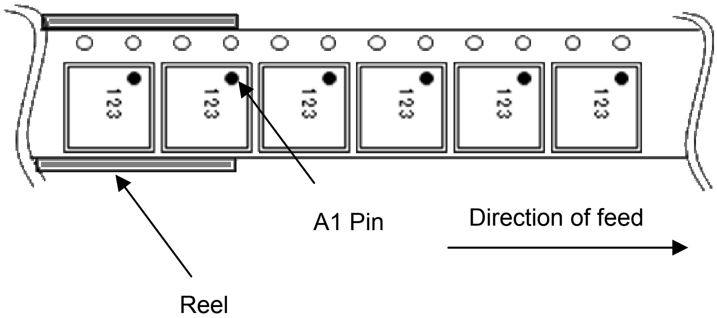
UCSP30L1 (BU64291GWZ)



(Unit:mm)

<Tape and Reel Information>

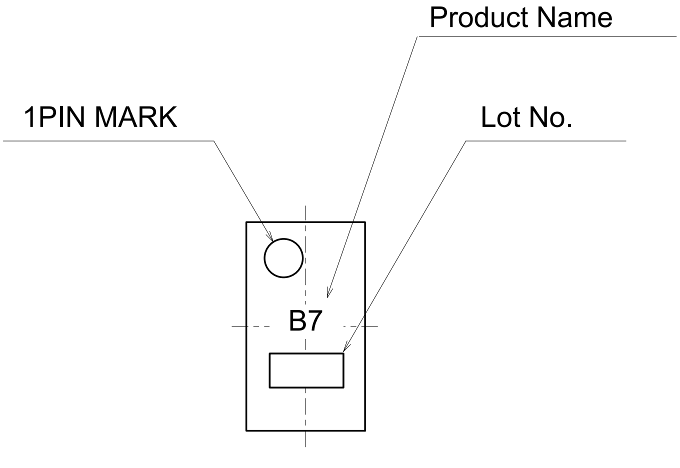
Tape	Embossed carrier tape
Quantity	6,000 pcs / reel
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the right hand)



*Order quantity needs to be multiple of the minimum quantity.

●Marking Diagram(TOP VIEW)

UCSP30L1 (BU64291GWZ)



●Revision History

Date	Revision	Changes
6.Aug.2012	001	New Release
5.Oct.2012	002	Change tape and reel information (P.20)

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4) The Products are not subject to radiation-proof design.

5) Please verify and confirm characteristics of the final or mounted products in using the Products.

6) In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse) is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7) De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8) Confirm that operation temperature is within the specified range described in the product specification.

9) ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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1) When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2) In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

●Precautions Regarding Application Examples and External Circuits

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   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2) Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3) Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4) Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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