

# 4V Drive Pch MOSFET

# UM6J1N

#### Structure

Silicon P-channel MOSFET

# ● Features

- 1) Two RSU002P03 transistors in a single UMT package.
- 2) The MOSFET elements are independent, eliminating mutual interference.
- 3) Mounting cost and area can be cut in half.

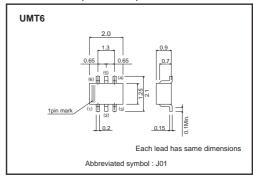
## Applications

Switching

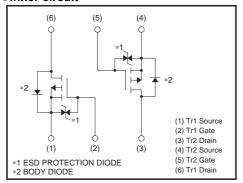
#### Packaging specifications

	Package	Taping
Type	Code	TN
	Basic ordering unit (pieces)	3000
UM6J1N		0

#### ●Dimensions (Unit: mm)



#### •Inner circuit



#### ●Absolute maximum ratings (Ta=25°C)

<It is the same ratings for Tr1 and Tr2.>

Parameter		Symbol	Limits	Unit
Drain-source voltage		V <sub>DSS</sub>	-30	V
Gate-source voltage		V <sub>GSS</sub>	±20	V
Drain current	Continuous	ID	±0.2	A
	Pulsed	IDP *1	±0.4	A
Total power dissipation		Pp *2	150	mW / TOTAL
		PD -	120	mW / ELEMENT
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	-55 to +150	°C

<sup>\*1</sup> Pw≤10μs, Duty cycle≤1%

#### ●Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a)*	833	°C/W / TOTAL
Charmer to ambient	Kill(Cli-a)	1042	°C/W / ELEMENT

<sup>\*</sup> Each terminal mounted on a recommended land

<sup>\*2</sup> Each terminal mounted on a recommended land

### ●Electrical characteristics (Ta=25°C)

<It is the same characteristics for Tr1 and Tr2.>

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	I <sub>GSS</sub>	-	-	±10	μА	V <sub>GS</sub> =±20V, V <sub>DS</sub> =0V
Drain-source breakdown voltage	V <sub>(BR)</sub> DSS	-30	-	_	V	I <sub>D</sub> = -1mA, V <sub>GS</sub> =0V
Zero gate voltage drain current	I <sub>DSS</sub>	_	-	-1	μΑ	V <sub>DS</sub> = -30V, V <sub>GS</sub> =0V
Gate threshold voltage	V <sub>GS (th)</sub>	-1.0	-	-2.5	V	V <sub>DS</sub> = -10V, I <sub>D</sub> = -1mA
Static drain-source on-state resistance	RDS (on)	_	0.9	1.4	Ω	I <sub>D</sub> = -0.2A, V <sub>G</sub> s= -10V
		_	1.4	2.1	Ω	I <sub>D</sub> = -0.15A, V <sub>G</sub> s= -4.5V
		_	1.6	2.4	Ω	I <sub>D</sub> = -0.15A, V <sub>G</sub> s= -4V
Forward transfer admittance	Y <sub>fs</sub>  *	0.2	-	-	S	V <sub>DS</sub> = -10V, I <sub>D</sub> = -0.15A
Input capacitance	Ciss	_	30	_	pF	V <sub>DS</sub> = -10V
Output capacitance	Coss	_	4	_	pF	V <sub>GS</sub> =0V
Reverse transfer capacitance	Crss	_	5	_	pF	f=1MHz
Turn-on delay time	t <sub>d (on)</sub> *	_	8	_	ns	Vpp≒ –15V
Rise time	tr *	-	5	-	ns	ID= -0.15A
Turn-off delay time	td (off)*	_	30	-	ns	Vgs= −10V RL≒ 100Ω
Fall time	t <sub>f</sub> *	_	40	_	ns	R <sub>G</sub> =10Ω

<sup>\*</sup> Pulsed

#### ●Body diode characteristics (source-drain)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward voltage	Vsp *	_	_	-1.2	V	Is= -0.1A, Vgs=0V

<sup>\*</sup>Pulsed

#### •Electrical characteristic curves

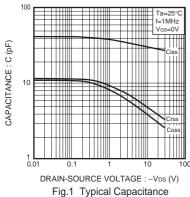


Fig.1 Typical Capacitance vs. Drain-Source Voltage

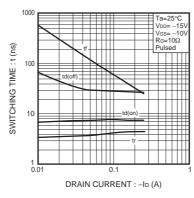


Fig.2 Switching Characteristics

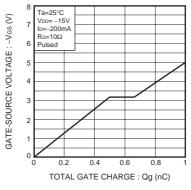


Fig.3 Dynamic Input Characteristics

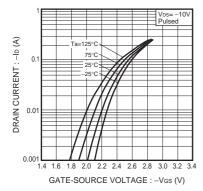


Fig.4 Typical Transfer Characteristics

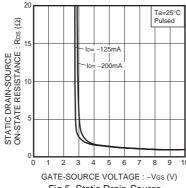
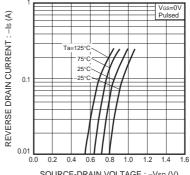


Fig.5 Static Drain-Source On-State Resistance vs. Gate-Source Voltage

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SOURCE-DRAIN VOLTAGE: -Vsd (V) Fig.6 Reverse Drain Current vs. Source-Drain Voltage

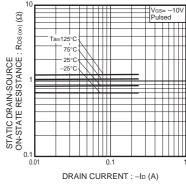


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current ( I )

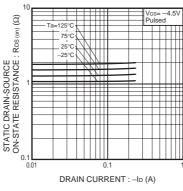


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current ( II )

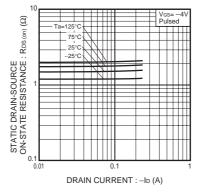


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current ( III )

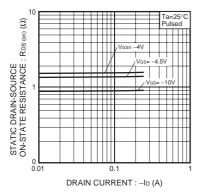


Fig.10 Static Drain-Source On-State Resistance vs. Drain Current ( IV)

#### Notice

This product might cause chip aging and breakdown under the large electrified environment. Please consider to design ESD protection circuit.

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