v00.0512

HMC1049

GaAs pHEMT MMIC LOW NOISE AMPLIFIER, 0.3 - 20 GHz

Typical Applications

This HMC1049 is ideal for:

- Point-to-Point Radios
- Point-to-Multi-Point Radios
- Military & Space
- Test Instrumentation

Features

Low Noise Figure: 1.7 dB

High Gain: 16 dB

P1dB Output Power: 15 dBm

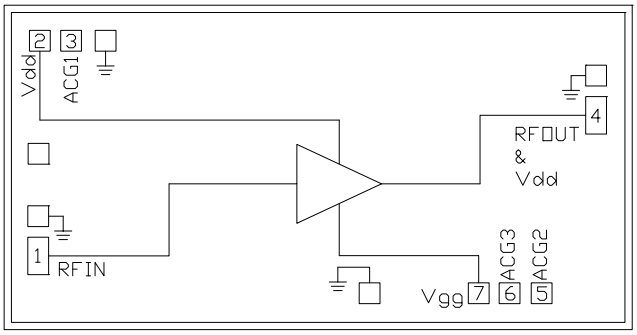
Supply Voltage: +7 V @ 70 mA

Output IP3: 27 dBm

50 Ohm matched Input/Output

Die Size: 1.43 x 2.9 x 0.1 mm

Functional Diagram



General Description

The HMC1049 is a GaAs MMIC Low Noise Amplifier which operates between 0.3 and 20 GHz. This LNA provides 16 dB of small signal gain, 1.7 dB noise figure, and output IP3 of 27 dBm, while requiring only 70 mA from a +7 V supply. The P1dB output power of 16 dBm enables the LNA to function as a LO driver for balanced, I/Q or image reject mixers. Vdd can be applied to pad 2 or pad 4. Pad 4 will require a bias tee. The HMC1049 also is internally matched to 50 Ohms for ease of integration into multi-chip-modules (MCMs). All data is taken with the chip in a 50 Ohm test fixture connected via 0.025 mm (1 mil) diameter wire bonds of 0.31 mm (12 mils) length.

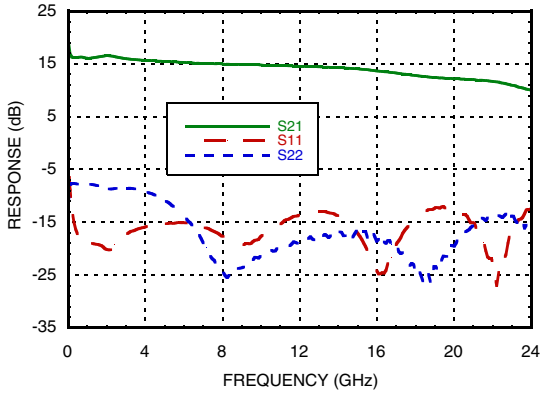
Electrical Specifications, T_A = +25° C, Vdd = +7V, Idd = 70 mA [1]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		0.3 - 10			10 - 16			16 - 20		GHz
Gain	12.5	16		12	14.5		11	13		dB
Gain Variation over Temperature		0.012			0.016			0.015		dB / °C
Noise Figure		1.7	2.4		2	2.7		2.7	3.6	dB
Input Return Loss		17			14			14		dB
Output Return Loss		12			17			17		dB
Output Power for 1 dB Compression		15			13			12		dBm
Saturated Output Power (Psat)		18			16.5			15.5		dBm
Output Third Order Intercept (IP3)		27			25			23.5		dBm
Supply Current (Idd) (Vdd = 7V)		70			70			70		mA

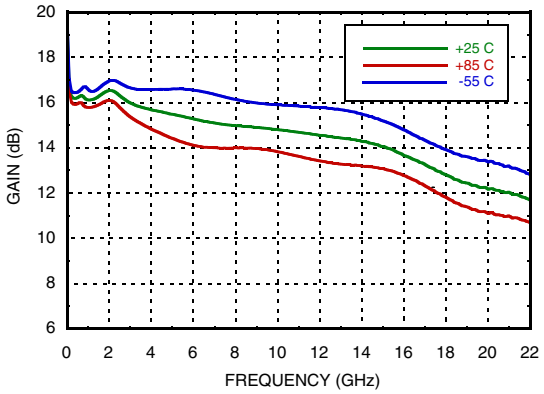
[1] Adjust Vgg to achieve Idd= 70 mA

Data taken with Vdd applied to pad 2.

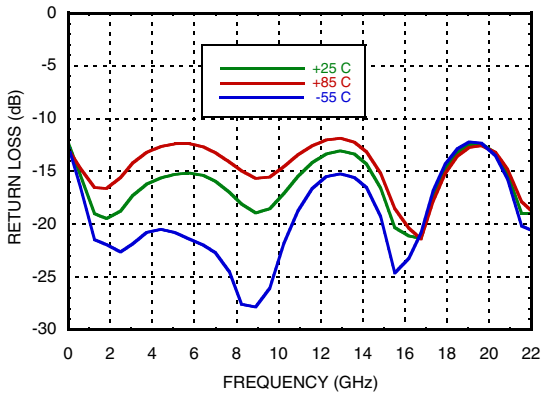
Broadband Gain & Return Loss [1]



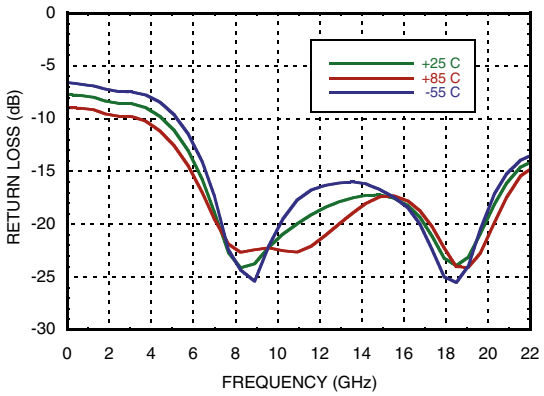
Gain vs. Temperature



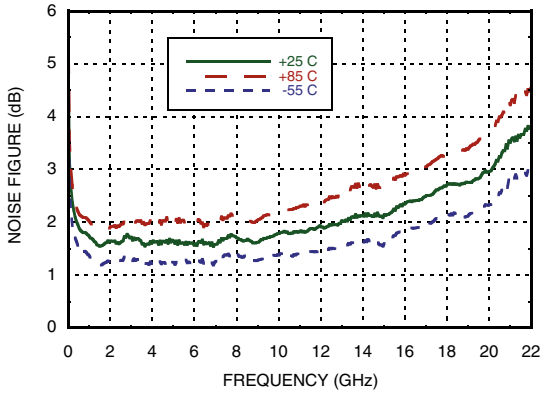
Input Return Loss vs. Temperature



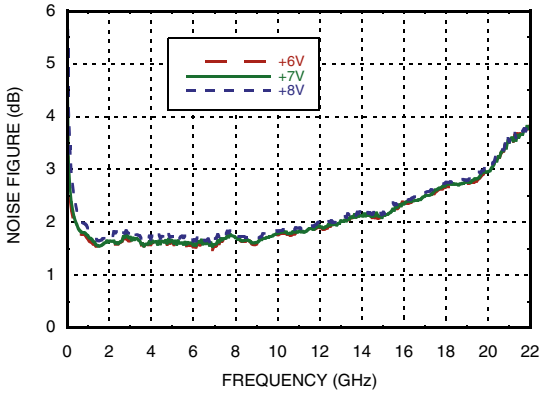
Output Return Loss vs. Temperature



Noise Figure vs. Temperature

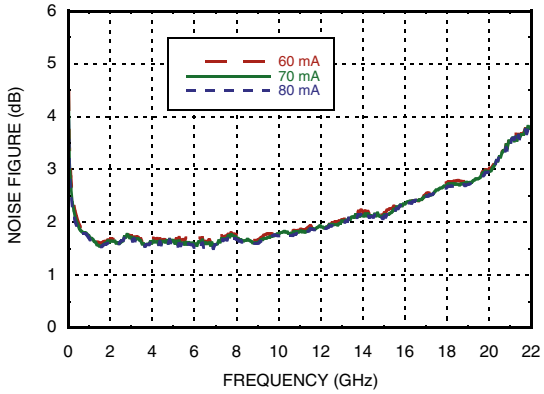


Noise Figure vs. Vdd

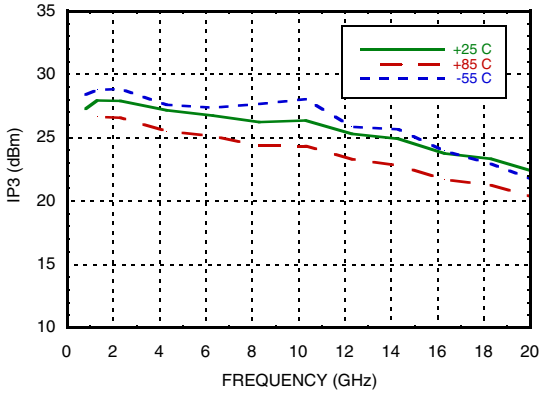


Data taken with Vdd applied to pad 2.

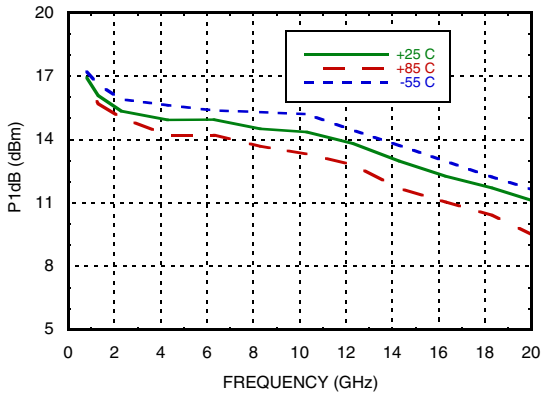
Noise Figure vs. Idd



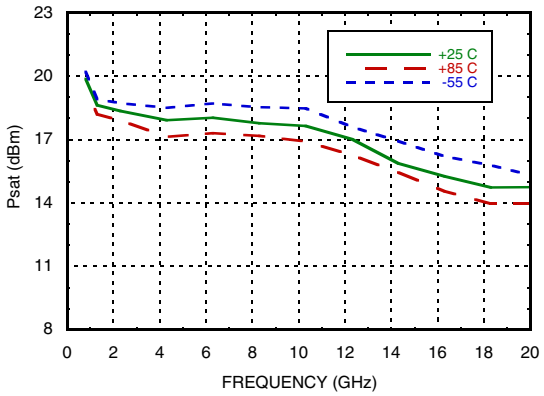
Output IP3 vs. Temperature



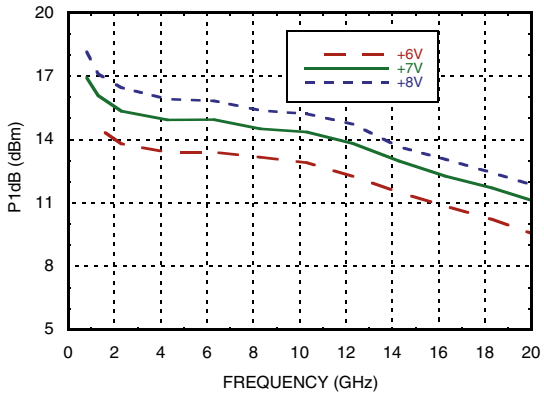
P1dB vs. Temperature



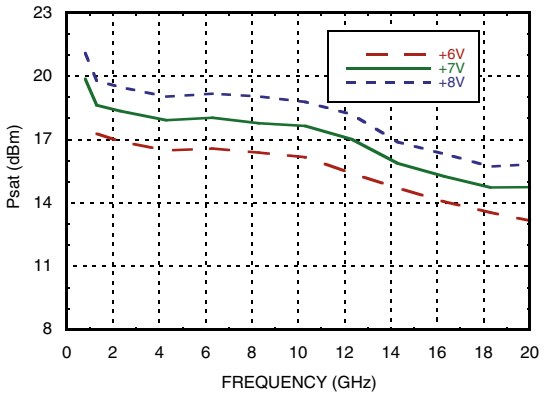
Psat vs. Temperature



P1dB vs. Vdd

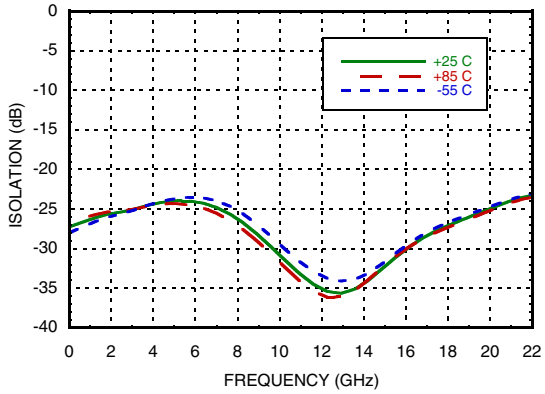


Psat vs. Vdd

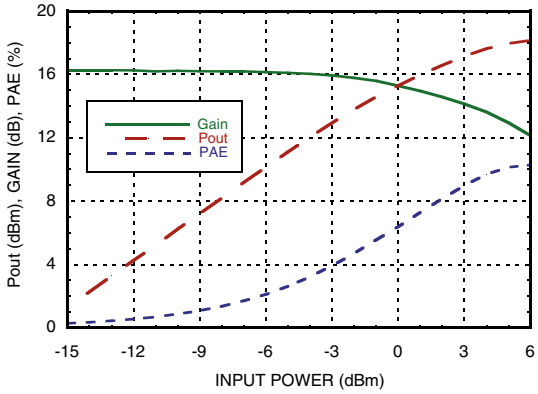


Data taken with Vdd applied to pad 2.

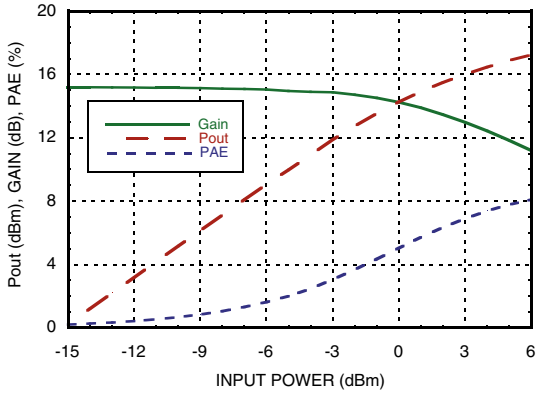
Reverse Isolation vs. Temperature



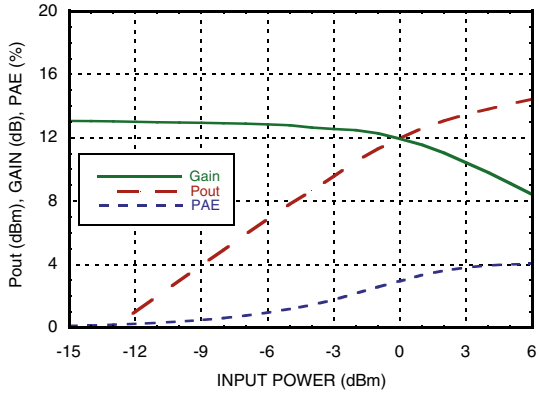
Power Compression @ 2 GHz



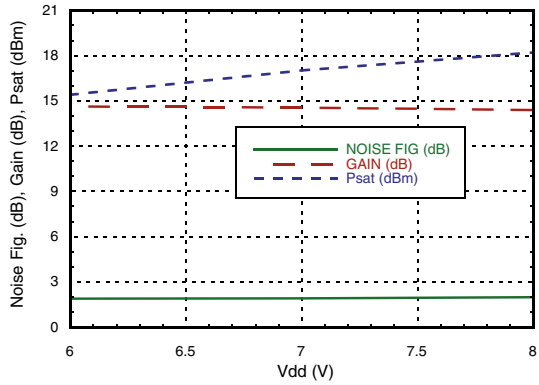
Power Compression @ 10 GHz



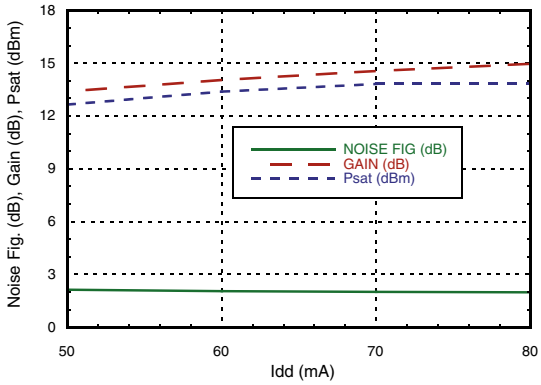
Power Compression @ 18 GHz



Noise Figure, Gain & Power vs. Supply Voltage @ 12 GHz

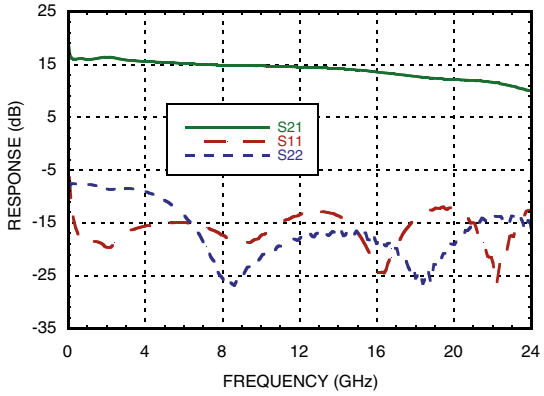


Noise Figure, Gain & Power vs. Supply Current @ 12 GHz

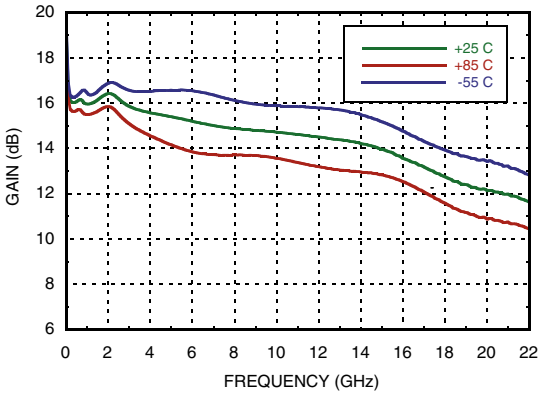


Data taken with Vdd applied to bias tee at pad 4.

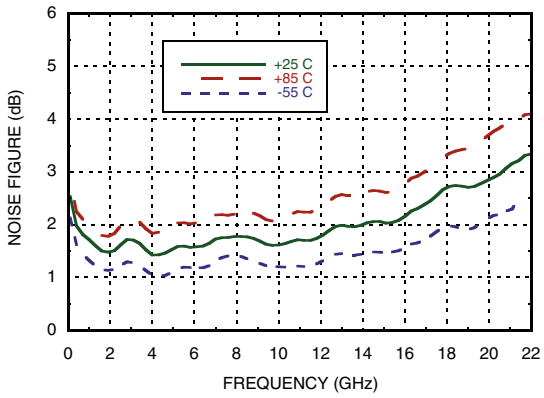
Broadband Gain & Return Loss [1]



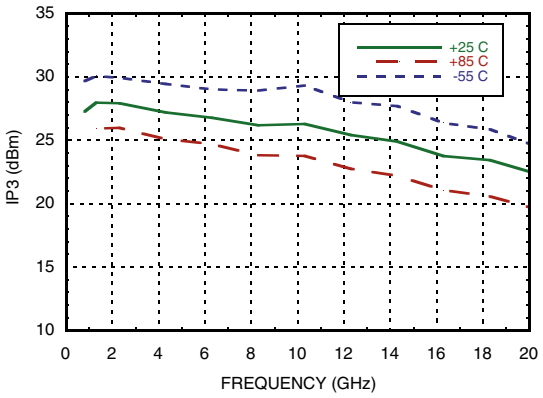
Gain vs. Temperature [1]



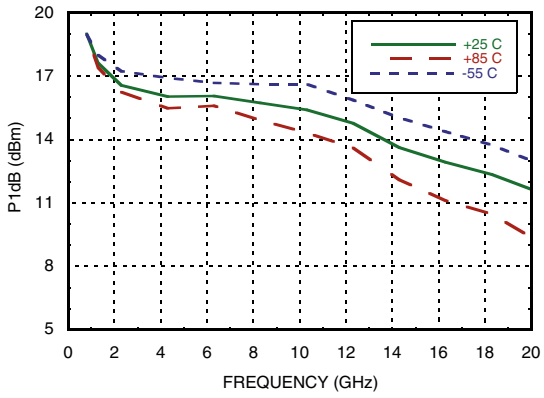
Noise Figure vs. Temperature [1]



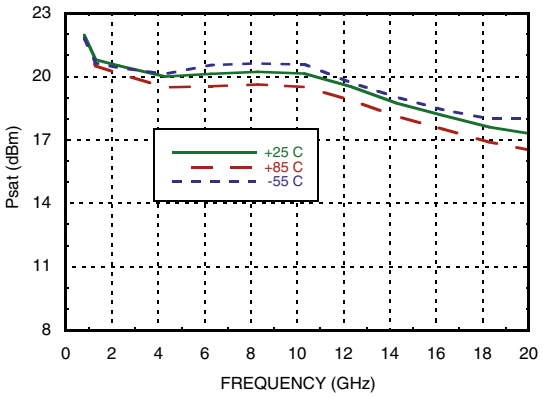
Output IP3 vs. Temperature [1]



P1dB vs. Temperature [1]



Psat vs. Temperature [1]



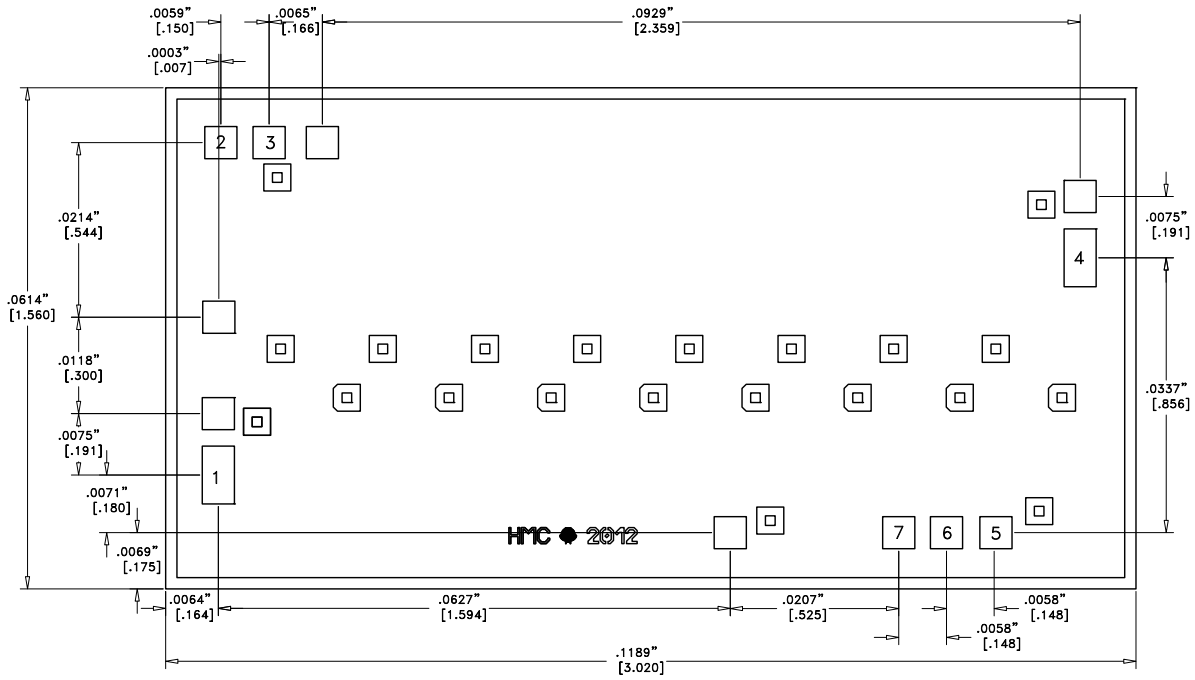
[1] Vdd= 4V, supply to bias tee.

Absolute Maximum Ratings

Drain Bias Voltage (Vdd)	+10V
Drain Bias Voltage (RF out / Vdd)	+7V
RF Input Power	+18 dBm
Gate Bias Voltage, Vgg1	-2V to +0.2V
Channel Temperature	175 °C
Continuous Pdiss (T = 85 °C) (derate 37.4 mW/°C above 85 °C)	3.4 W
Thermal Resistance (Channel to die bottom)	26.7 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



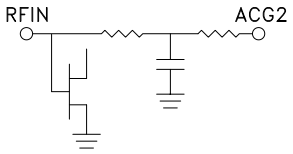
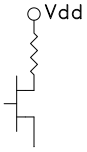
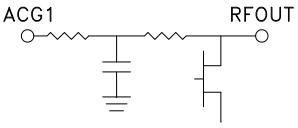
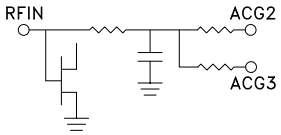
NOTES:
1. ALL DIMENSIONS IN INCHES [MILLIMETERS]
2. DIE THICKNESS IS 0.004 (0.100)
3. TYPICAL BOND PAD IS 0.004 (0.100) SQUARE
4. BOND PAD METALIZATION: GOLD
5. BACKSIDE METALLIZATION: GOLD
6. BACKSIDE METAL IS GROUND
7. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
8. OVERALL DIE SIZE IS ±.002

Die Packaging Information [1]

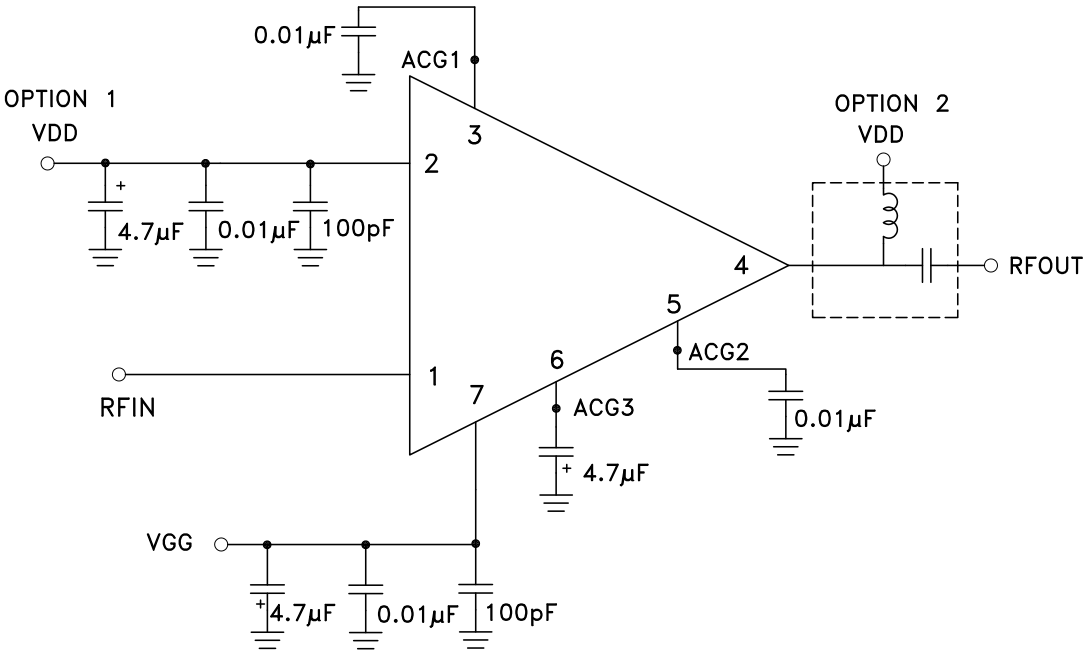
Standard	Alternate
GP-1(Gel Pack)	[2]

[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] For alternate packaging information contact Hittite Microwave Corporation.

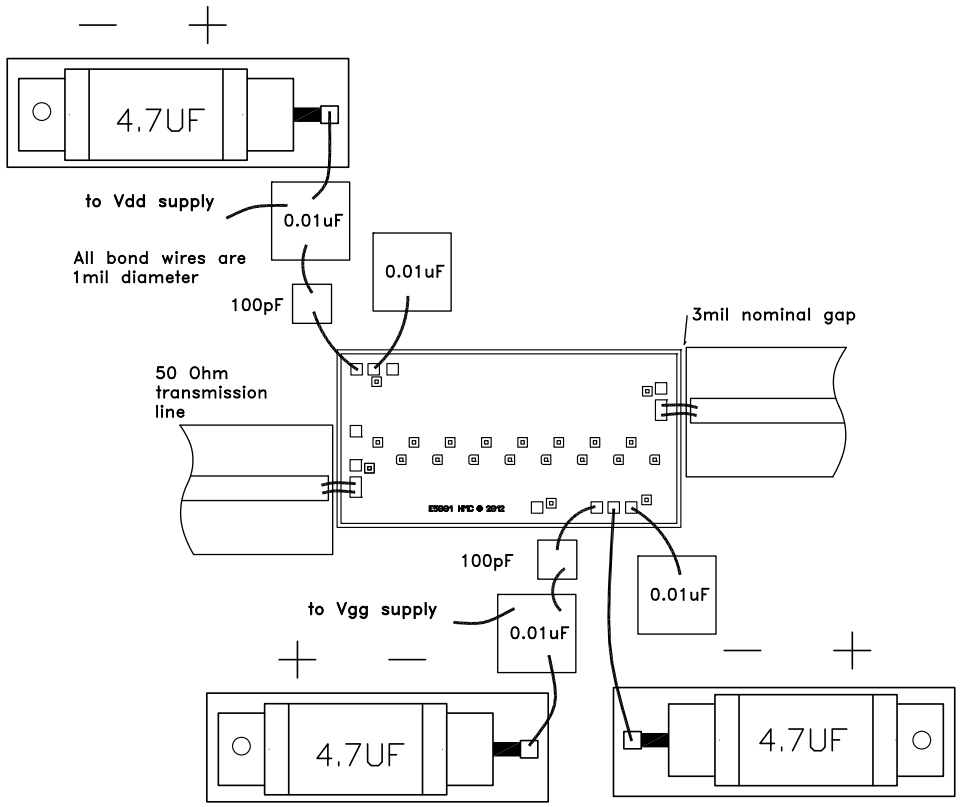
Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1	RFIN	This pin is DC coupled and matched to 50 Ohms	
2	Vdd	Power supply voltage for the amplifier. External bypass capacitors are required.	
3	ACG1	Low frequency termination. Attach bypass capacitor per application circuit herein.	
4	RFOUT	This pin is DC coupled and matched to 50 Ohms	
5, 6	ACG2, ACG3	Low frequency termination. Attach bypass capacitor per application circuit herein.	
7	Vgg	Gate control for amplifier. Adjust to achieve Idd= 70 mA.	
Die Bottom	GND	Die bottom must be connected to RF/DC ground.	

Application Circuit



Assembly Diagram



Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should be placed as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm to 0.152 mm (3 to 6 mils).

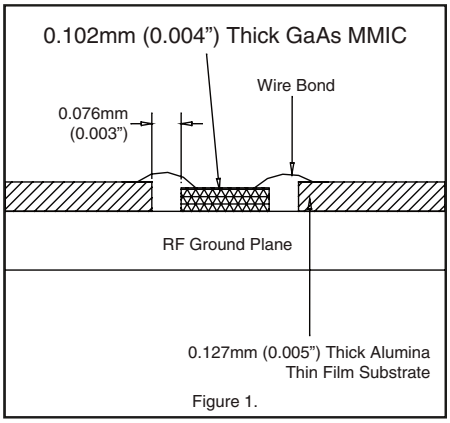


Figure 1.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

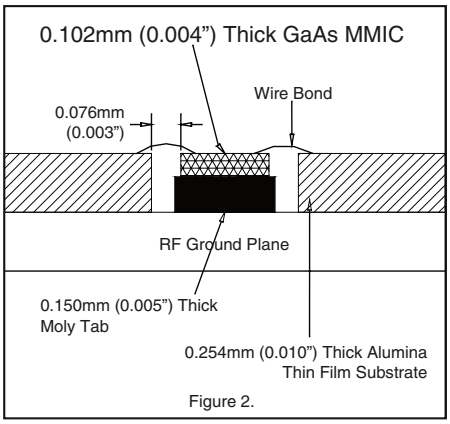


Figure 2.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

RF bonds made with two 1 mil wires are recommended. These bonds should be thermosonically bonded with a force of 40-60 grams. DC bonds of 0.001" (0.025 mm) diameter, thermosonically bonded, are recommended. Ball bonds should be made with a force of 40-50 grams and wedge bonds at 18-22 grams. All bonds should be made with a nominal stage temperature of 150 °C. A minimum amount of ultrasonic energy should be applied to achieve reliable bonds. All bonds should be as short as possible, less than 12 mils (0.31 mm)

Notes: