HMC381LP6 / 381LP6E

HIGH IP3 RFIC DUAL DOWNCONVERTER, 1.7 - 2.7 GHz

Typical Applications

The HMC381LP6 / HMC381LP6E is ideal for Wireless Infrastructure Applications:

- GSM, GPRS & EDGE
- CDMA & W-CDMA
- PHS & PDC
- WiMAX

Features

Input IP3: +27 dBm

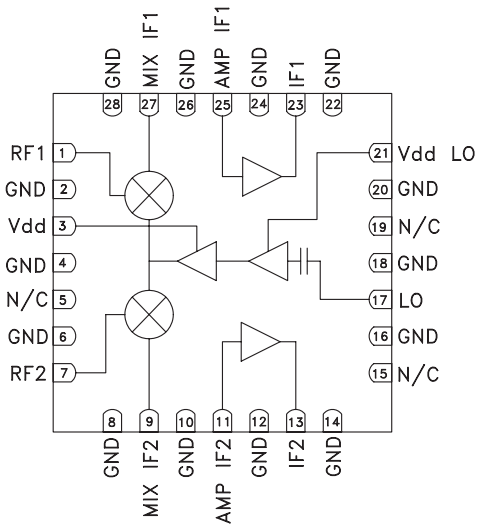
Low Single Input LO Drive: 0 dBm

Conversion Gain: 9 dB

Noise Figure: 12 dB

Single Positive Supply: +5V @ 260 mA

Functional Diagram



General Description

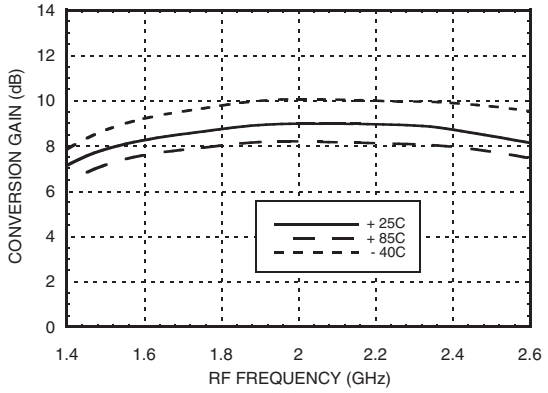
The HMC381LP6 & HMC381LP6E are high linearity Dual Down Converter Receiver ICs that operate from 1.7 - 2.7 GHz and deliver a +27 dBm input third order intercept point for UMTS, PHS and WiMAX applications. The passive mixer outputs and high dynamic range IF amplifier inputs are positioned so that an external IF filter can be placed in series between them. The converter provides a gain of 9 dB and 12 dB typical single side band noise figure. The IC operates from a positive +5V rail consuming 260 mA of current while requiring a LO drive level of only -4 to +4 dBm. The design requires no external baluns and supports IF frequencies between 50 and 300 MHz.

Electrical Specifications, T_A = +25° C, LO = 0 dBm, Vdd = 5V

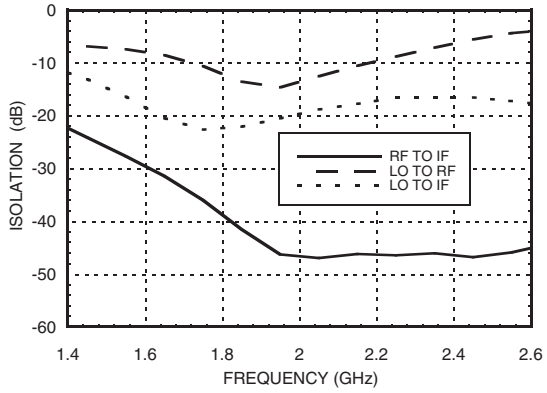
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range, RF	1.7 - 2.0			2.0 - 2.2			2.5 - 2.7			GHz
Frequency Range, LO	1.4 - 2.3			1.7 - 2.5			2.2 - 2.6			GHz
Frequency Range, IF	50 - 300 [1]			50 - 300 [1]			50 - 300 [2]			MHz
Conversion Gain	6.5	8.5		7	9		7	9		dB
Noise Figure (SSB)		12			12.5					dB
LO to RF Isolation		11			11			5		dB
LO to IF Isolation	16	20		14	18		13	18		dB
RF to IF Isolation	30	40		40	46		32	37		dB
IP3 (Input)	23	26		24	27		23	26		dBm
1 dB Compression (Input)		12			12			10		dBm
Branch Isolation		50			52			50		dB
LO Drive Input Level (Typical)	-4 to +4									dBm
Supply Current (Idd for LO & IF) (IF bias resistor= 4.7 Ohms)		260	330		260	330		260	330	mA

[1] Unless otherwise noted all measurements with low side LO & IF = 250 MHz.
[2] Unless otherwise noted all measurements with low side LO & IF = 156 MHz.

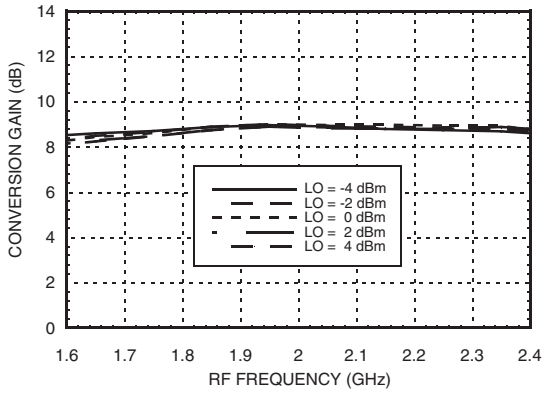
Conversion Gain vs. Temperature @ LO = 0 dBm



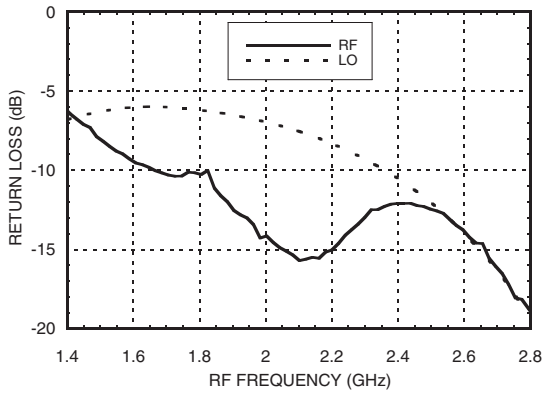
Isolation @ LO = 0 dBm



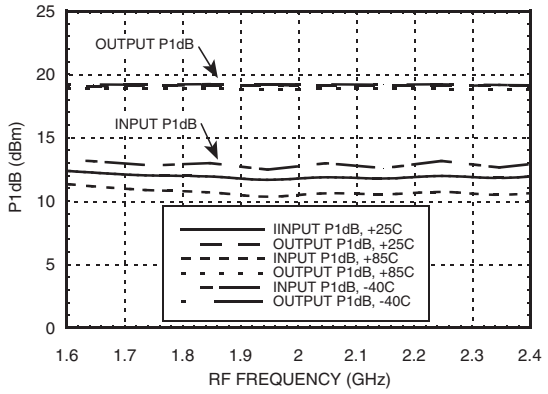
Conversion Gain vs. LO Drive



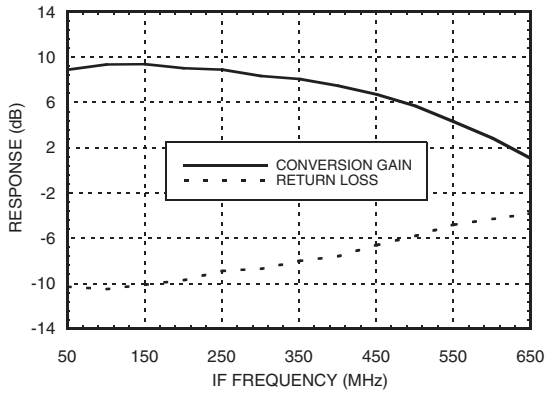
Return Loss @ LO = 0 dBm



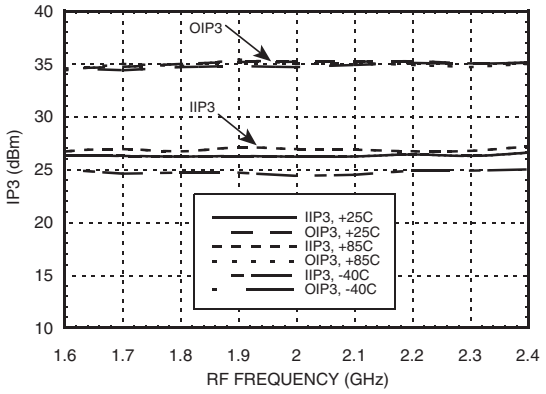
P1dB vs. Temperature @ LO = 0 dBm



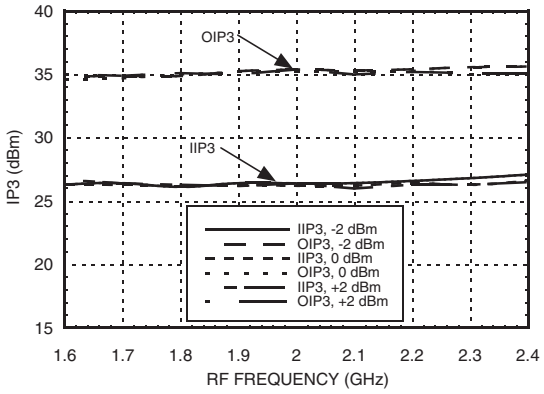
IF Bandwidth @ LO = -5 dBm



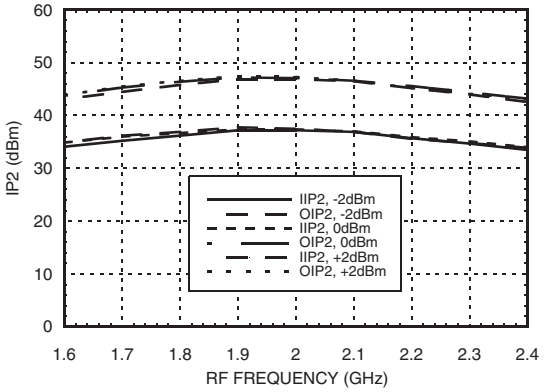
Input and Output IP3 vs. Temperature @ LO = 0 dBm



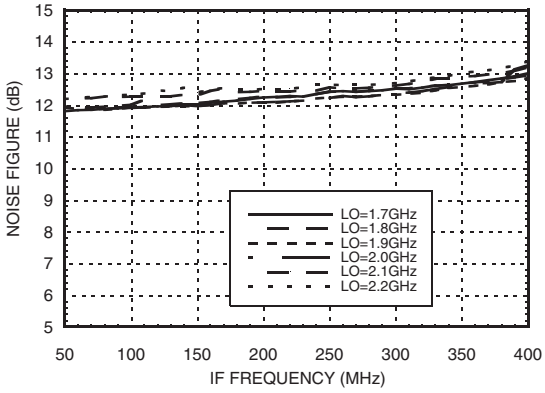
Input and Output IP3 vs LO Drive



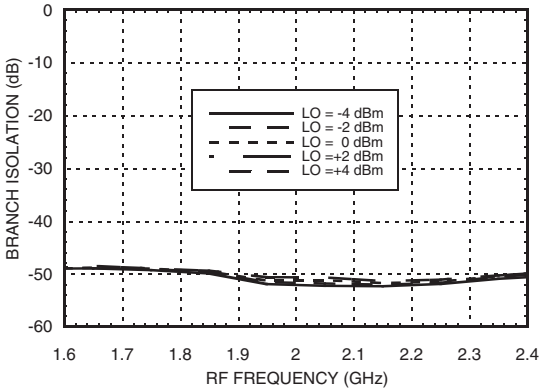
Input and Output IP2 vs. LO Drive



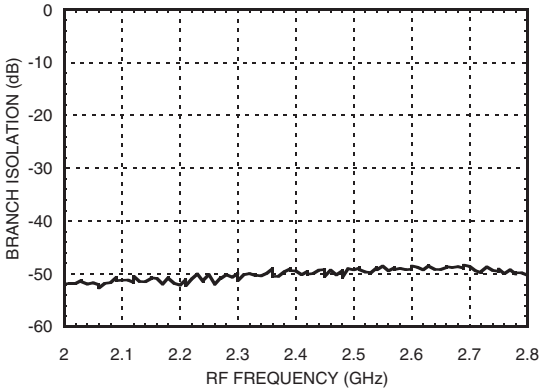
Noise Figure vs. IF Frequency



Branch Isolation RF1 - IF2 vs. LO Drive IF = 250 MHz

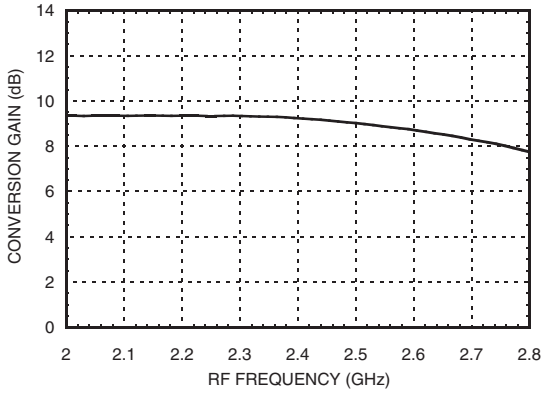


Branch Isolation RF1 - IF2 LO = 0 dBm, IF = 156 MHz

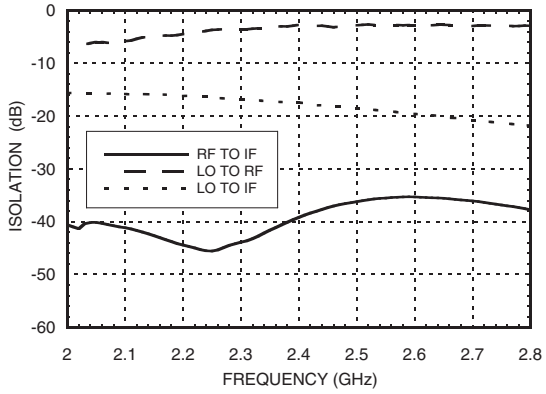


Reference to output of standard path

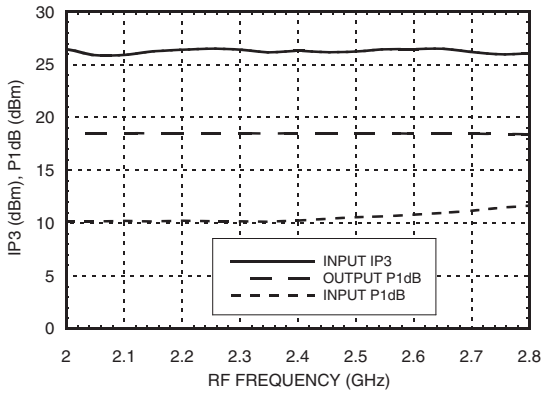
Conversion Gain @ LO = 0 dBm IF = 156 MHz



Isolation @ LO = 0 dBm, IF = 156 MHz



Input IP3 & Input P1dB @ LO = 0 dBm, IF = 156 MHz



MxN Spurious @ IF Port

	nLO				
mRF	0	1	2	3	4
0	xx	21	52	40	48
1	54	0	57	82	88
2	95	79	53	84	94
3	94	94	95	72	95
4	94	95	94	95	95

RF Freq. = 1.9 GHz @ -10 dBm
LO Freq. = 1.65 GHz @ 0 dBm
All values in dBc relative to the IF power level.

Harmonics of LO

	nLO Spur @ RF Port			
LO Freq. (GHz)	1	2	3	4
1.4	8	12	15	19
1.5	9	13	16	21
1.6	11	14	17	24
1.7	13	15	18	29
1.8	12	13	19	29
1.9	11	12	19	28

LO = 0 dBm
All values in dBc below input LO level measured at RF port.

HMC381LP6 / 381LP6E

HIGH IP3 RFIC DUAL DOWNCONVERTER, 1.7 - 2.7 GHz

Absolute Maximum Ratings

RF / IF Input (Vdd= +5V)	+13 dBm
LO Drive (Vdd= +5V)	+15 dBm
Vdd (LO or IF)	+7 Vdc
Channel Temperature	150°C
Continuous Pdiss (T = 85°C) (derate 25.5 mW/°C above 85°C)	1.64 W
Thermal Resistance (junction to ground paddle)	39.6 °C/W
Storage Temperature	-65 to +150°C
Operating Temperature	-40 to +85°C
ESD Sensitivity (HBM)	Class 1A

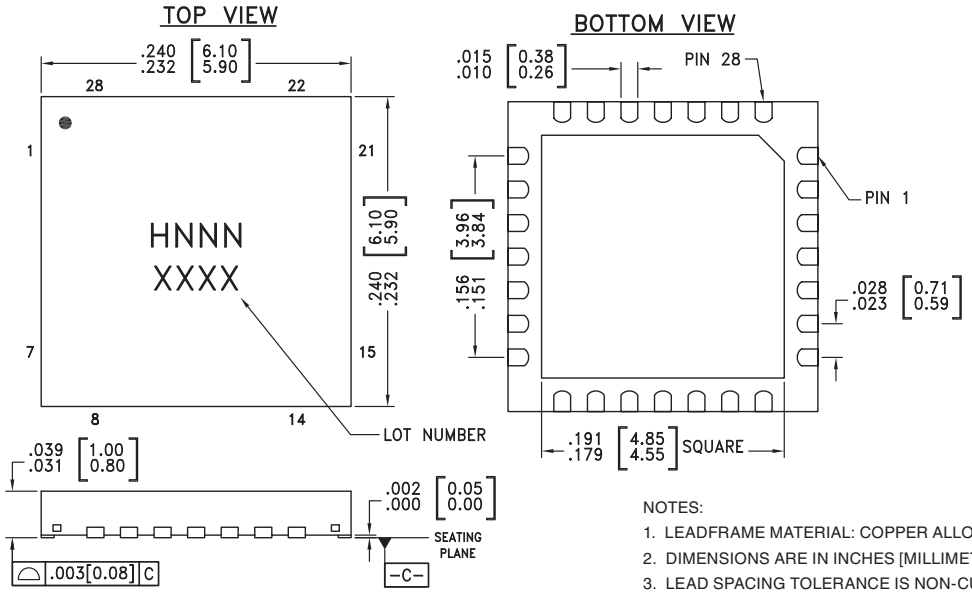
Typical Supply Current vs. Vdd

Vdd (LO + IF)	Idd (mA)
+4.5	190
+5.0	260
+5.5	340

Downconverter will operate over full voltage range shown above.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

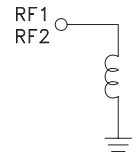
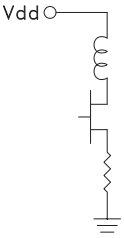
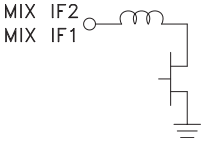
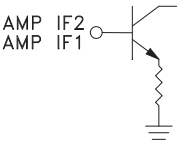
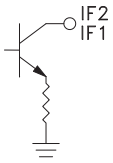
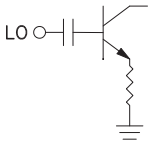
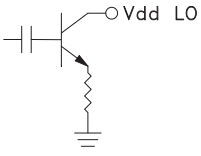
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

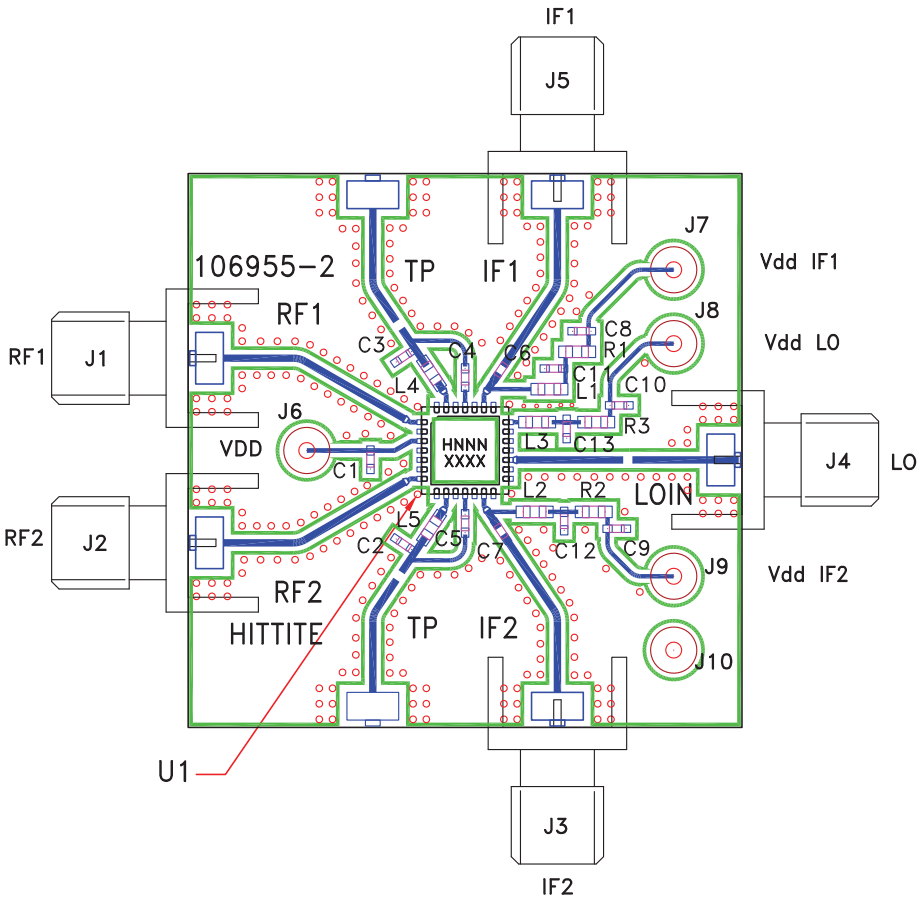
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC381LP6	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H381 XXXX
HMC381LP6E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H381 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 7	RF1, RF2	These pins are DC coupled and matched to 50 Ohms.	
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28	GND	Backside of package has exposed metal ground slug that must also be connected to ground.	
3	Vdd	Power supply for the second stage LO amplifier. One external bypass capacitor (1,000 pF) is required.	
5, 15, 19	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	
9, 27	MIX IF2, MIX IF1	IF output from the mixers. This pin is DC coupled to the mixer. A low pass filter and blocking capacitor are required between mixer IF port and IF amplifier. (See application circuit).	
11, 25	AMP IF2, AMP IF1	Inputs to the IF amplifiers. A low pass filter and blocking capacitor are required between mixer IF port and IF amplifier. (See application circuit).	
13, 23	IF2, IF1	Outputs of the IF amplifiers and bias ports for the IF amplifiers. A pull up inductor, resistor, and bypass capacitors are required. (See application circuit).	
17	LO	These pins are AC coupled and matched to 50 Ohms.	
21	Vdd LO	Bias voltage for the first stage of the LO amplifier. A pull up inductor, resistor, and bypass capacitors are required. (See application circuit).	

Evaluation PCB



List of Materials for Evaluation PCB 106971 [1]

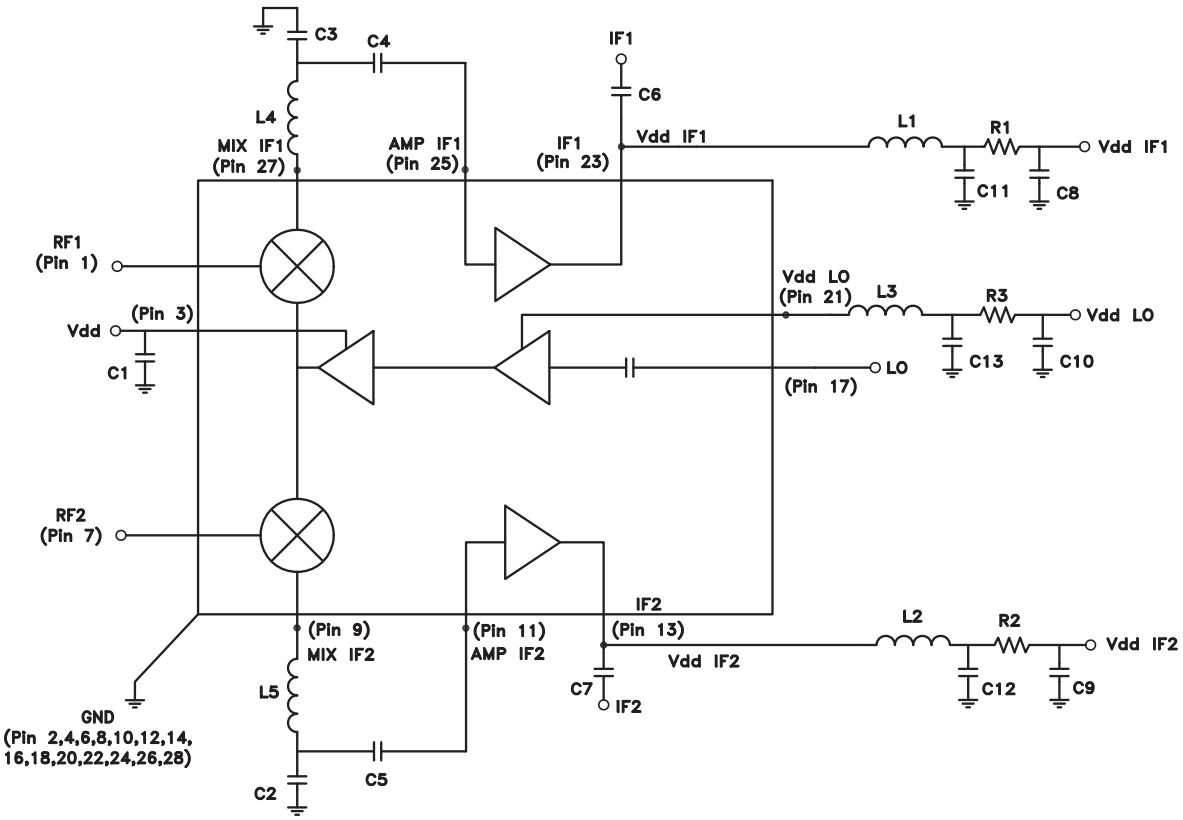
Item	Description
J1 - J5	PCB Mount SMA RF Connector
J6 - J10	DC Pins
C1, C4 - C10	1000 pF Chip Capacitor, 0402 Pkg.
C2, C3	7 pF Chip Capacitor, 0402 Pkg.
C11, C12, C13	100 pF Chip Capacitor, 0402 Pkg.
L1, L2	220 nH Chip Inductor, 0603 Pkg.
L3	22 nH Chip Inductor, 0603 Pkg.
L4, L5	27 nH Chip Inductor, 0603 Pkg.
R1, R2	4.7 Ohm Resistor, 0603 Pkg.
R3	22 Ohm Resistor, 0603 Pkg.
U1	HMC381LP6 / HMC381LP6E
PCB [2]	106955 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit



Recommended Components Values (IF = DC - 300 MHz)	
C1, C4 - C10	1000 pF
C2, C3	7 pF
C11, C12, C13	100 pF
L1, L2	220 nH
L3	22 nH
L4, L5	27 nH
R1, R2	4.7 Ohm
R3	22 Ohm

Note: L4, C3 and L5, C2 form low pass filters. C4 and C5 are DC blocks.