HMC424LH5

v02.0909

0.5dB LSB GaAs MMIC 6-BIT DIGITAL ATTENUATOR, DC - 13 GHz

Typical Applications

The HMC424LH5 is ideal for:

- Telecom Infrastructure
- Military Radio, Radar & ECM
- Space Systems
- Test Instrumentation

Features

0.5 dB LSB Steps to 31.5 dB

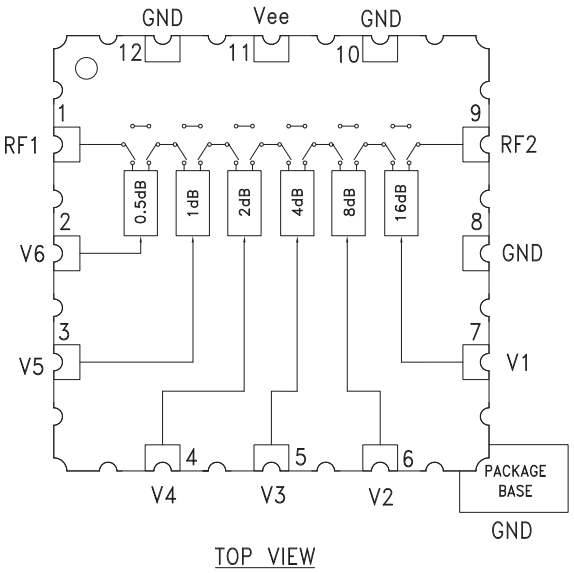
Single Control Line Per Bit

± 0.3 dB Typical Bit Error

Hermetic SMT Package, 25mm²

Screening to MIL-PRF-38535 (Class B or S) Available

Functional Diagram



TOP VIEW

General Description

The HMC424LH5 is a broadband 6-bit GaAs MMIC digital attenuator housed in a hermetic SMT leadless package. Covering DC to 13 GHz, the insertion loss is less than 3.5 dB typical. The attenuator bit values are 0.5 (LSB), 1, 2, 4, 8, and 16 dB for a total attenuation of 31.5 dB. Attenuation accuracy is excellent at ±0.5 dB typical step error with an IIP3 of +32 dBm. Six control voltage inputs, toggled between 0 and -5V, are used to select each attenuation state. A single Vee bias of -5V allows operation at frequencies down to DC. The HMC424LH5 is compatible with standard and lead free surface mount manufacturing techniques and is suitable for high reliability military, industrial and space applications.

Electrical Specifications, T_A = +25° C, With Vee = -5V & VCTL= 0/-5V

Parameter		Frequency (GHz)	Min.	Typ.	Max.	Units
Insertion Loss		DC - 4 GHz 4.0 - 8.0 GHz 8.0 - 13.0 GHz		2.7 3.3 4.2	3.2 3.8 4.7	dB dB dB
Attenuation Range		DC - 13.0 GHz		31.5		dB
Return Loss (RF1 & RF2, All Atten. States)		DC - 13.0 GHz		12		dB
Attenuation Accuracy: (Referenced to Insertion Loss)						
	0.5 - 16.5 dB States	DC - 13.0 GHz	± 0.4 + 4% of Atten. Setting Max			dB
	17 - 31.5 dB States	DC - 13.0 GHz	± 0.5 + 5% of Atten. Setting Max			dB
Input Power for 0.1 dB Compression		1.0 - 13.0 GHz		22		dBm
Input Third Order Intercept Point	REF State	1.0 - 13.0 GHz		46		dBm
(Two-Tone Input Power= 0 dBm Each Tone)	All Other States			32		dBm
Switching Characteristics		DC - 13.0 GHz				
tRISE, tFALL (10/90% RF)				30		ns
tON/tOFF (50% CTL to 10/90% RF)				50		ns

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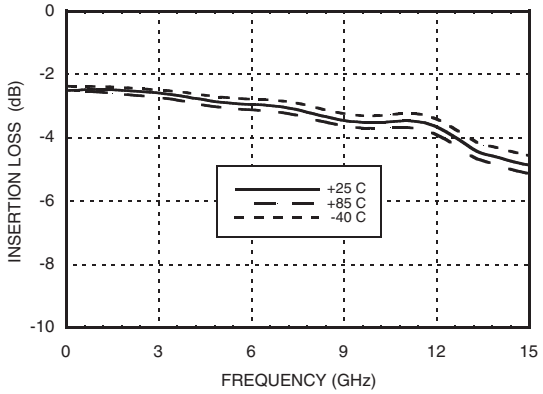
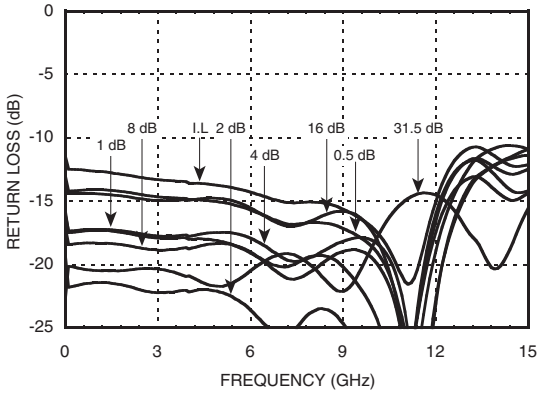
Insertion Loss



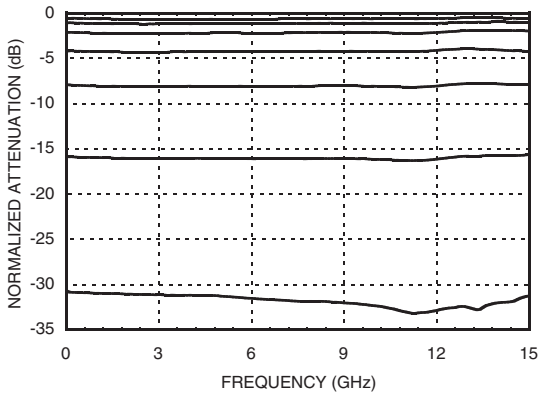
Return Loss RF1, RF2

(Only Major States are Shown)

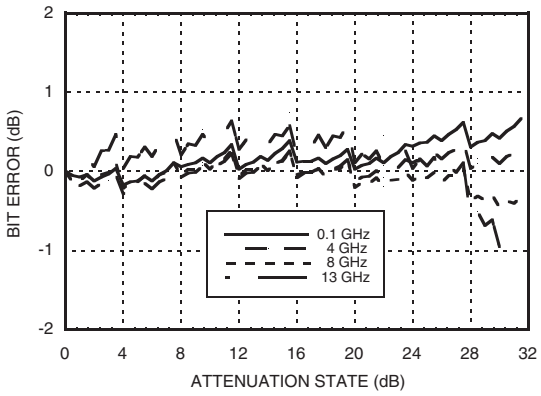


Normalized Attenuation

(Only Major States are Shown)

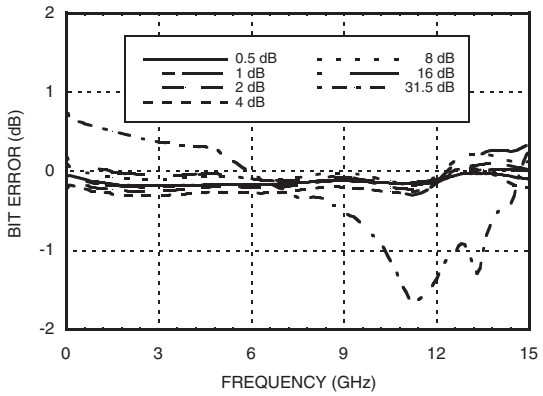


Bit Error vs. Attenuation State



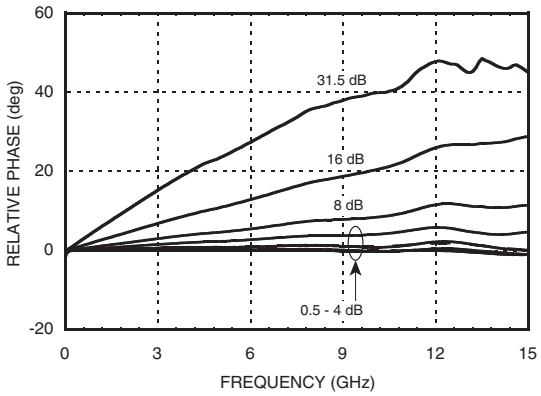
Bit Error vs. Frequency

(Only Major States are Shown)

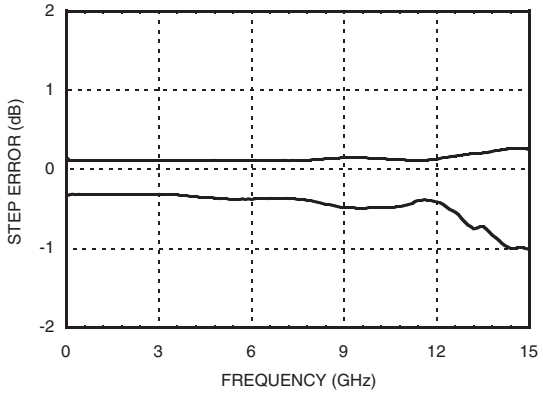


Relative Phase vs. Frequency

(Only Major States are Shown)



Worst Case Step Error Between Successive Attenuation States



Bias Voltage & Current

Vee Range= -5 Vdc ± 10%		
Vee (VDC)	Iee (Typ.) (mA)	Iee (Max.) (mA)
-5.0	3	5

Control Voltage

State	Bias Condition
Low	0 to -3V @ 35 µA Typ.
High	Vee to Vee +0.8V @ 5 µA Typ.

Truth Table

Control Voltage Input						Attenuation State RF1 - RF2
V1 16 dB	V2 8 dB	V3 4 dB	V4 2 dB	V5 1 dB	V6 0.5 dB	
Low	Low	Low	Low	Low	Low	Reference I.L.
Low	Low	Low	Low	Low	High	0.5 dB
Low	Low	Low	Low	High	Low	1 dB
Low	Low	Low	High	Low	Low	2 dB
Low	Low	High	Low	Low	Low	4 dB
Low	High	Low	Low	Low	Low	8 dB
High	Low	Low	Low	Low	Low	16 dB
High	High	High	High	High	High	31.5 dB

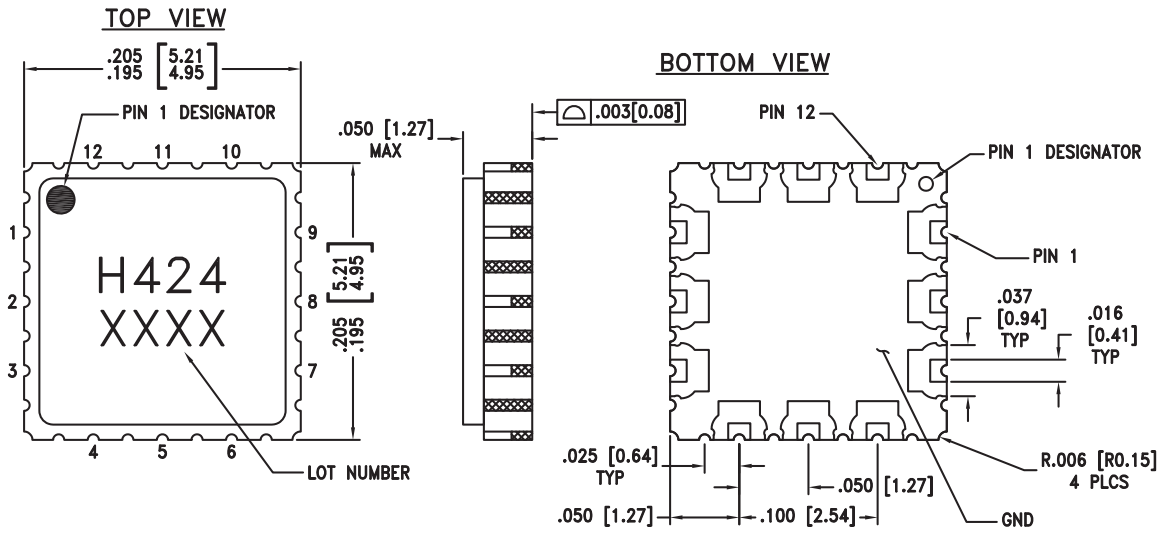
Any Combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.

Absolute Maximum Ratings

Control Voltage (V1 to V6)	Vee - 0.5 Vdc
Bias Voltage (Vee)	-7 Vdc
Channel Temperature	150 °C
Thermal Resistance	344 °C/W
Continuous Pdiss (T= 85 °C) (derate 2.9 mW/ °C above 85 °C)	0.18 W
Storage Temperature	-65 to + 150 °C
Operating Temperature	-40 to +85 °C
RF Input Power (0.5 - 13 GHz)	+25 dBm

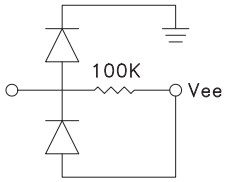
ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing

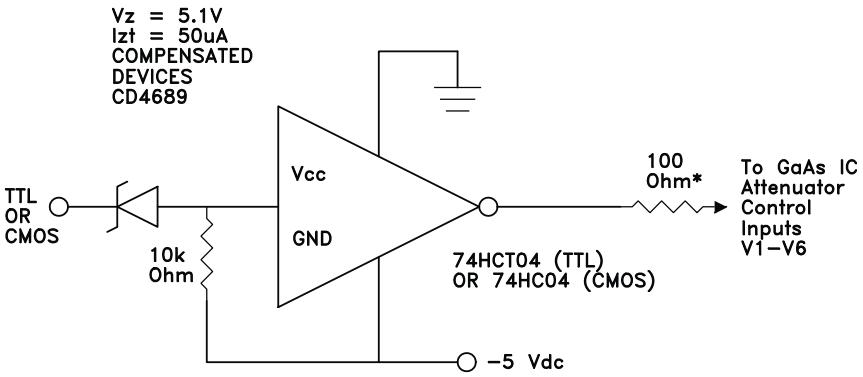


NOTES:
1. PACKAGE BODY MATERIAL: CERAMIC & KOVAR
2. LEAD AND GROUND PADDLE PLATING: GOLD 40 - 80 MICROINCHES.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PAD BURR LENGTH 0.15mm MAX.
   PAD BURR HEIGHT 0.25mm MAX.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.

Pin Description

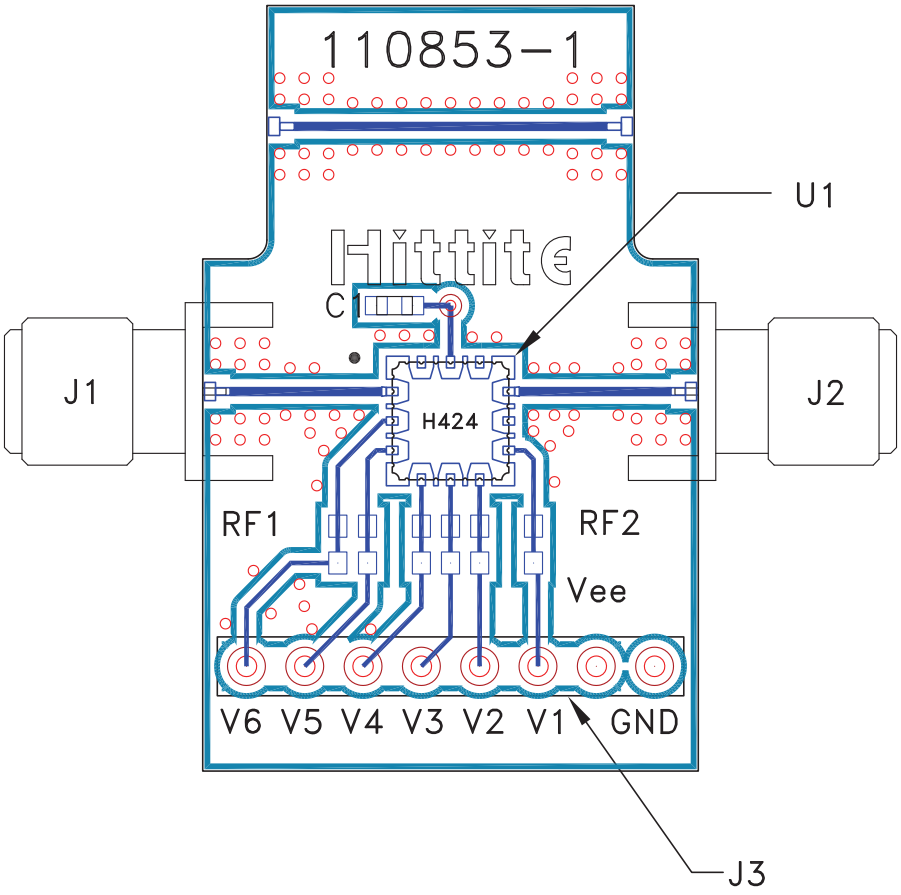
Pad Number	Function	Description	Interface Schematic
1, 9	RF1, RF2	This pin is DC coupled and matched to 50 Ohm. Blocking capacitors are required if RF line potential is not equal to 0V.	
2 - 7	V6 - V1	See truth table and control voltage table.	
8, 10, 12	GND	Package base must also be connected to RF ground	
11	Vee	Supply Voltage -5V ± 10%	

Suggested Driver Circuit *(One Circuit Required Per Bit Control Input)*



Simple driver using inexpensive standard logic ICs provides fast switching using minimum DC current.
** Recommended value to suppress unwanted RF signals at V1 - V6 control lines.*

Evaluation PCB



List of Materials for Evaluation PCB 110855 [1]

Item	Description
J1 - J2	PCB Mount SMA SRI Connector
J3	8 Pin DC Connector .1" Thruhole
C1	0.01 µF Capacitor, 0603 Pkg.
U1	HMC424LH5 Digital Attenuator
PCB [2]	110853 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.