HMC464LP5 / 464LP5E

GaAs PHEMT MMIC POWER AMPLIFIER, 2 - 20 GHz

Typical Applications

The HMC464LP5 / HMC464LP5E is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military EW, ECM & C³I
- Test Instrumentation
- Fiber Optics

Features

P1dB Output Power: +26 dBm

Gain: 14 dB

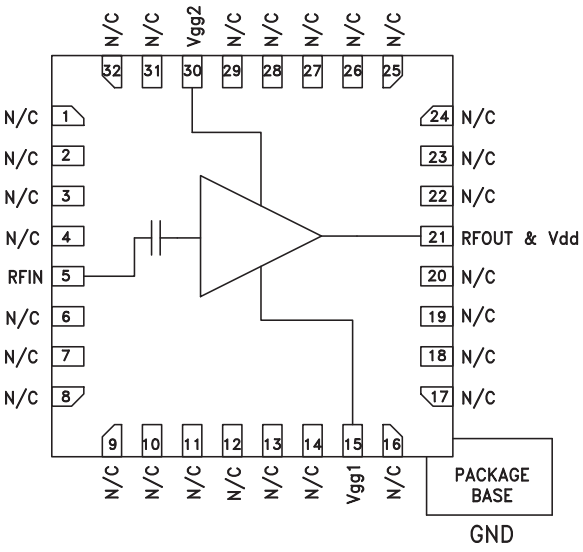
Output IP3: +30 dBm

Supply Voltage: +8V @ 290 mA

50 Ohm Matched Input/Output

25 mm² Leadless SMT Package

Functional Diagram



General Description

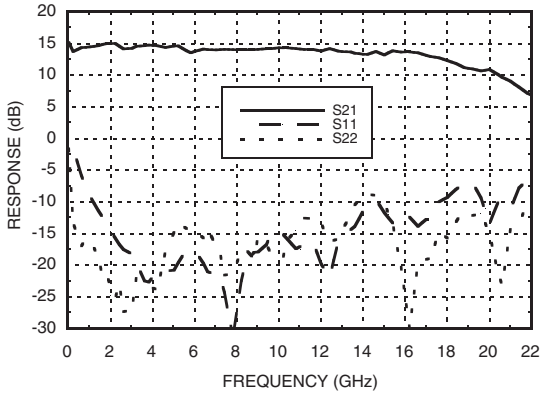
The HMC464LP5 & HMC464LP5E are GaAs MMIC PHEMT Distributed Power Amplifiers in leadless 5 x 5 mm surface mount packages which operate between 2 and 20 GHz. The amplifier provides 14 dB of gain, +30 dBm output IP3 and +26 dBm of output power at 1 dB gain compression while requiring 290 mA from a +8V supply. Gain flatness is good from 2 - 18 GHz making the HMC464LP5(E) ideal for EW, ECM and radar driver amplifiers as well as test equipment applications. The wideband amplifier I/O's are internally matched to 50 Ohms.

Electrical Specifications, T_A = +25° C, Vdd= 8V, Vgg2= 3V, Idd= 290 mA [1]

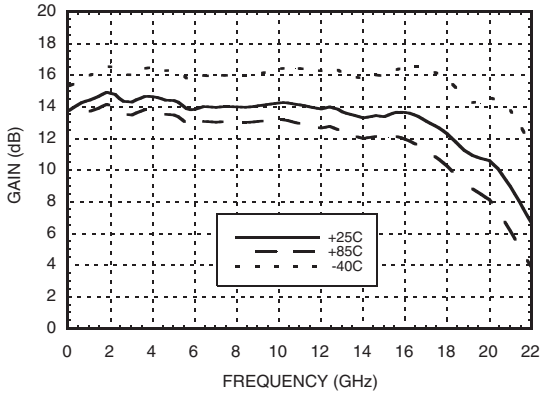
Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		2.0 - 6.0			6.0 - 16.0			16.0 - 20.0		GHz
Gain	12	14		11.5	13.5		8	11		dB
Gain Flatness		±0.5			±0.5			±1.0		dB
Gain Variation Over Temperature		0.025	0.035		0.03	0.04		0.05	0.06	dB/ °C
Input Return Loss		15			10			7		dB
Output Return Loss		15			9			11		dB
Output Power for 1 dB Compression (P1dB)	23.5	26.5		22	25		18	21		dBm
Saturated Output Power (Psat)		27.5			26			24.0		dBm
Output Third Order Intercept (IP3)		32			26			22		dBm
Noise Figure		4.0			4.0			6.0		dB
Supply Current (Idd) (Vdd= 8V, Vgg= -0.5V Typ.)		290			290			290		mA

[1] Adjust Vgg1 between -2 to 0V to achieve Idd = 290 mA typical.

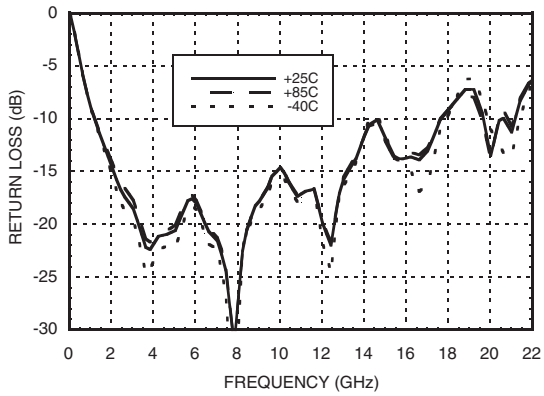
Gain & Return Loss



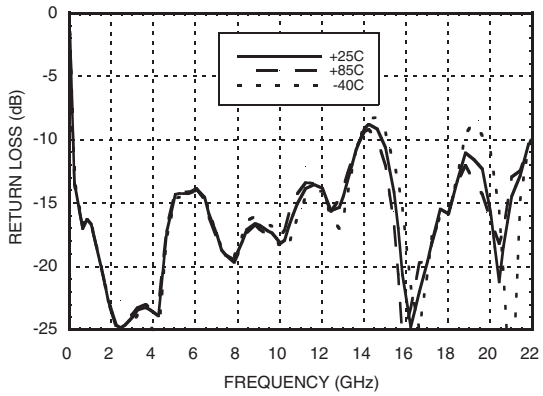
Gain vs. Temperature



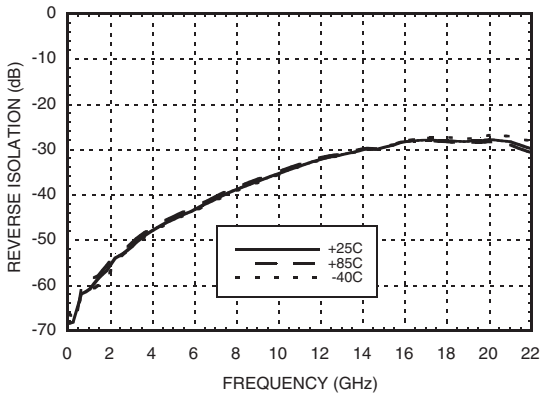
Input Return Loss vs. Temperature



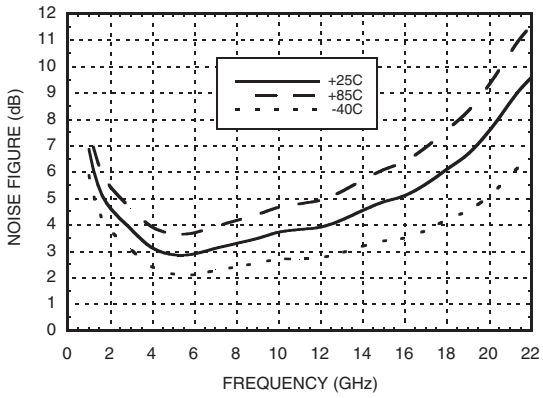
Output Return Loss vs. Temperature



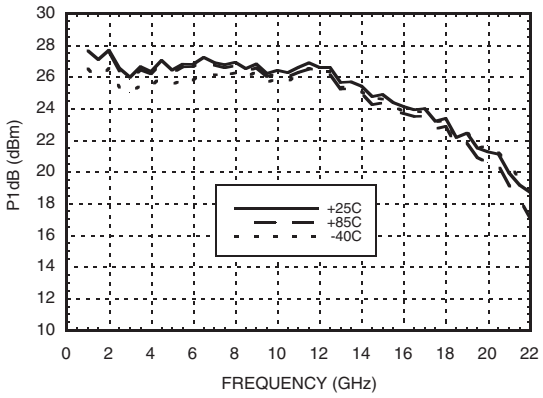
Reverse Isolation vs. Temperature



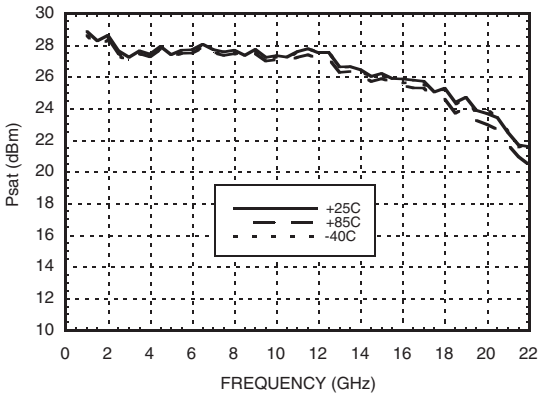
Noise Figure vs. Temperature



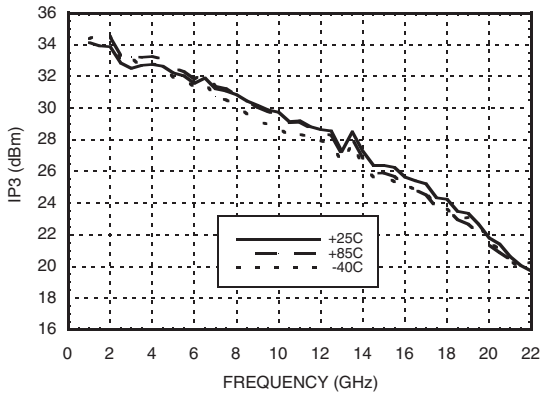
P1dB vs. Temperature



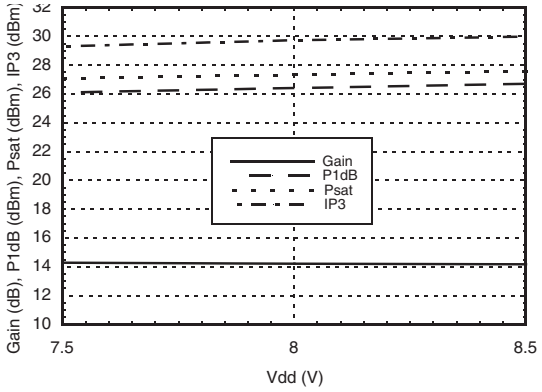
Psat vs. Temperature



Output IP3 vs. Temperature



Gain, Power & Output IP3 vs. Supply Voltage @ 10 GHz, Fixed Vgg1



Absolute Maximum Ratings

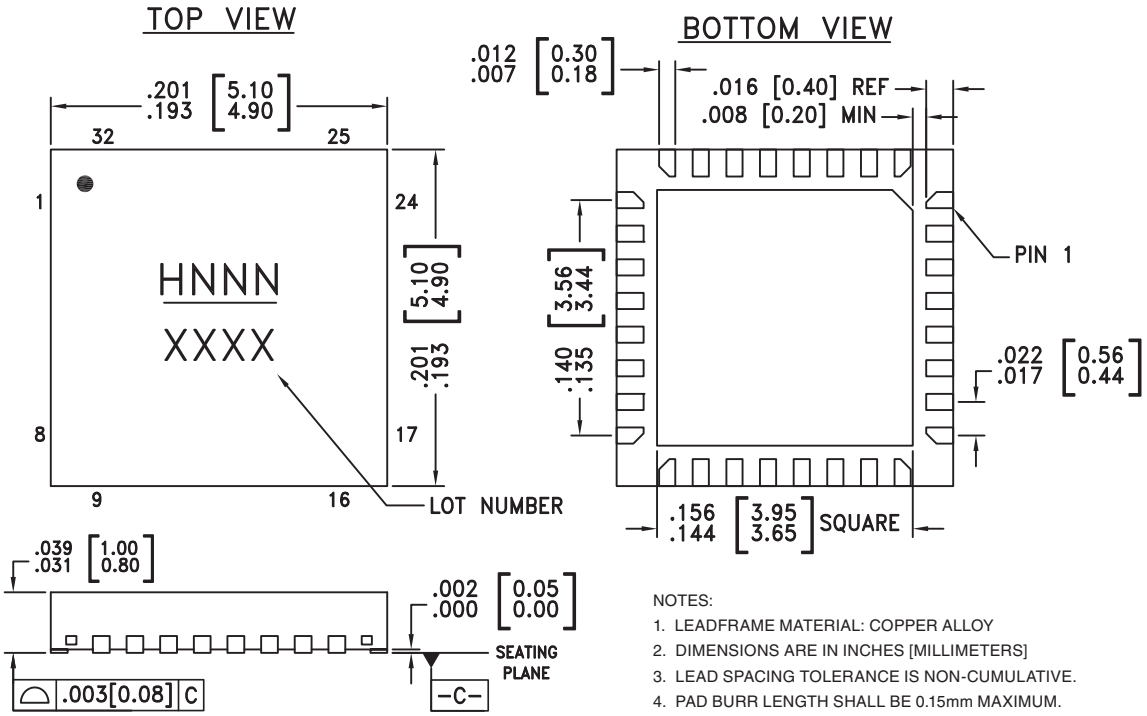
Drain Bias Voltage (Vdd)	+9 Vdc
Gate Bias Voltage (Vgg1)	-2 to 0 Vdc
Gate Bias Voltage (Vgg2)	(Vdd -8.0) Vdc to Vdd
RF Input Power (RFIN)(Vdd = +8 Vdc)	+20 dBm
Channel Temperature	150 °C
Continuous Pdiss (T= 85 °C) (derate 51.5 mW/°C above 85 °C)	3.35 W
Thermal Resistance (channel to ground paddle)	19.4 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1A

Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+7.5	292
+8.0	290
+8.5	288

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

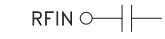
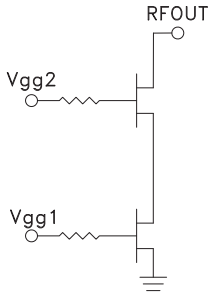
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

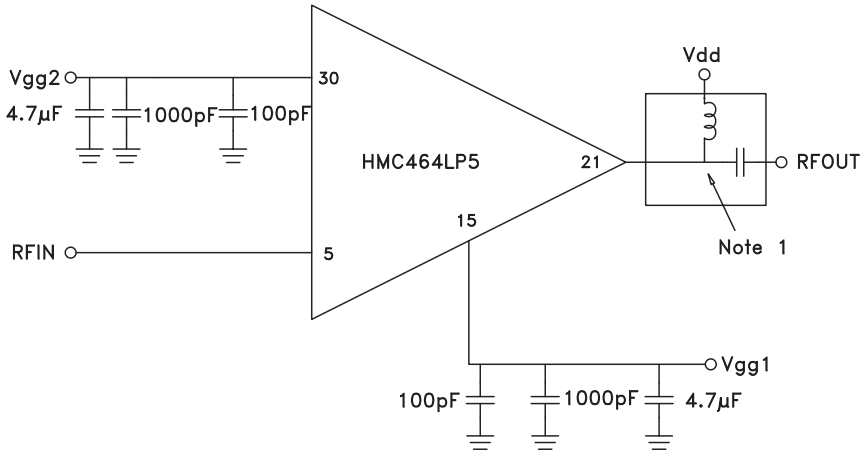
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [3]
HMC464LP5	Low Stress Injection Molded Plastic	Sn/Pb Solder	MSL1 [1]	H464 XXXX
HMC464LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H464 XXXX

[1] Max peak reflow temperature of 235 °C
[2] Max peak reflow temperature of 260 °C
[3] 4-Digit lot number XXXX

Pin Descriptions

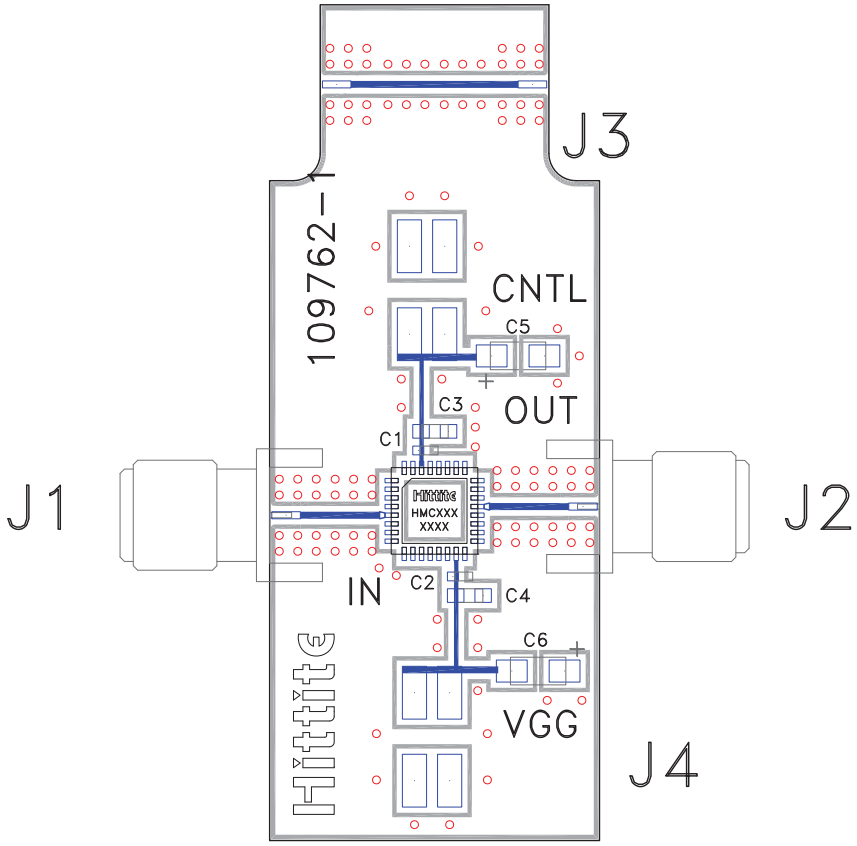
Pin Number	Function	Description	Interface Schematic
5	RFIN	This pin is AC coupled and matched to 50 Ohms.	
15	Vgg1	Gate Control for amplifier. Adjust between -2 to 0V to achieve Idd= 290 mA.	
21	RFOUT & Vdd	RF output for amplifier. Connect the DC bias (Vdd) network to provide drain current (Idd). See application circuit herein.	
30	Vgg2	Control voltage for amplifier. +3V should be applied to Vgg2 for nominal operation.	
Ground Paddle	GND	Ground paddle must be connected to RF/DC ground.	
1 - 4, 6 - 14, 16 - 20, 22 - 29, 31, 32	N/C	No connection. These pins may be connected to RF ground. Performance will not be affected.	

Application Circuit



NOTE 1: Drain Bias (Vdd) must be applied through a broadband bias tee or external bias network.

Evaluation PCB



List of Materials for Evaluation PCB 108344 [1]

Item	Description
J1, J2	PCB Mount SMA Connector
J3, J4	2 mm Molex Header
C1, C2	100 pF Capacitor, 0402 Pkg.
C3, C4	1000 pF Capacitor, 0603 Pkg.
C5, C6	4.7 µF Capacitor, Tantalum
U1	HMC464LP5 / HMC464LP5E
PCB [2]	109762 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350

The circuit board used in the final application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and package bottom should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation board should be mounted to an appropriate heat sink. The evaluation circuit board shown is available from Hittite upon request.