HMC6146BLC5A

v00.0812

GaAs MMIC I/Q UPCONVERTER 40 - 44 GHz

Typical Applications

The HMC6146BLC5A is ideal for:

- Point-to-Point and Point-to-Multi-Point Radio
- Military Radar, EW & ELINT
- Satellite Communications
- Sensors

Features

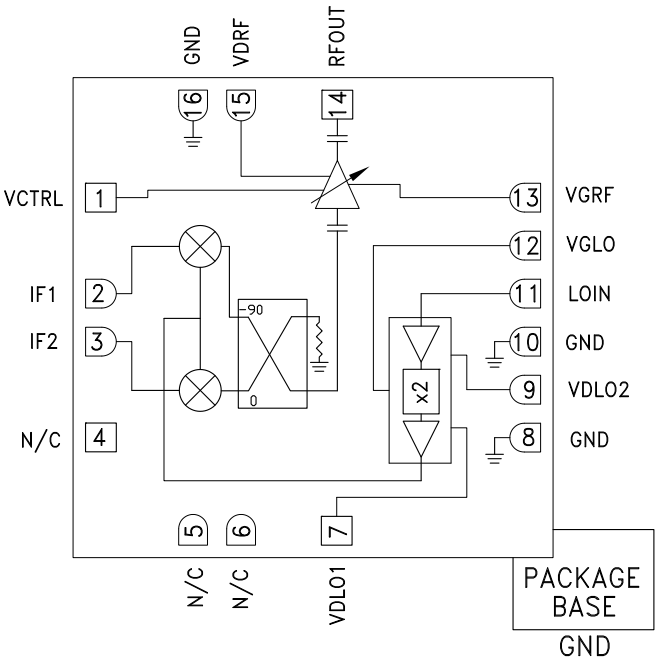
Conversion Gain: 12 dB

Sideband Rejection: 25 dBc

High Output IP3: +27 dBm

16 Lead 5x5 mm SMT Ceramic Package: 25 mm²

Functional Diagram



General Description

The HMC6146BLC5A is a compact GaAs MMIC I/Q variable gain upconverter in a leadless RoHS compliant SMT package. This device provides a small signal conversion gain of 12 dB with 25 dBc of sideband rejection, and 17 db of gain control. The HMC6146BLC5A utilizes a RF variable gain amplifier preceded by an I/Q mixer where the LO is driven by a X2 multiplier. IF1 and IF2 mixer inputs are provided and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces the need for filtering of the unwanted sideband. The HMC6146BLC5A is a much smaller alternative to hybrid style single sideband upconverter assemblies and it eliminates the need for wire bonding by allowing the use of surface mount manufacturing techniques.

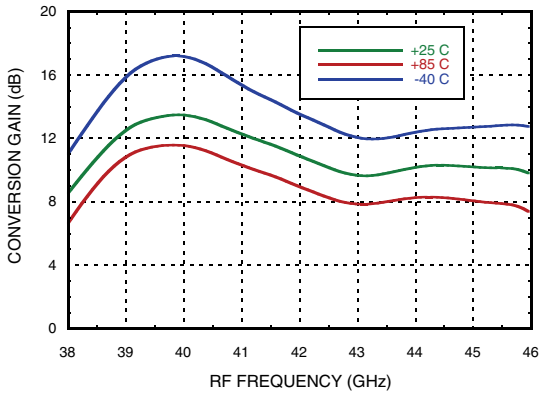
Electrical Specifications [1][2], T_A = +25°C, IF = 2350 MHz, LO = +4 dBm, VDLO1, 2 = +3V, IDLO = 150 mA, VDRF = +3V, IDRF = 200mA, USB [1][2]

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range, RF		40 - 42			42 - 44		GHz
Frequency Range, LO		18 - 20			20 - 22		GHz
Frequency Range, IF		0 - 4			0 - 4		GHz
Conversion Gain	9	12		7	10		dB
Sideband Rejection	21	25		14	18		dBc
Dynamic Range		17			13		dB
1 dB Compression (Output)		16			16		dBm
IP3 (Output)		27			28		dBm
2LO / RF Isolation		15			15		dB
Supply Current IDLO [2]		150			150		mA
Supply Current IDRF [2]		200			200		mA

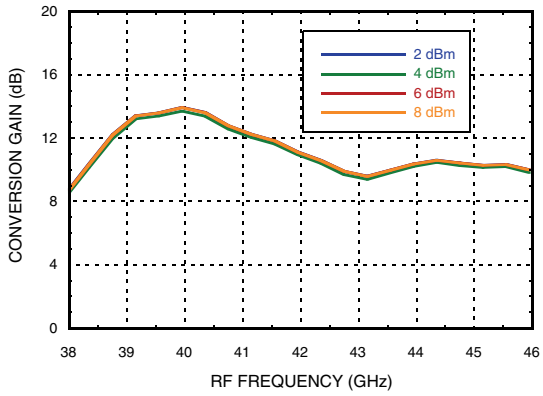
[1] Unless otherwise noted all measurements performed with low side LO, IF = 2350 MHz and external IF 90° hybrid.
[2] Adjust Vgg between -2 to 0V to achieve IDLO = 150 mA and IDRF = 200 mA Typical.

Data Taken as SSB Upconverter with External IF 90° Hybrid, IF = 2350 MHz

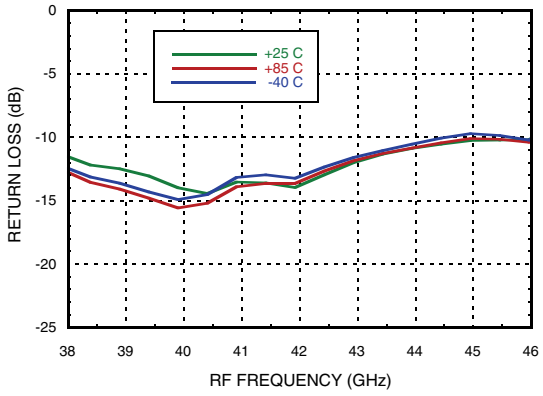
Conversion Gain, USB vs. Temperature



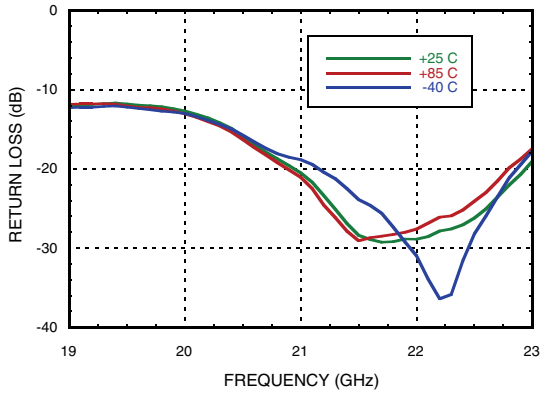
Conversion Gain, USB vs. LO Drive



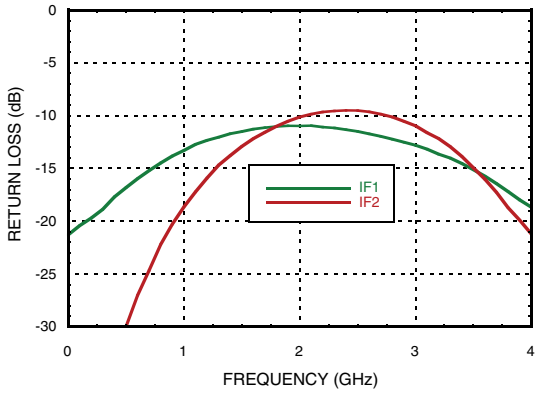
RF Return Loss vs. Temperature



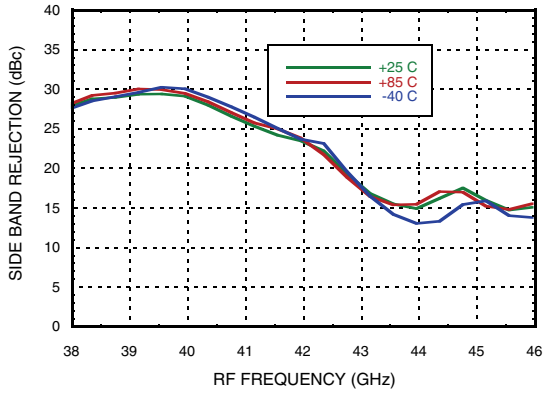
LO Return Loss vs. Temperature



IF Return Loss [1]



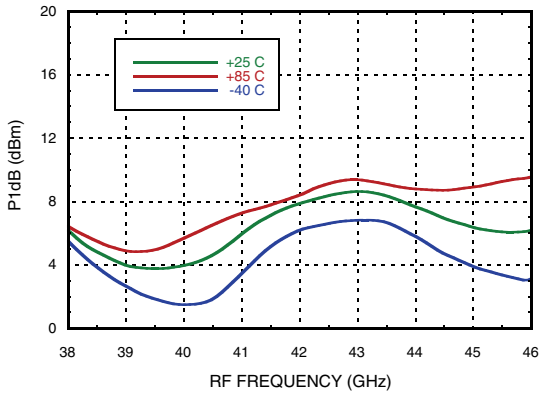
Sideband Rejection vs. Temperature



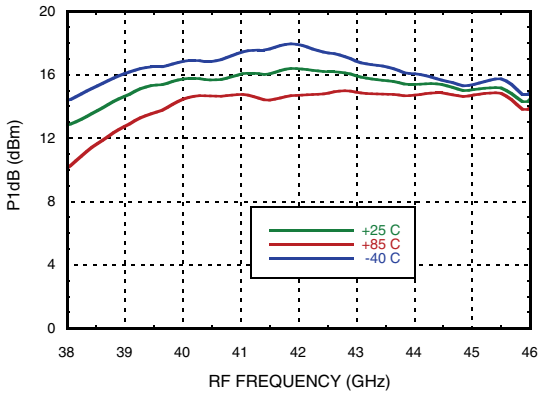
[1] Data taken without external IF 90° hybrid

Data Taken as SSB Upconverter with External IF 90° Hybrid, IF = 2350 MHz

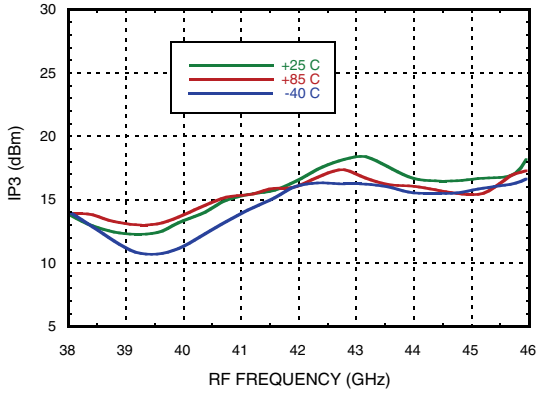
Input P1dB, USB vs. Temperature



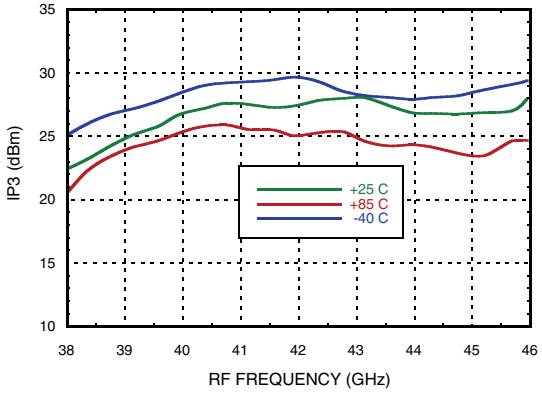
Output P1dB, USB vs. Temperature



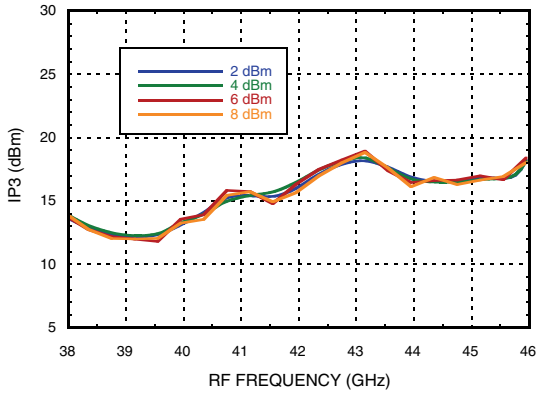
Input IP3, USB vs. Temperature



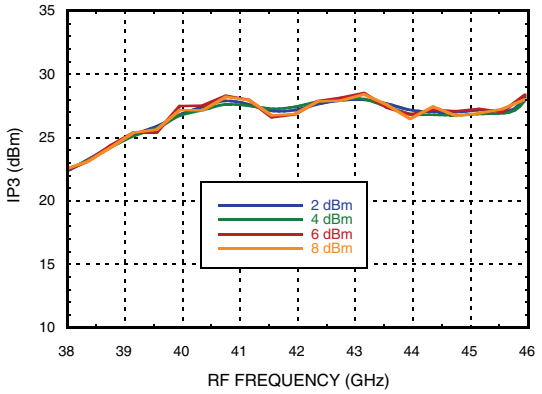
Output IP3, USB vs. Temperature



Input IP3, USB vs. LO Drive

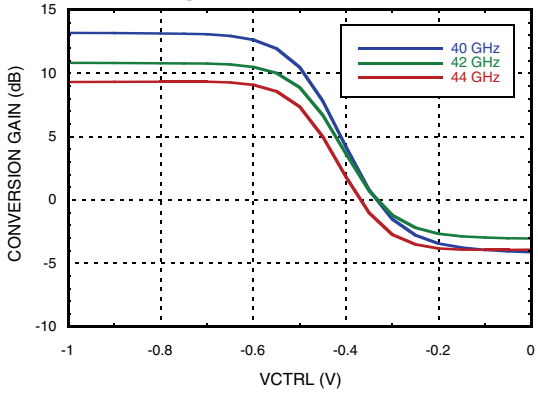


Output IP3, USB vs. LO Drive

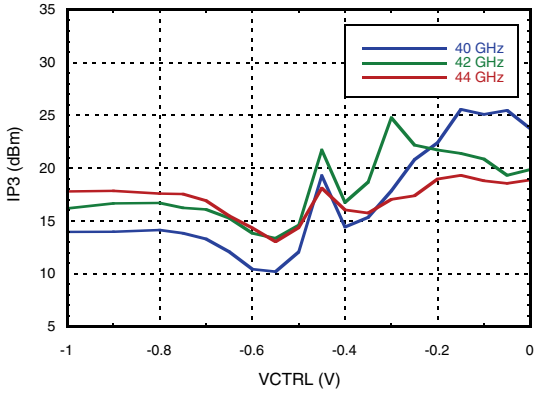


Data Taken as SSB Upconverter with External IF 90° Hybrid, IF = 2350 MHz

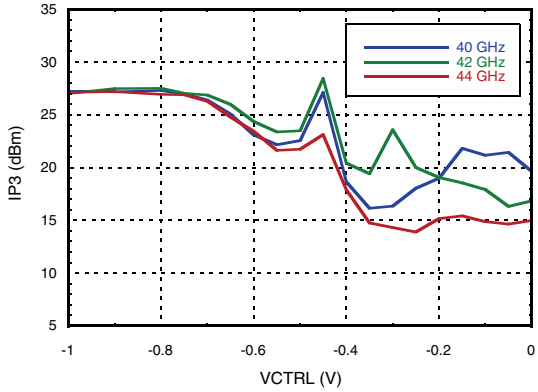
Conversion Gain, USB vs. Control Voltage [1]



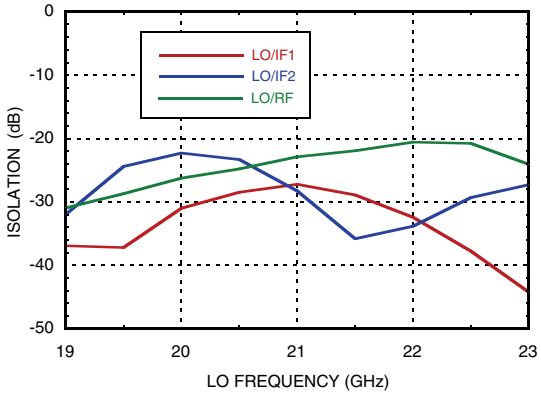
Input IP3, USB vs. Control Voltage [1]



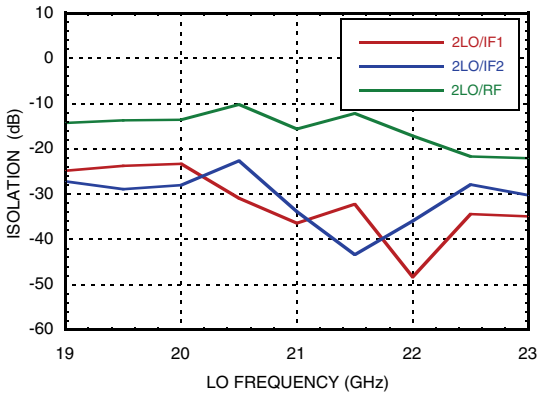
Output IP3, USB vs. Control Voltage [1]



LO Isolation



2LO Isolation



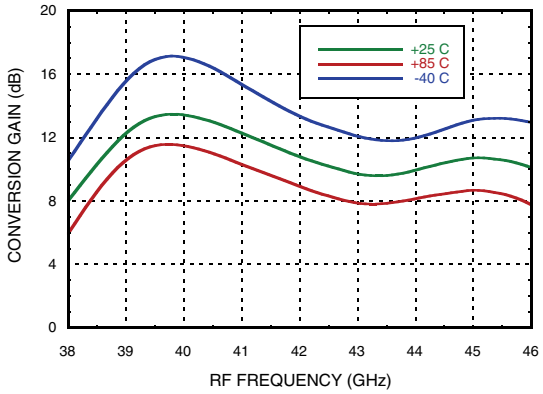
[1] Control voltage plots taken at 150 mA

HMC6146BLC5A

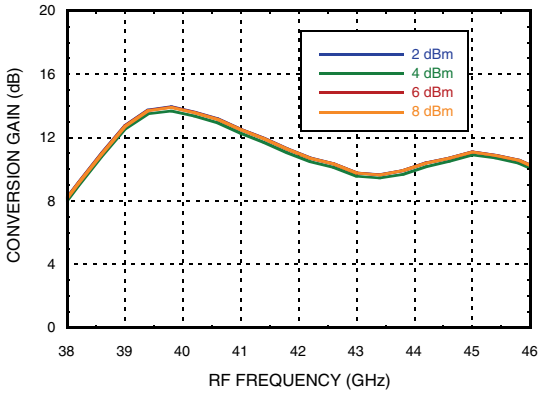
GaAs MMIC I/Q UPCONVERTER 40 - 44 GHz

Data Taken as SSB Upconverter with External IF 90° Hybrid, IF = 3000 MHz

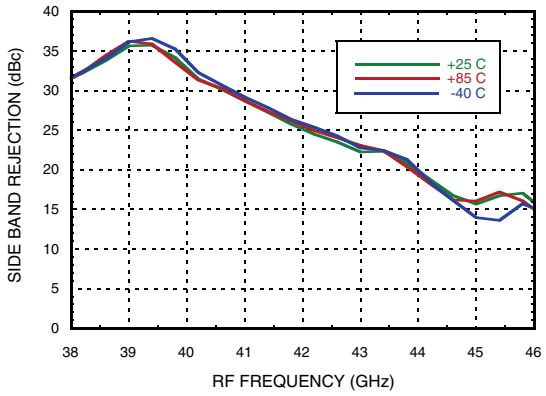
Conversion Gain, USB vs. Temperature



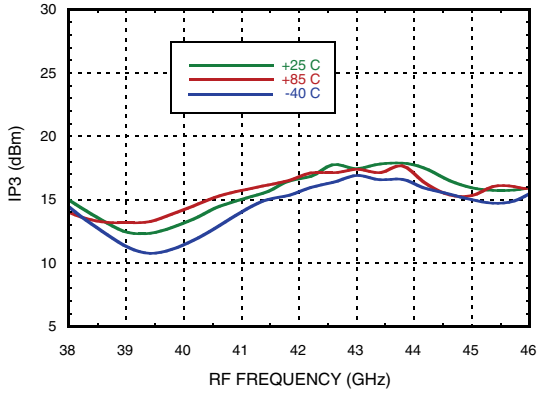
Conversion Gain, USB vs. LO Drive



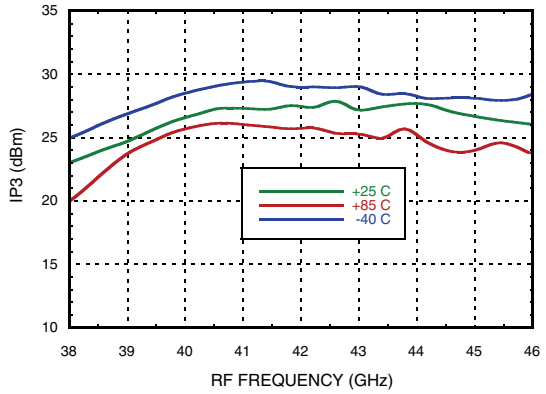
Sideband Rejection vs. Temperature



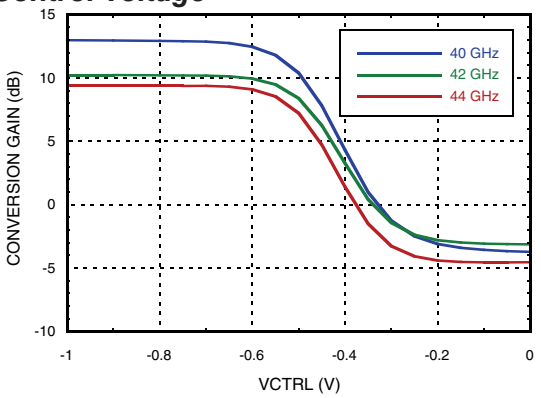
Input IP3, USB vs. Temperature



Output IP3, USB vs. Temperature



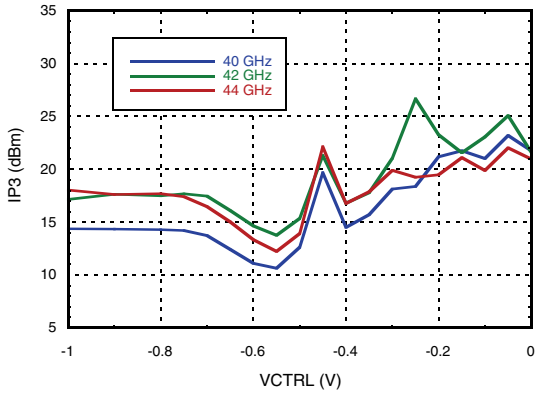
Conversion Gain, USB vs. Control Voltage [1]



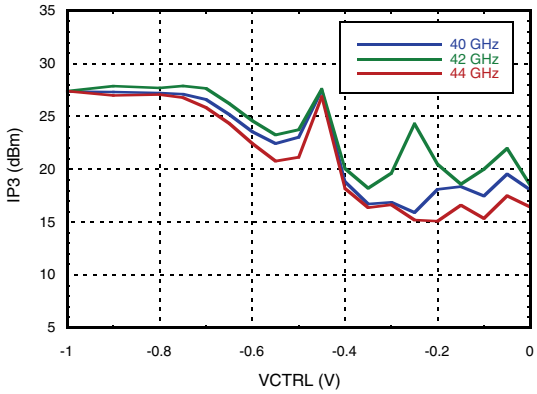
[1] Control voltage plots taken at 150 mA

Data Taken as SSB Upconverter with External IF 90° Hybrid, IF = 3000 MHz

Input IP3, LSB vs. Control Voltage [1]



Output IP3, LSB vs. Control Voltage [1]

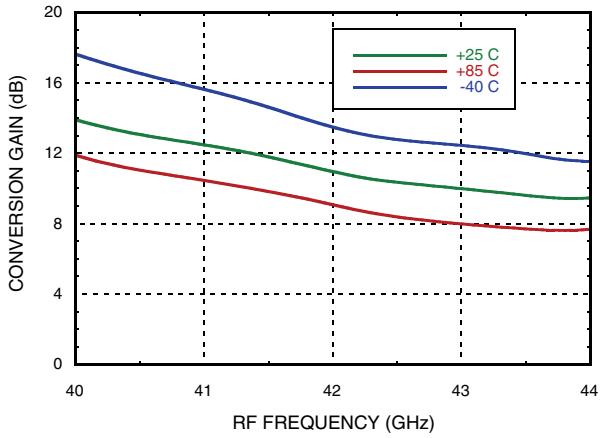


[1] Control voltage plots taken at 150 mA

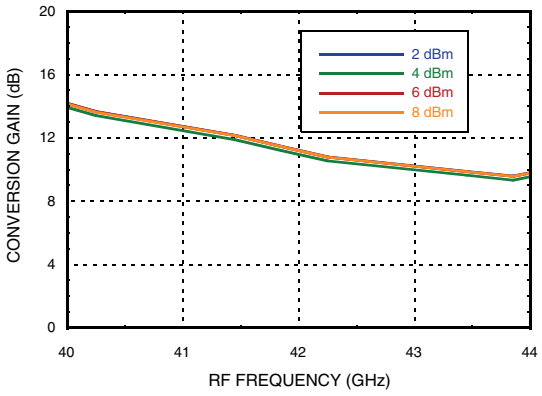
GaAs MMIC I/Q UPCONVERTER 40 - 44 GHz

Data Taken as SSB Upconverter with External IF 90° Hybrid, IF = 3750 MHz

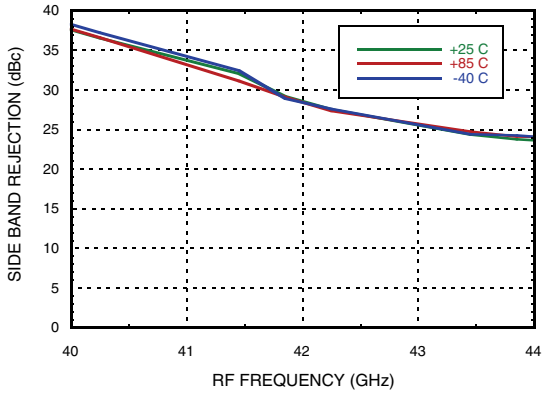
Conversion Gain, USB vs. Temperature



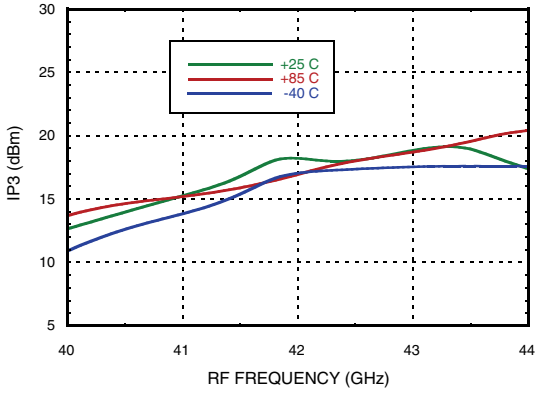
Conversion Gain, USB vs. LO Drive



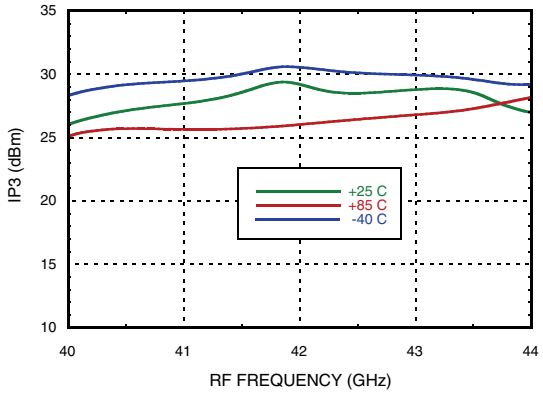
Sideband Rejection vs. Temperature



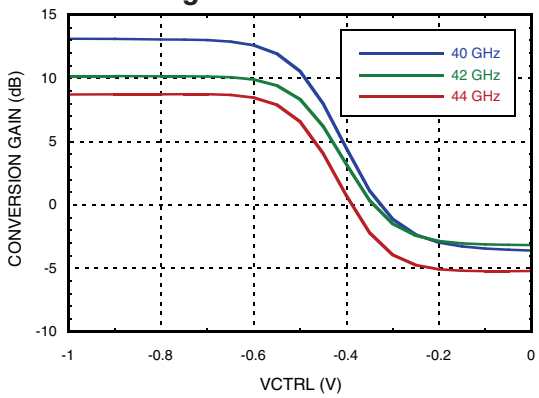
Input IP3, USB vs. Temperature



Output IP3, USB vs. Temperature



Conversion Gain, USB vs. Control Voltage [1]

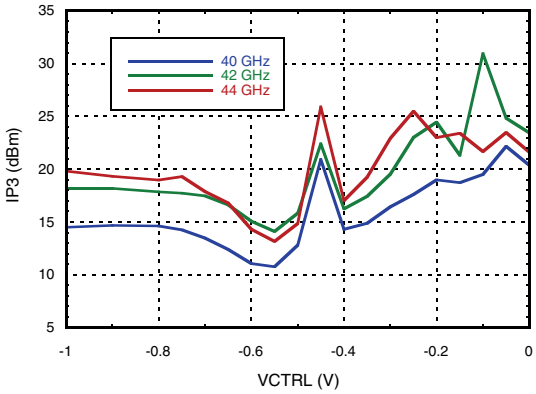


[1] Control voltage plots taken at 150 mA

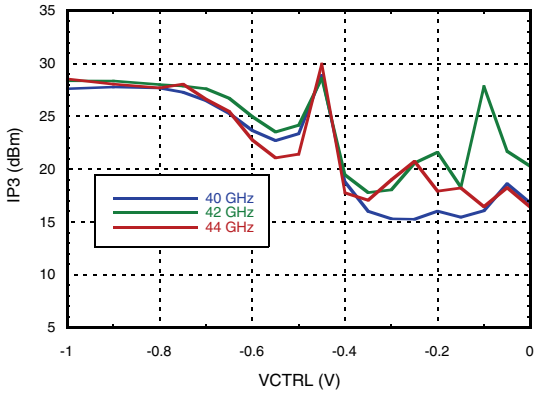
GaAs MMIC I/Q UPCONVERTER 40 - 44 GHz

Data Taken as SSB Upconverter with External IF 90° Hybrid, IF = 3750 MHz

Input IP3, LSB vs. Control Voltage [3]



Output IP3, LSB vs. Control Voltage [3]



MxN Spurious Outputs [1][2]

	nLO				
mIF	0	1	2	3	4
0		31	22		
1	68	76	0		
2	71	88	60		
3	120	110	73		
4	120	120	120		
5	120	120	120		

IF = 2.35 GHz @ -8 dBm
LO = 19.075 GHz @ +4 dBm

MxN Spurious Outputs [1][2]

	nLO				
mIF	0	1	2	3	4
0		28	14		
1	61	63	0		
2	69	85	60		
3	109	109	83		
4	118	118			
5	118	118			

IF = 3 GHz @ -8 dBm
LO = 19.5 GHz @ +4 dBm

MxN Spurious Outputs [1][2]

	nLO				
mIF	0	1	2	3	4
0		25	7		
1	55	67	0		
2	66	91	51		
3	116	108			
4	116	116			
5	116	116			

IF = 4 GHz @ -8 dBm
LO = 19.75 GHz @ +4 dBm

[1] Data taken without external IF 90° hybrid
[2] All values in dBc below RF power level (2LO + IF) USB
[3] Control voltage plots taken at 150 mA

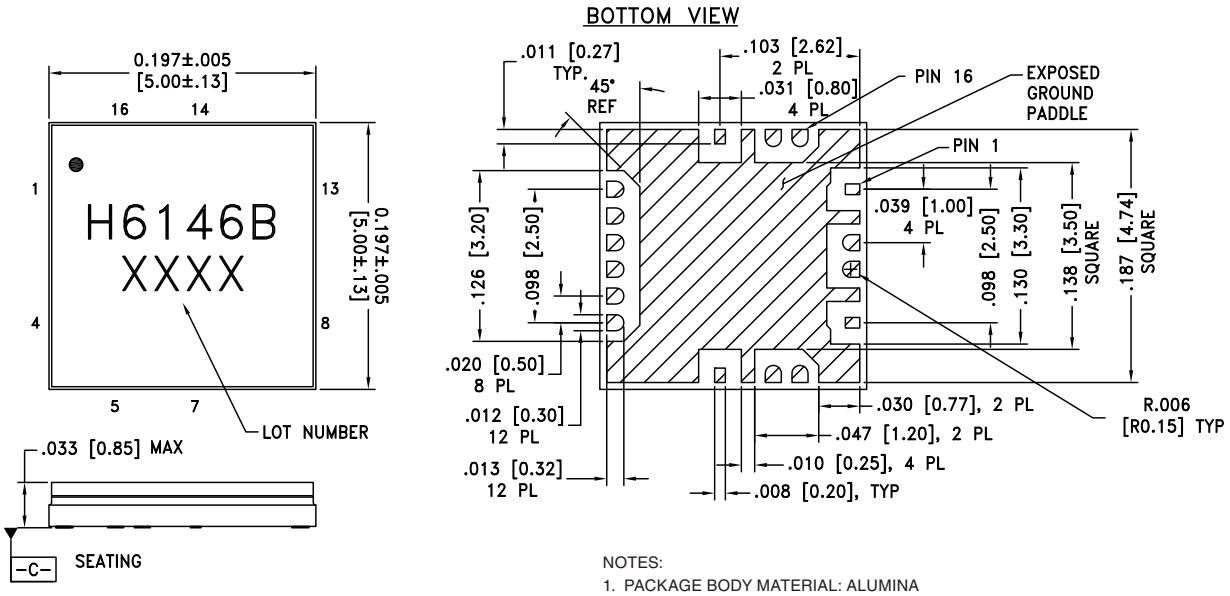
GaAs MMIC I/Q UPCONVERTER 40 - 44 GHz

Absolute Maximum Ratings

IF Input	+20 dBm
LO Input	+10 dBm
Channel Temperature	175 °C
Continuous Pdiss (T = 85°C) (derate 18.3 mW/°C above 85°C)	1.65 W
Thermal Resistance (channel to ground paddle)	54.6 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 0 Passed 150V

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



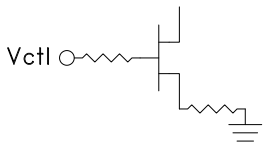
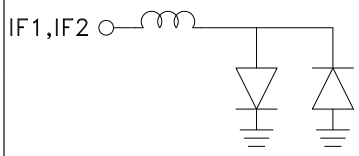
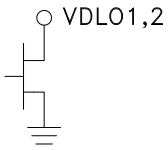
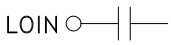
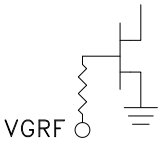
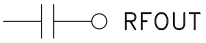
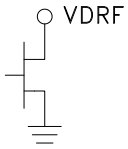
NOTES:
1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING: 30 - 80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKLE
3. DIMENSIONS ARE IN INCHES [MILLIMETERS]
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND

Package Information

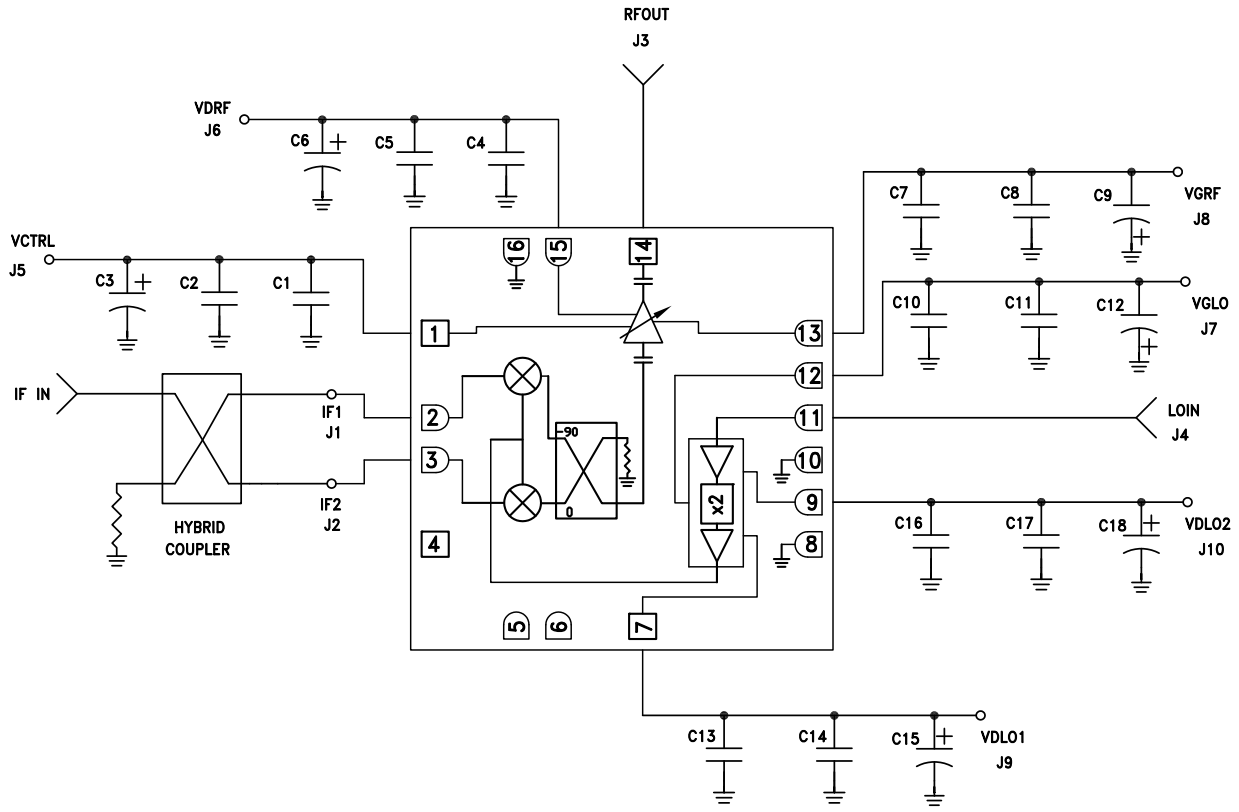
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC6146BLC5A	Alumina, White	Gold over Nickel	MSL3 [1]	6146B XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

Pin Descriptions

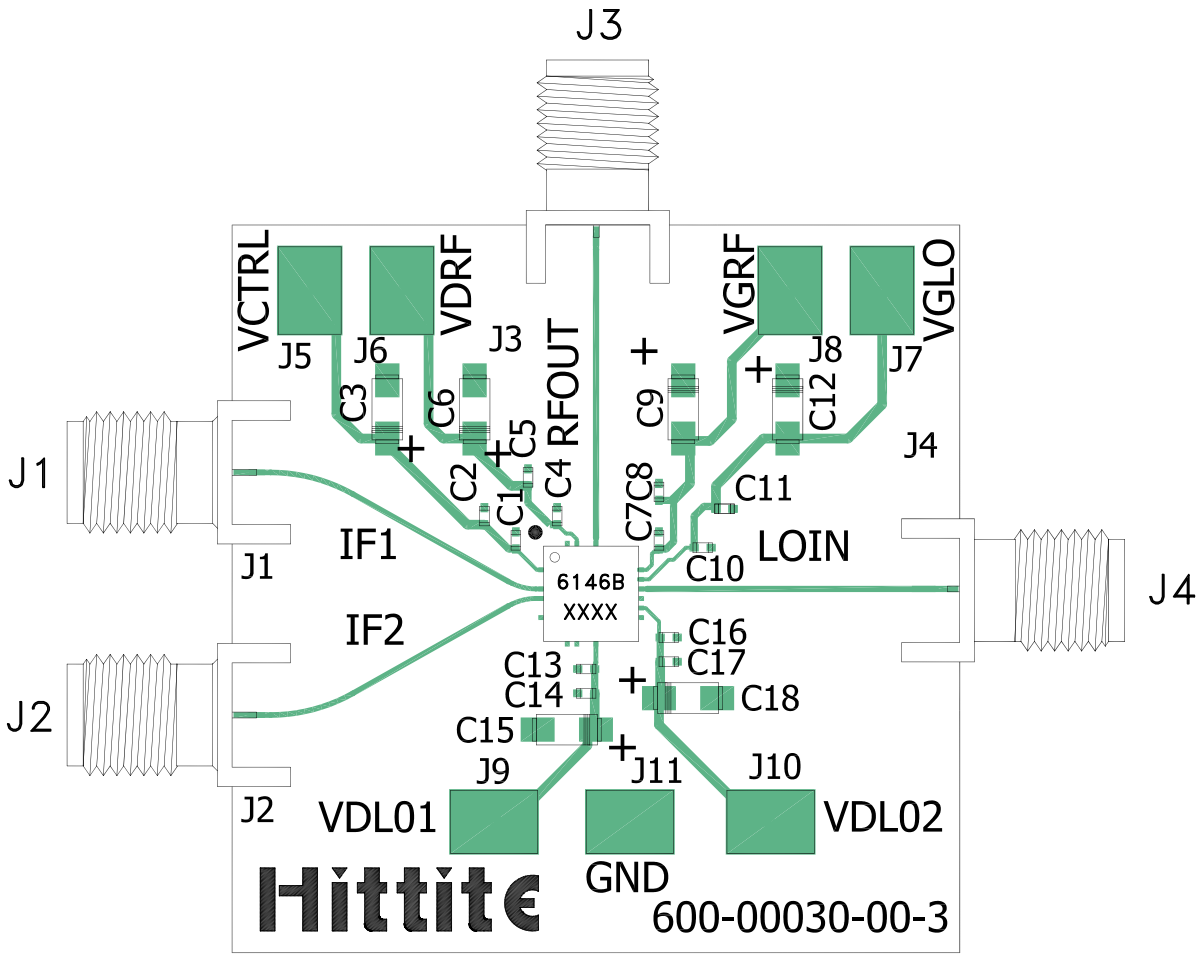
Pin Number	Function	Description	Interface Schematic
1	VCTRL	Vary Vctrl from -2V to 0V to adjust conversion gain.Maximum Gain occurs at -2V. Current draw << 1 mA.	
2	IF1	Pins are DC coupled Must not source or sink more than +/- 3 mA for applications requiring operation to DC.	
3	IF2		
4, 5, 6	N/C	No connection required. The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
7	VDLO1	Bias for multiplier input buffer amp. The recommended DC voltage is +3V.	
9	VDLO2	Bias for multiplier input buffer amp. The recommended DC voltage is +3V.	
8, 10, 16	GND	These pins and package bottom must be connected to RF/DC ground.	
11	LOIN	LO input port. The recommeded LO power is 0 to 5 dBm.	
12	VGLO	Adjust VGLO for -1V to 0V to set the multiplier quiescent current to 120 mA (200 - 230 mA with LO Drive).	
13	VGRF	Adjust VGRF for -1V to 0V to set the VGA current to 200 mA.	
14	RFOUT	RF output port.	
15	VDRF	Bias voltage for the VGA.	

Typical Application



C1, C4, C7, C10, C13, C16	100 pF Capacitor, 0402 Pkg.
C2, C5, C8, C11, C14, C17	0.1 uF Capacitor, 0402 Pkg.
C3, C6, C9, C12, C15, C18	4.7 µF Capacitor, Case A Pkg.

Evaluation PCB



List of Materials for Evaluation PCB Eval01-HMC6146BLC5A [1]

Item	Description
J1, J2	SMA Connector
J3, J4	K-Connector SRI
J5 - J11	DC Pins
C1, C4, C7, C10, C13, C16	100 pF Capacitor, 0402 Pkg.
C2, C5, C8, C11, C14, C17	0.1 uF Capacitor, 0402 Pkg.
C3, C6, C9, C12, C15, C18	4.7 µF Capacitor, Case A
U1	HMC6146BLC5A Upconverter
PCB [2]	600-00030-00 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR, FR4 or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.