v01.0811

HMC675LP3E

10 GHz LATCHED COMPARATOR WITH RSCML OUTPUT STAGE

Typical Applications

The HMC675LP3E is ideal for:

- ATE Applications
- High Speed Instrumentation
- Digital Receiver Systems
- Pulse Spectroscopy
- High Speed Trigger Circuits
- Clock & Data Restoration

Features

Equivalent Input Bandwidth: 10 GHz

Propagation Delay: 100 ps

Overdrive & Slew Rate Dispersion: 10 ps

Minimum Pulse Width: 60 ps

Resistor Programmable Hysteresis

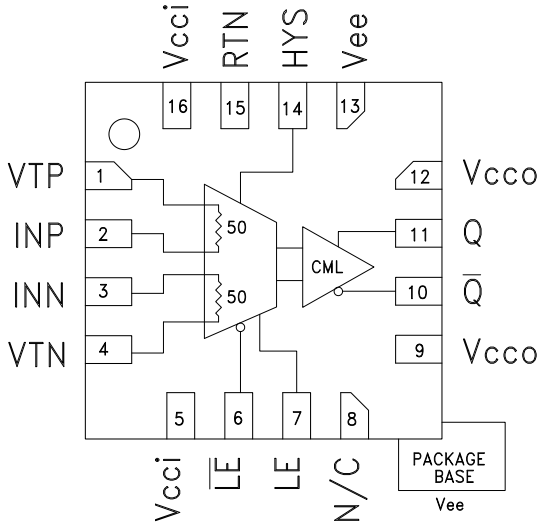
Differential Latch Control

Power Dissipation: 100 mW

RSPECL and RSECL Versions Available

16 Lead 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC675LP3E is a SiGe monolithic, ultra fast comparator which features reduced swing (RS) CML output drivers and latch inputs. The comparator supports 10 Gbps operation while providing 100 ps propagation delay and 60 ps minimum pulse width with 0.2 ps rms random jitter (RJ). Overdrive and slew rate dispersion are typically 10 ps, making the device ideal for a wide range of applications from ATE to broadband communications. The reduced swing CML output stage is designed to directly drive 400 mV into 50 Ohms terminated to GND. The HMC675LP3E features high speed latch and programmable hysteresis and may be configured to operate in either latch mode, or as a tracking comparator.

Electrical Specifications, T_A = +25 °C, Vcci= +3.3 V, Vcco = 0 V, Vee = -3 V, V_{TERM} = 0 V

Parameter	Conditions	Min.	Typ.	Max	Units
Input Voltage Range		-2		2	V
Input Differential Voltage		-1.75		1.75	V
Input Offset Voltage			±5		mV
Input Offset Voltage, Temperature Coefficient			15		µV / °C
Input Bias Current			15		uA
Input Bias Current Temperature Coefficient			50		nA / °C
Input Offset Current			4		µA
Input Impedance			50		Ω
Common Mode Input Impedance			350		KΩ
Differential Input Impedance			15		KΩ
Active Gain			43		dB
Common Mode Rejection Ratio			80		dB
Hysteresis	Rhys = ∞		±1		mV

Latch Enable Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
Latch Enable Input Impedance	Each Pin		8		KΩ
Latch to Output Delay, t_{PLOL}, t_{PLOH}	VOD = 200 mV		85		ps
Latch Minimum Pulse Width, t_{PL}	VOD = 200 mV		20		ps
Latch Enable Input Range	VOD = 200 mV	1.6		2.4	V
Latch Setup Time, t_S	VOD = 200 mV		45		ps
Latch Hold Time, t_H			-42		ps

DC Output Characteristics, with 50 Ω to GND

Parameter	Conditions	Min.	Typ.	Max	Units
Output Voltage High Level, Voh		-10		0	mV
Output Voltage Low Level, Vol		-420	-400	-380	mV
Output Voltage Differential Swing		410	400	380	mV

AC Performance

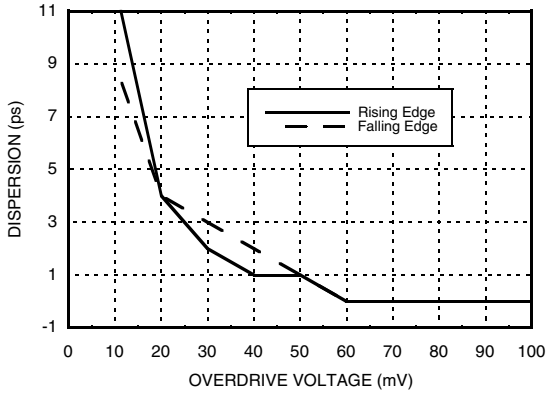
Parameter	Conditions	Min.	Typ.	Max	Units
Propagation Delay - t_{PD}, t_{PDL}, t_{PDH}	VOD = 500 mV	70	100	130	ps
Propagation Delay, Temperature Coefficient			0.45		ps / °C
Propagation Delay Skew (Rising to Falling Transition)	VOD - 500 mV		10		ps
VOD Dispersion	50 mV < VOD < 1 V		10		ps
t_{PD} vs. Common Mode Dispersion, -1.75 V <Vcm <1.75 V	VOD = 500 mV		3		ps
Noise (RTI)			3.2		nV/√(Hz) RTI
Equivalent Input Bandwidth [1]		8.5	10	10.5	GHz
Deterministic Jitter (pp)	Deterministic Jitter at 10 Gbps with ±100 mV Overdrive		2		ps
Random Jitter (rms)	Random Jitter at 10 Gbps with ±100 mV Overdrive		0.2		ps rms
Input Signal Minimum Pulse Width			60		ps
Q / QB Rise Time	From 20% to 80%		27		ps
Q / QB Fall Time	From 20% to 80%		18		ps

Power Supply Requirements

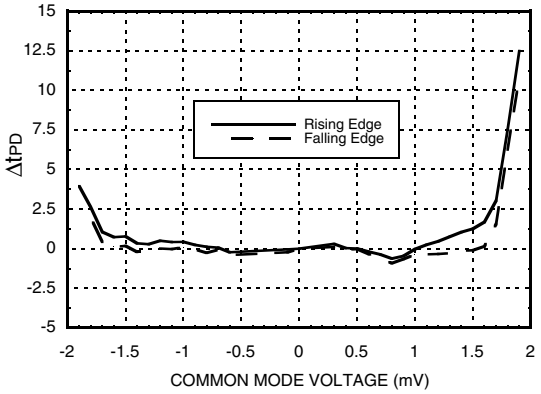
Parameter	Conditions	Min.	Typ.	Max	Units
Input Supply Current, Icci			9		mA
Output Supply Current, Icco			8		mA
Vee Current, Iee			24		mA
Power Dissipation, Pd			100		mW
PSRR, Vcci			35		dB
PSRR, Vee			35		dB

Note 1: Equivalent Input Bandwidth is calculated with the following formula: Bweq=0.22/√ (TRCOMP^2-TRIN^2) where TRIN is the 20%/80% transition time of a quasi-Gaussian signal applied to the comparator input, and TRCOMP is the effective transition time digitized by the comparator.

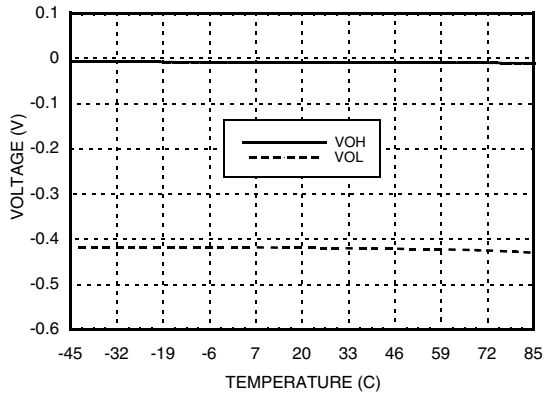
Dispersion vs. Overdrive Voltage



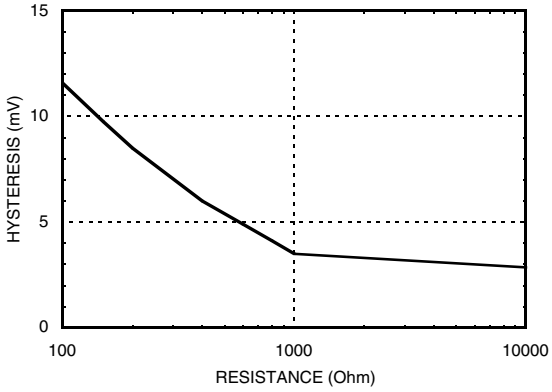
Propagation Delay vs. Common Mode[1]



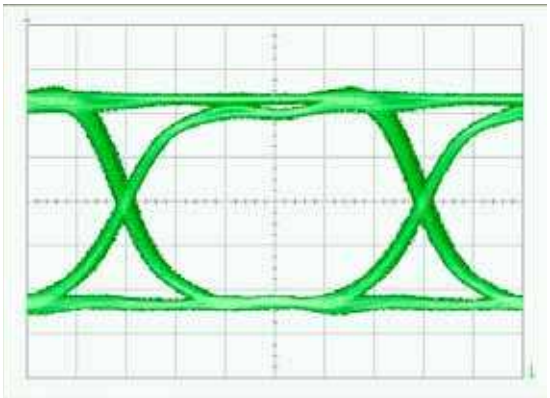
Output Voltage vs. Temperature



Comparator Hysteresis vs. Rhys Control Resistor

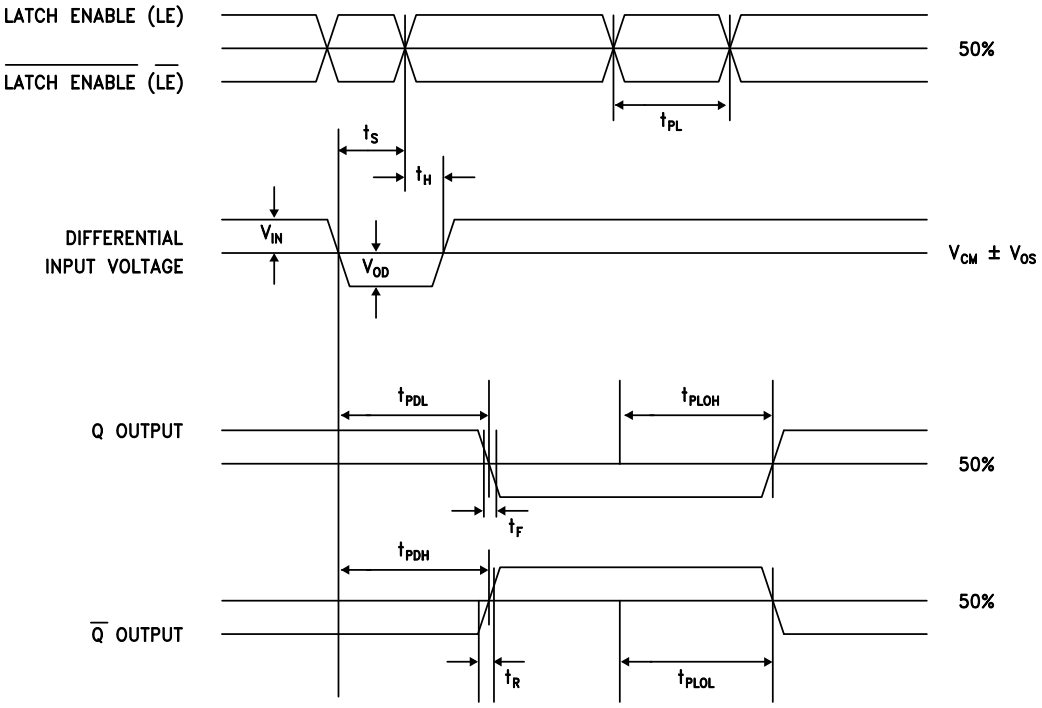


Eye Diagram



[1] Vcci = 3.3 V, Vcc0 = 0, Vee = -3 V, V_{TERM} = 0

Timing Diagram



Timing Descriptions

Symbol	Timing	Description
t_{PDH}	Input to output high delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output low-to-high transition.
t_{PDL}	Input to output low delay	Propagation delay measured from the time the input signal crosses the reference (± the input offset voltage) to the 50% point of an output high-to-low transition.
t_{PLOH}	Latch enable to output high delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output low-to-high transition.
t_{PLOL}	Latch enable to output low delay	Propagation delay measured from the 50% point of the latch enable signal low-to-high transition to the 50% point of an output high-to-low transition.
t_H	Minimum hold time	Minimum time after the positive transition of the latch enable signal that the input signal must remain unchanged to be acquired and held at the outputs.
t_{PL}	Minimum latch enable pulse width	Minimum time that the latch enable signal must be high to acquire an input signal change.
t_S	Minimum setup time	Minimum time before the positive transition of the latch enable signal that an input signal change must be present to be acquired and held at the outputs.
t_R	Output rise time	Amount of time required to transition from a low to a high output as measured at the 20% and 80% points.
t_F	Output fall time	Amount of time required to transition from a high to a low output as measured at the 20% and 80% points.
V_{OD}	Voltage overdrive	Difference between the input voltages V_{INP} and V_{INN}.

Operational Description

The HMC675LP3E is a Latched Comparator with 10 GHz equivalent input bandwidth. The device is comprised of three blocks: 1) An input amplifier, 2) A latch, and 3) An RSCML Output Buffer. The latching circuit is level sensitive, and consists of a single high-speed latch. The HMC675LP3E comparator supports 10 Gb/s operation. The minimum input data latching pulse width is 60 ps.

The HMC675LP3E operates in either Track (Transparent) Mode, where the output follows the logical value of the input, or the Latch (Hold) Mode, where the output value is held to the logical value of the comparison result of the input just prior to (LE - LE_bar) going HI. Track Mode operation is selected by either 1) (LE - LE_bar) LO, or 2) LE and LE_bar inputs floating. Latch Mode is selected by (LE - LE_bar) HI. The input impedance of the LE and LE_bar inputs is 8 k ohms, but these inputs can be terminated with 50 ohm external resistors if desired.

When DC coupled, the clock inputs operate at an input common mode voltage of 2 V. In this case, any termination resistors would ideally be returned to 2 V. If the clock is AC coupled to the device, the input termination resistors can be returned to ground.

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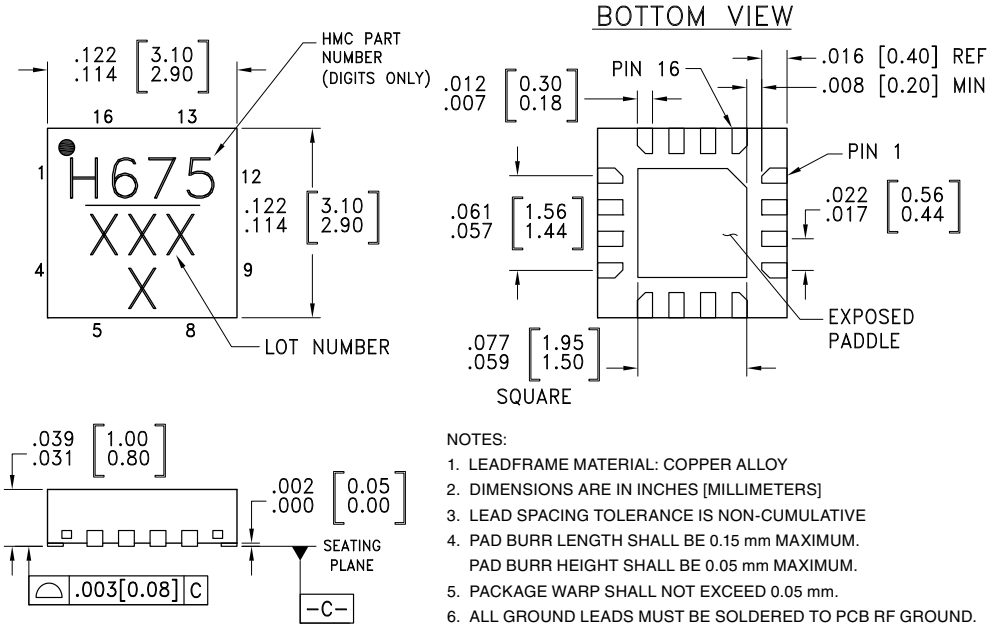
Absolute Maximum Ratings

Input Supply Voltage (Vcci to GND)	-0.5 V to +4 V
Output Supply Voltage (Vcco to GND)	-0.5 V to +4 V
Positive Supply Voltage Differential (Vcci - Vcco)	-0.5 V to +3.3 V
Input Voltage	-2 V to +2 V
Differential Input Voltage	-2 V to +2 V
Input Voltage, Latch Enable	-0.5 V to Vcci +0.5 V
Applied Voltage (HYS)	Vee to GND
Maximum Input Current	±1 mA
Output Current	20 mA
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 43.5 mW/°C above 85°C)	1.74 W
Thermal Resistance (Rth) (Junction to Lead)	23 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C
ESD Sensitivity (HBM)	Class 1A

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15 mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05 mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05 mm.
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN
8. PADDLE MUST BE SOLDERED TO Vee..

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMC675LP3E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [1]	H675 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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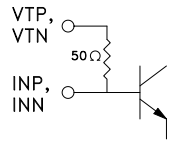
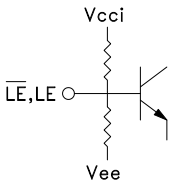
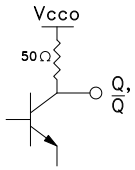
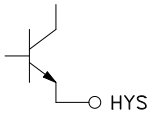
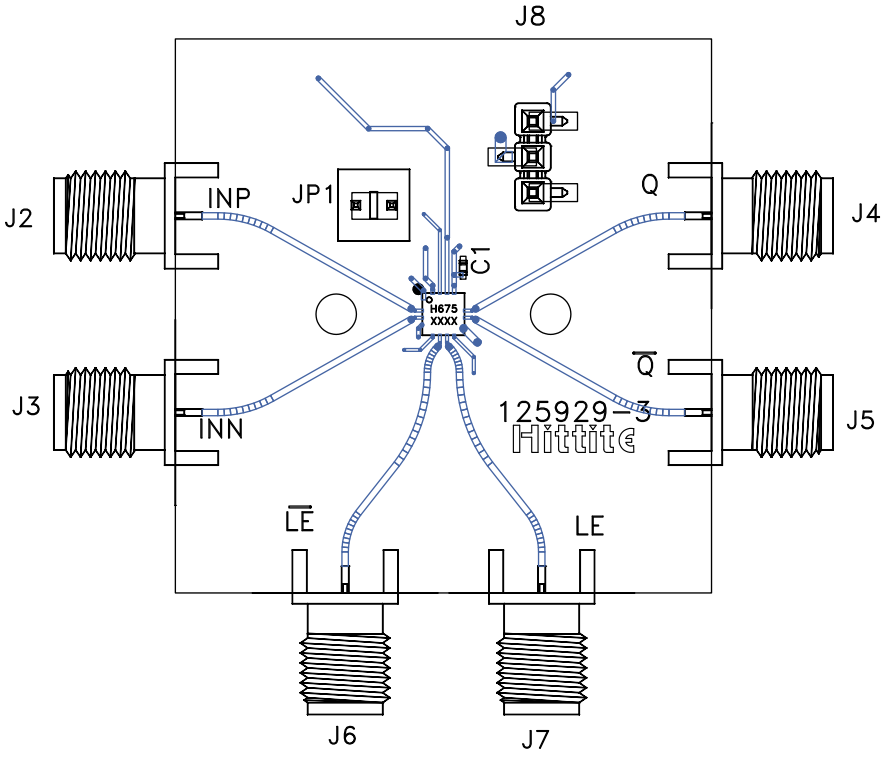
Pin Descriptions

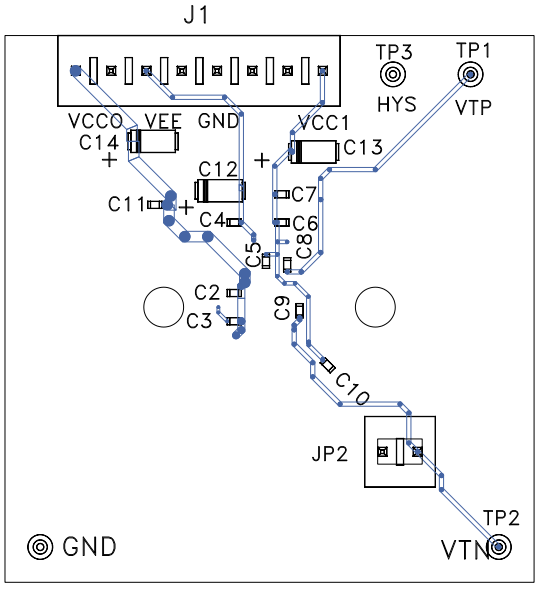
Pin Number	Function	Description	Interface Schematic
1	VTP	Termination resistor return pin for Vp Input.	
2	INP	Non-Inverting analog input	
3	INN	Inverting analog input	
4	VTN	Termination resistor return pin for Vn input	
5, 16	Vcci	Positive supply voltage input stage.	
6	$\overline{LE}$	Latch enable bar input pin, inverting side. Refer to the Operational Description for more details.	
7	LE	Latch enable bar input pin, non-inverting side. Refer to the Operational Description for more details.	
8	N/C	Pin is not connected inside the package. Connect package pin to GND for improved noise.	
9, 12	Vcco	Positive supply voltage for the output stage.	
10	$\overline{Q}$	Inverting output. Q bar is at logic low if the analog voltage at the non-inverting input, INP, is greater than the analog voltage at the inverting input, INN, provided that the comparator is in compare mode. Refer to the Operational Description for more details.	
11	Q	Non-inverting output. Q is at logic high if the analog voltage at the non-inverting input, INP, is greater than the analog voltage at the inverting input, INN, provided that the comparator is in compare mode. Refer to the Operational Description for more details.	
14	HYS	Hysteresis Control pin. This pin should be left disconnected for zero hysteresis. Connect to Vee with a resistor to add the desired amount of hysteresis. Refer to hysteresis graph to determine the correct sizing of Rhys hysteresis control resistor.	
13	Vee	Negative power supply, -3 V.	
15	RTN	Return for ESD protection.	
	Package Base	Exposed paddle must be connected to Vee.	

Evaluation PCB

Front Side



Back Side



List of Materials for Evaluation PCB 125932 [1]

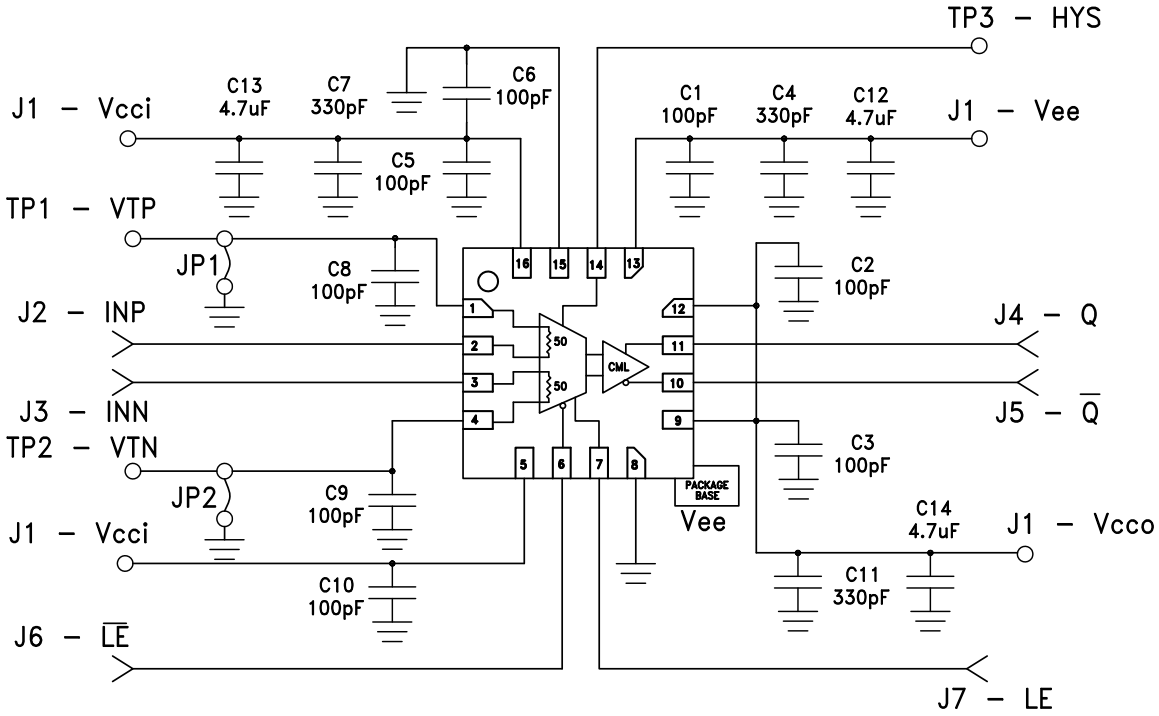
Item	Description
J1	8 Pos. Vertical TIN
J2 - J7	2.92 mm 40 GHz Jack
J8	Terminal Strip, Single Row 3 Pin SMT
JP1, JP2	2 Pos. Vertical TIN
C1 - C3, C5, C6, C8 - C10	100 pF Capacitor, 0402 Pkg.
C4, C7, C11	330 pF Capacitor, 0402 Pkg.
C11 - C13	4.7 µF Tantalum
TP1 - TP4	DC Pin, Swage Mount
U1	HMC675LP3E Comparator
PCB	125929 Evaluation PCB

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes in order to provide good RF grounding to 25 GHz. The evaluation circuit board shown is available from Hittite upon request.

Application Circuit



Notes: