Hittite MICROWAVE CORPORATION v00.0409

RoHS✓ EARTH FRIENDLY

HMC795LP5E

SiGe WIDEBAND DIRECT QUADRATURE MODULATOR w/ VGA, 50 - 2800 MHz

Typical Applications

The HMC795LP5E is ideal for:

- UMTS, GSM or CDMA Basestations
- Fixed Wireless or WLL
- ISM Transceivers, 900 & 2400 MHz
- GMSK, QPSK, QAM, SSB Modulators
- Cellular/3G and WiMAX/4G
- Microwave IFs

Features

High Linearity OIP3: + 22 dBm

High Output Power: +10 dBm Output P1dB

High Carrier Suppression: 55 dBc

High Sideband Suppression: 53 dBc

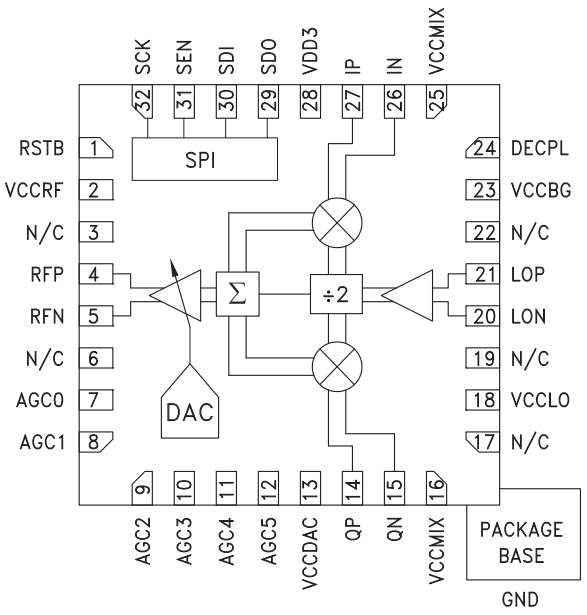
Read/Write Serial Port Interface (SPI)

SPI & 6-bit parallel port programmable 32 dB Gain Control

DC - 440 MHz Baseband Input

32 Lead 5x5 mm QFN Package: 25 mm^2

Functional Diagram



General Description

The HMC795LP5E is a variable gain, direct quadrature modulator ideal for digital modulation applications from 50 - 2800 MHz including: Cellular/3G, Broadband Wireless Access and ISM circuits. Housed in a compact 5x5mm (LP5) SMT QFN package, the modulator offers a high level of integration, exceptionally low carrier feedthrough, and a low cost alternative to more complicated double upconversion architectures.

The LO requires -9 to +3 dBm and can be driven in either differential or single-ended mode. The baseband inputs will support modulation inputs from DC - 440 MHz.

The differential RF output port is driven by a 6 bit digital controlled variable gain amplifier to nominally provide up to 32 dB of very linear gain control in 0.5 dB steps. The low carrier suppression is maintained over the VGA dynamic range. The gain control interface accepts either three wire serial input or 6 bit parallel word. In addition, the gain control can be modified through the SPI to adjust a look up table to control the gain step to as low as 0.1 dB, with reduced range, or to adjust individual gain steps for system linearization.

Electrical Specifications, See Test Conditions on Following Page

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
RF Frequency		1000			1950			2690		MHz
Output Power	8	9.5	11	7	9	11	4	8	11	dB
Output P1dB	13	14		9	11		9	11		dBm
Output IP3	23	25		18	22		17	22		dBm
Carrier Feedthrough (Uncal)	-40	-45		-42	-46		-42	-46		dBm
Carrier Feedthrough (Cal)	-55	-62		-55	-62		-52	-57		dBm
Sideband Suppression (Uncal)	43	55		49	53		45	50		dBc
Output Noise Floor @ 20 MHz offset		-158	-157		-156	-155		-154	-153	dBm/Hz
RF Return Loss	-10	-14		-10	-12		-10	-12		dB
LO Return Loss	-10	-15		-10	-15		-10	-12		dB

Electrical Specifications *(Continued)*

Parameter	Conditions	Min.	Typ.	Max.	Units
Gain Control Characteristics					
Gain Control Range		-31.5		0	dB
Gain Control Step	Can be adjusted with SPI		0.5		dB
State Error (at max Attenuation)			±0.5	±1	dB
Gain Step Error			±0.05	±0.13	dB
RF Input Characteristics					
RF Frequency Range		50		2800	MHz
RF Return Loss	Requires external matching	9	-15	-10	dB
RF Bandwidth	with matching specified in table	5	10	15	%
LO Input Characteristics					
LO Frequency Range		100		5600	MHz
LO Return Loss	Required 1 nF blocking cap			-10	dB
LO Drive Level		-9	0	+3	dBm
Baseband Inputs					
I/Q Input Bias Level	Output Power ±0.5 dB of Typ.	1.2	1.3	1.4	V
Input Bias Current			90		µA
Differential Input Impedance			5K||100pF		Ohms||pF
Bandwidth		DC		440	MHz
DC Power Requirements					
Analog Supply Voltage (VCCMIX, VCCBG, VCCRF, VCCDAC, VCCLO)	All must be equal	4.5	5	5.5	V
Digital Supply Voltage (VDD3)		3	3.3	3.5	V
IDD - Total Current Consumption		106	127	145	mA
Power Down Current				1	µA

Test Conditions: *Unless Otherwise Specified, the Following Test Conditions Were Used*

Parameter		Condition
Temperature		25 °C
VGA Attenuation		0 dB
Baseband Input Frequency		1 MHz
Baseband Input DC Voltage		1.3V
Baseband Input AC Voltage	(Peak to Peak Differential, I and Q)	1.4V
Baseband Input AC Voltage for OIP3 Measurement	(Peak to Peak Differential, I and Q)	290 mV per tone @ 1 & 1.5 MHz
Frequency Offset for Output Noise Measurements		20 MHz
Supply		Analog: +5V, Digital: +3.3V
LO Input Power		0 dBm
LO Input Mode		Differential
Sideband and Carrier Suppression		Uncalibrated
RF Output Mode		Differential

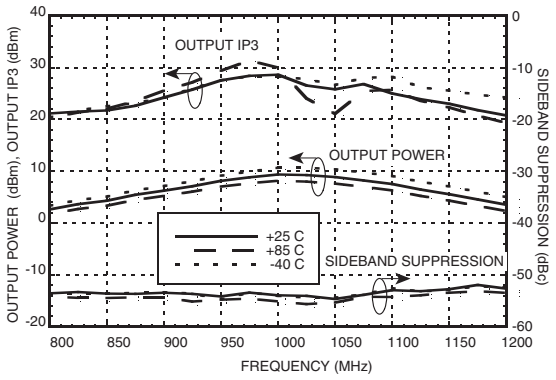
Calibrated vs. Uncalibrated Test Results

During the Uncalibrated Carrier Suppression tests, care is taken to ensure that the I/Q signal paths from the Vector Signal Generator (VSG) to the Device Under Test (DUT) are equal. The "Uncalibrated" Carrier Suppression plots were measured at T= -40 °C, +25 °C, and +85 °C.

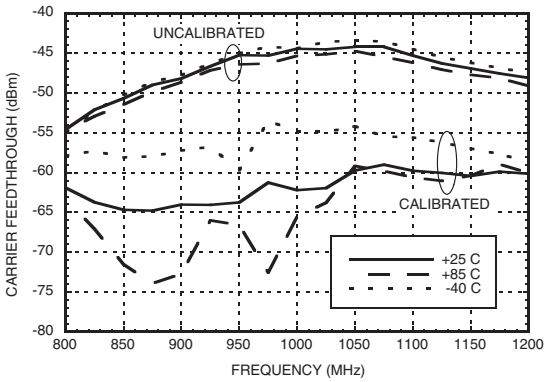
The "Calibrated" Carrier Suppression data was plotted after a manual adjustment of the IP/IN & QP/QN DC offsets at +25 °C, 5V Vcc, 0 dBm LO input power level, and the RF output frequency set to the midband of the measurement range. The adjustment settings were held constant during tests over temperature and frequency.

Typical Performance Characteristics, Vcc +5V, LO 0 dBm, +25 °C

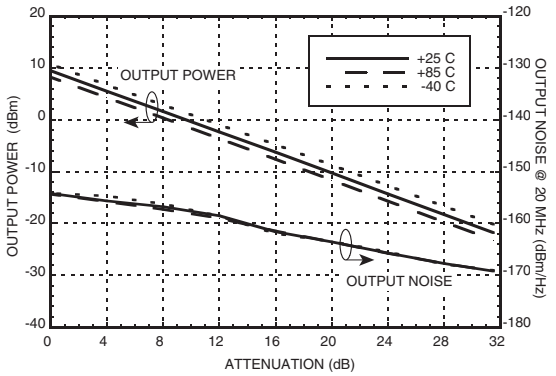
Output Power, Output IP3 & Sideband Suppression vs. Freq. over Temperature [1]



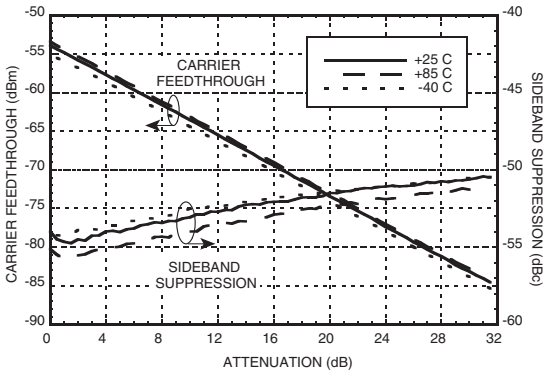
Uncalibrated & Calibrated Carrier Feedthrough vs. Freq. over Temperature [1]



Output Power & Output Noise @ 1 GHz vs. VGA Attenuation over Temperature [1]

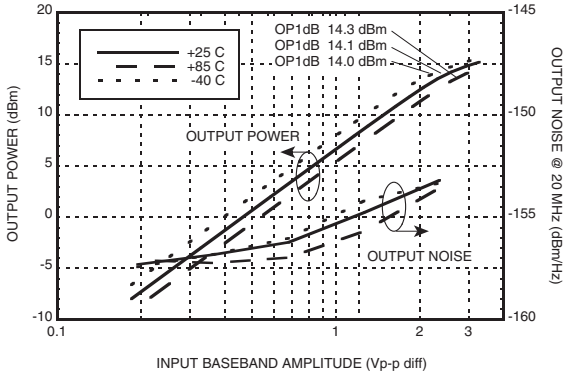


Carrier Feedthrough & Sideband Suppression @ 1 GHz vs. VGA Attenuation over Temperature [1]

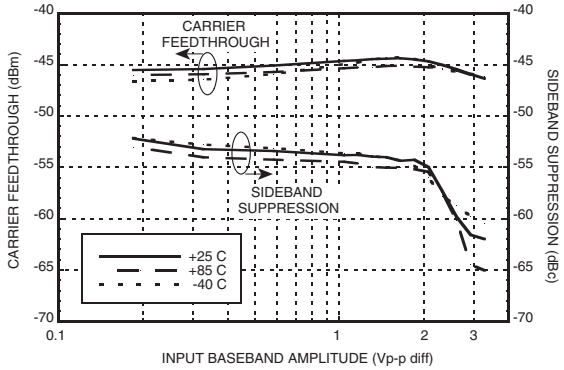


[1] Output Matched to 1 GHz

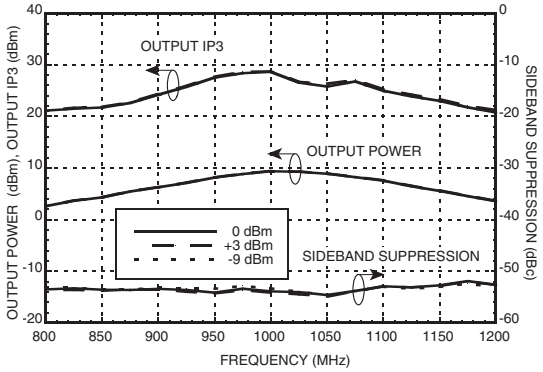
Output Power & Output Noise @ 1 GHz vs. Input Baseband Amplitude over Temperature [1]



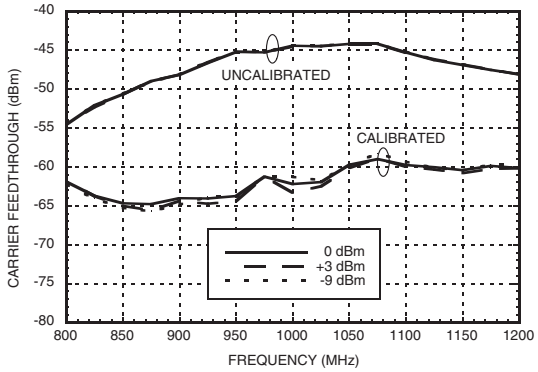
Carrier Feedthrough & Sideband Suppression @ 1 GHz vs. Input Baseband Amplitude over Temperature [1]



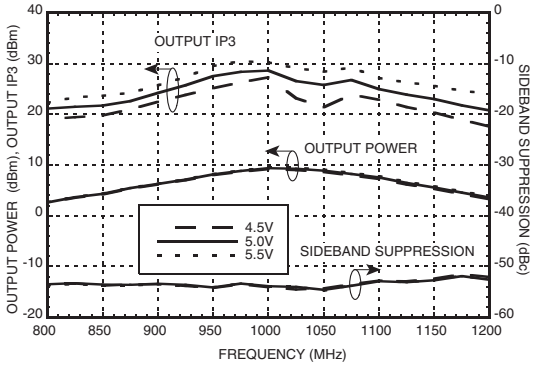
Output Power, Output IP3 & Sideband Suppression vs. Freq. over LO Power [1]



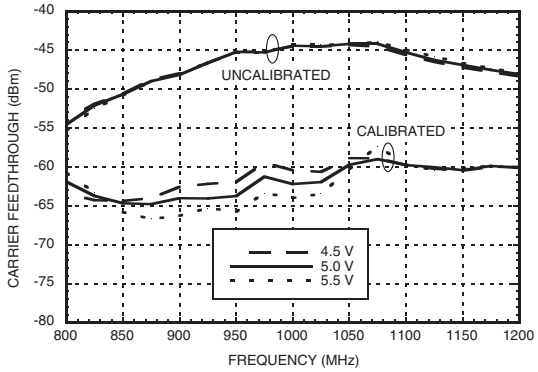
Uncalibrated & Calibrated Carrier Feedthrough vs. Freq. over LO Power [1]



Output Power, Output IP3 & Sideband Suppression vs. Freq. over Supply Voltage [1]

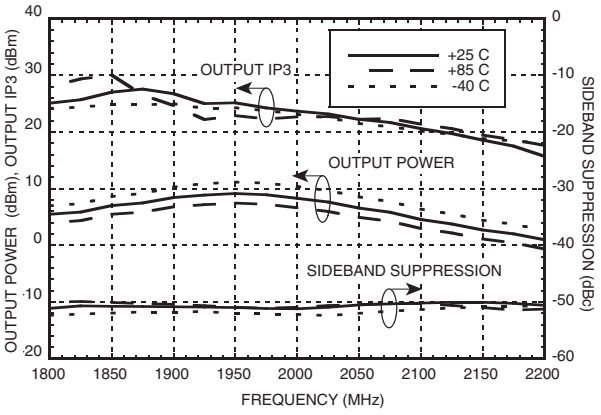


Uncalibrated & Calibrated Carrier Feedthrough vs. Freq. over Supply Voltage [1]

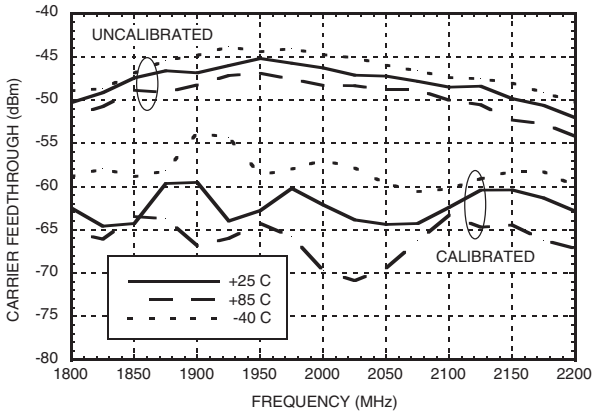


[1] Output Matched to 1 GHz

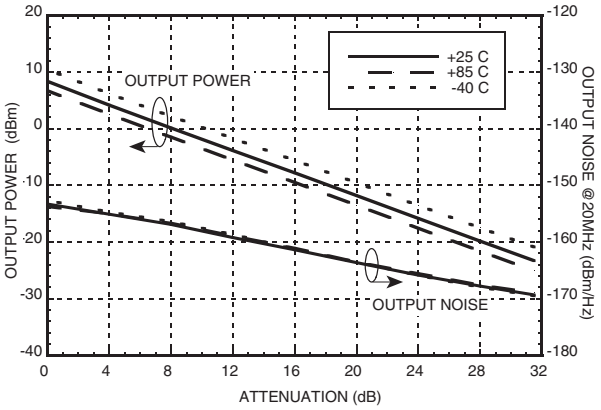
Output Power, Output IP3 & Sideband Suppression vs. Freq. over Temperature [1]



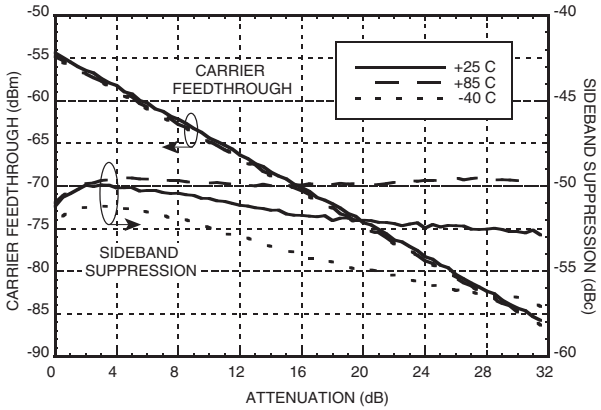
Uncalibrated & Calibrated Carrier Feedthrough vs. Freq. over Temperature [1]



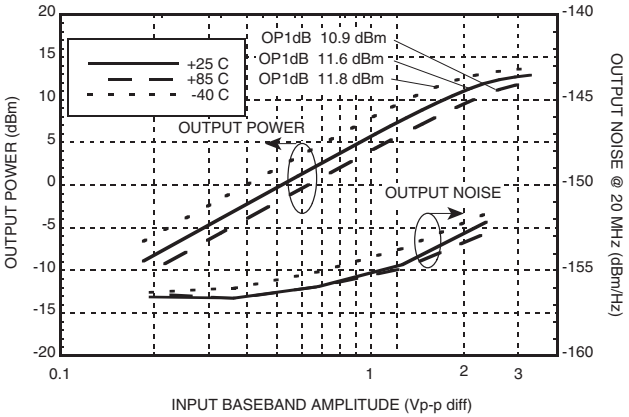
Output Power & Output Noise @ 1950 MHz vs. VGA Attenuation MHz over Temperature [1]



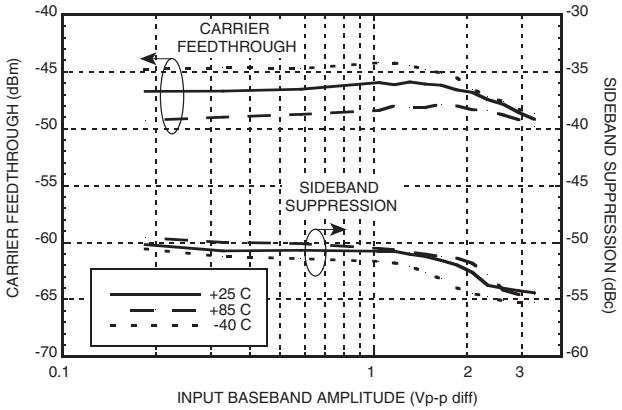
Carrier Feedthrough & Sideband Suppression @ 1950 MHz vs. VGA Attenuation over Temperature [1]



Output Power & Output Noise @ 1950 MHz vs. Input Baseband Amplitude over Temperature [1]

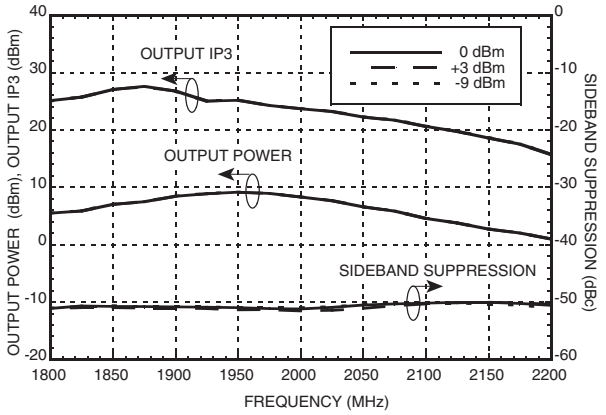


Carrier Feedthrough & Sideband Suppression @ 1950 MHz vs. Input Baseband Amplitude over Temperature [1]

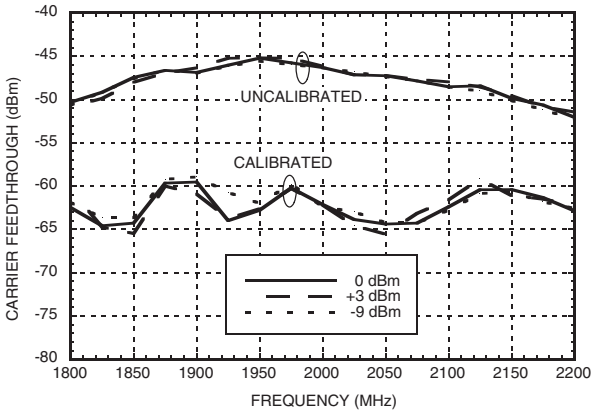


[1] Output Matched to 1950 MHz

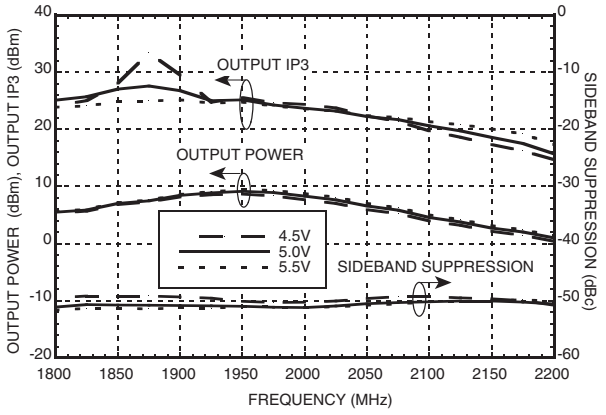
Output Power, Output IP3 & Sideband Suppression vs. Freq. over LO Power [1]



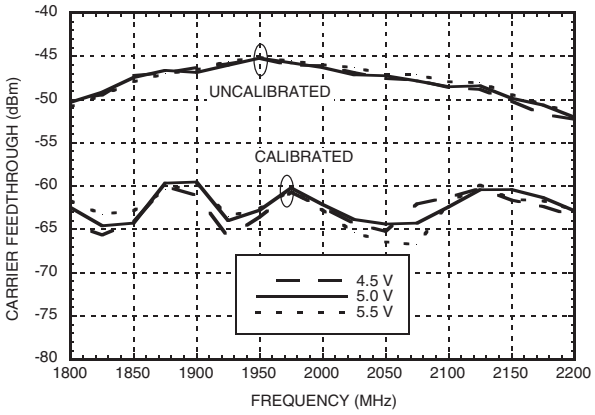
Uncalibrated & Calibrated Carrier Feedthrough vs. Freq. over LO Power [1]



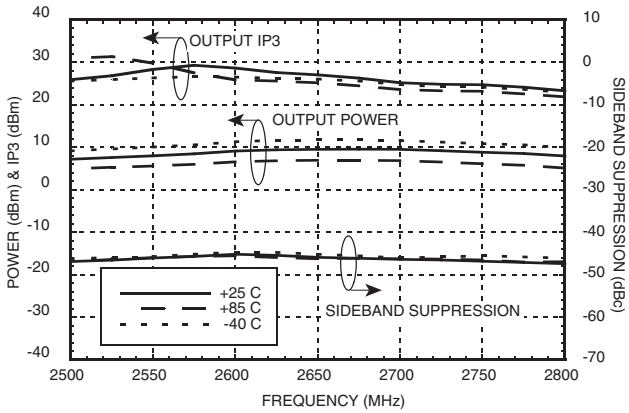
Output Power, Output IP3 & Sideband Suppression vs. Freq. over Supply Voltage [1]



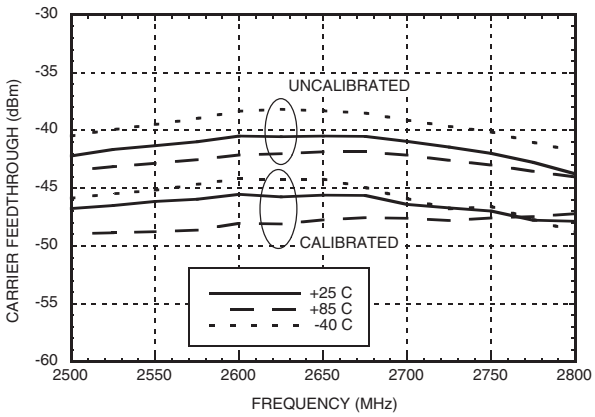
Uncalibrated & Calibrated Carrier Feedthrough vs. Freq. over Supply Voltage [1]



Output Power, Output IP3 & Sideband Suppression vs. Freq. over Temperature [2]



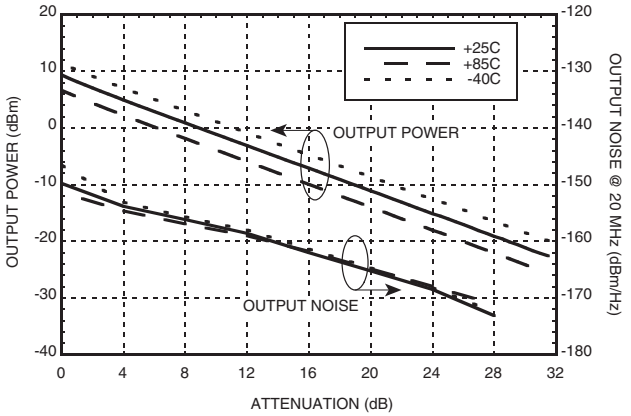
Uncalibrated & Calibrated Carrier Feedthrough vs. Freq. over Temperature [2]



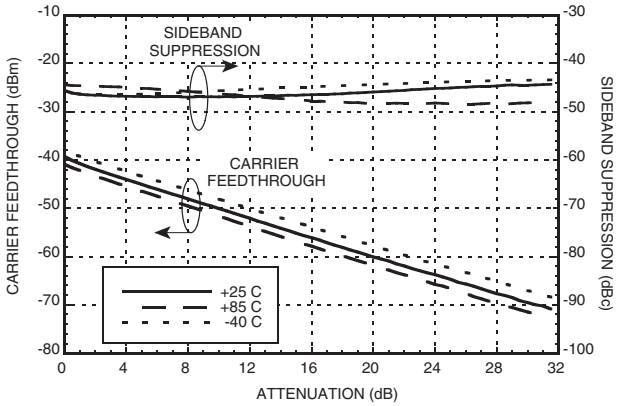
[1] Output Matched to 1950 MHz [2] Output Matched to 2690 MHz

SiGe WIDEBAND DIRECT QUADRATURE MODULATOR w/ VGA, 50 - 2800 MHz

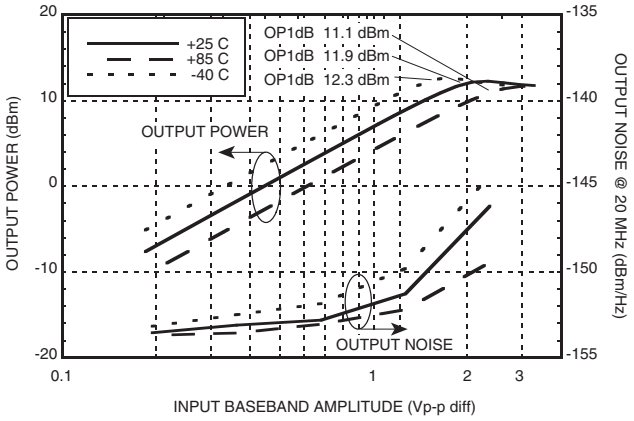
Output Power & Output Noise @ 2690 MHz vs. VGA Attenuation over Temperature [1]



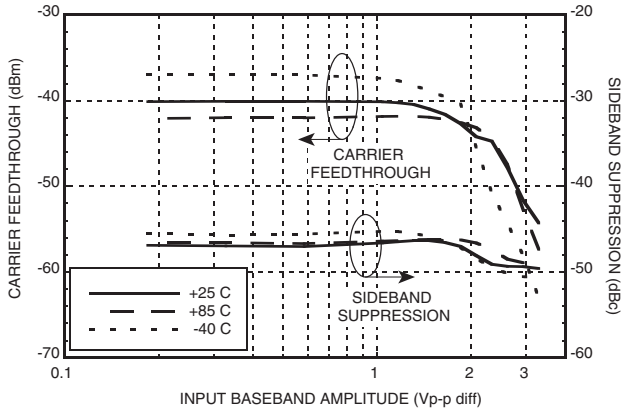
Carrier Feedthrough & Sideband Suppression @ 2960 MHz vs. VGA Attenuation over Temperature [1]



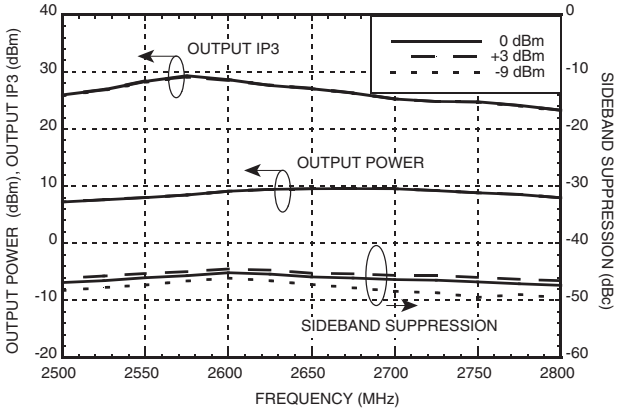
Output Power & Output Noise @ 2960 MHz vs. Input Baseband Amplitude over Temperature [1]



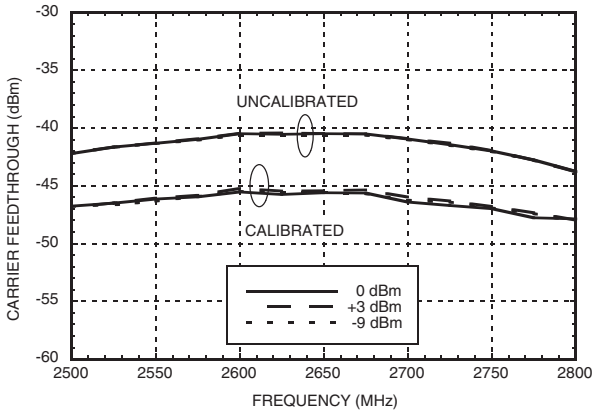
Carrier Feedthrough & Sideband Suppression @ 2960 MHz vs. Input Baseband Amplitude over Temperature [1]



Output Power, Output IP3 & Sideband Suppression vs. Freq. over LO Power [1]

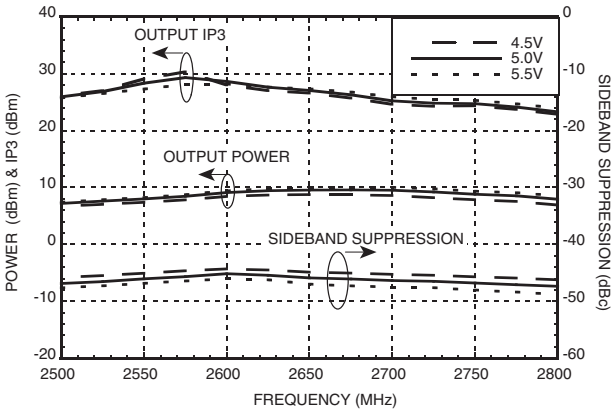


Uncalibrated & Calibrated Carrier Feedthrough vs. Freq. over LO Power [1]

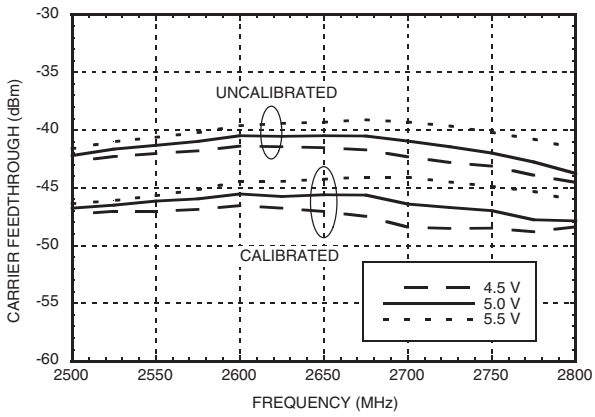


[1] Output Matched to 2960 MHz

Output Power, Output IP3 & Sideband Suppression vs. Freq. over Supply Voltage [1]

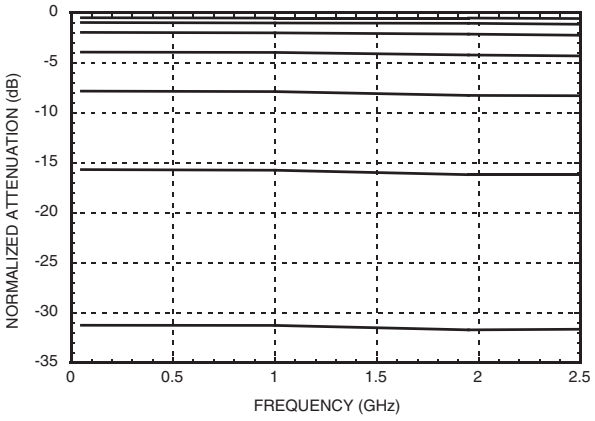


Uncalibrated & Calibrated Carrier Feedthrough vs. Freq. over Supply Voltage [1]



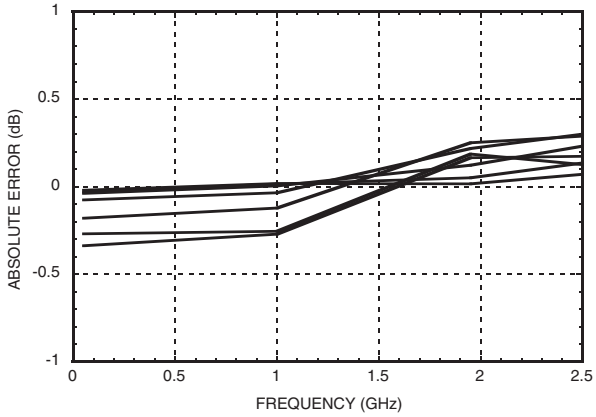
Normalized Attenuation vs. Frequency

(only Major States are Shown)

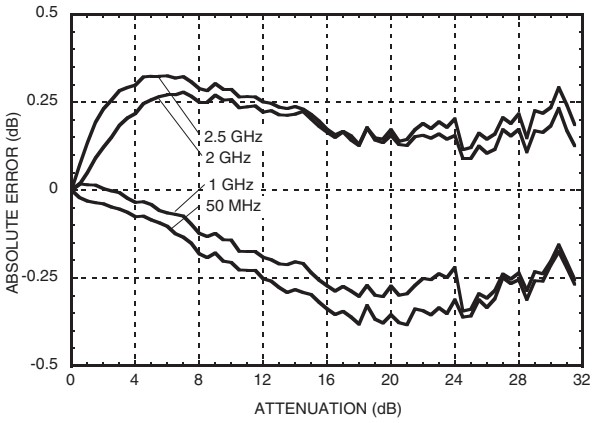


Absolute Error [2] vs. Frequency

(Only Major States are Shown)

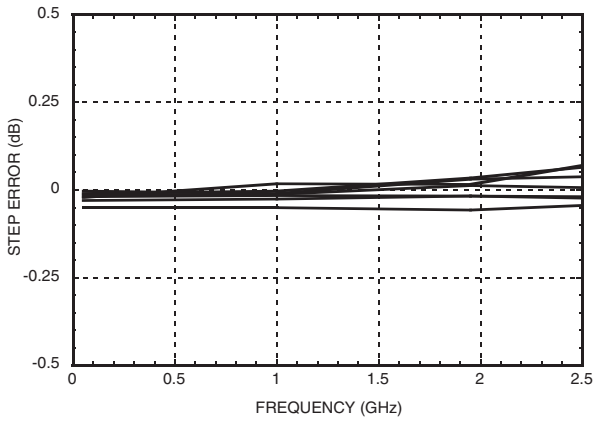


Absolute Error [2] vs. Attenuation State



Step Error [3] vs. Frequency

(Only Major States are Shown)

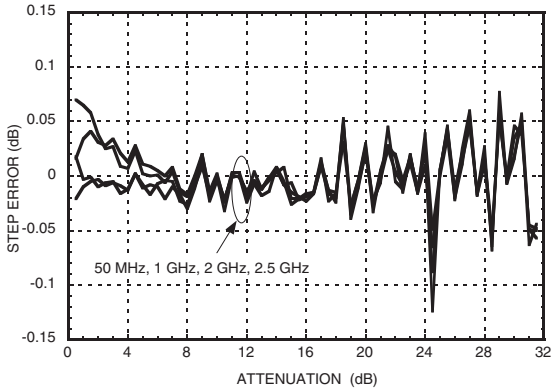


[1] Output Matched to 2960 MHz

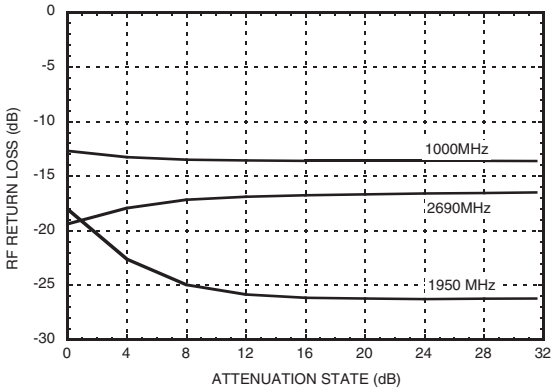
[2] Absolute error - difference between measured and ideal attenuation

[3] Step error - difference between measured attuation step and ideal step of 0.5 dB

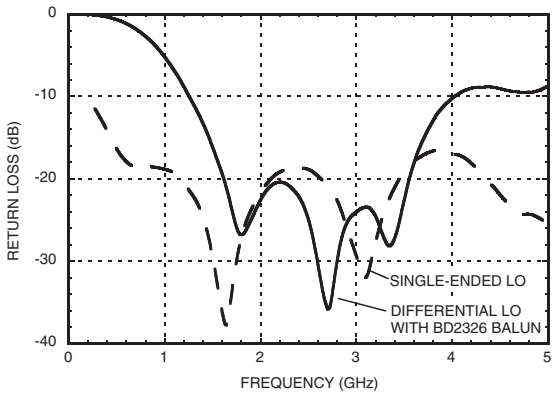
Step Error vs. Attenuation



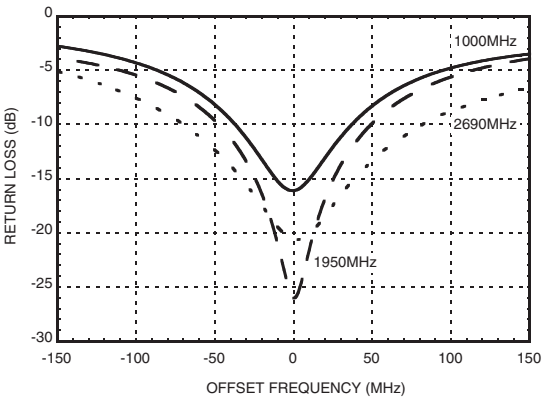
RF Return Loss vs. Attenuation



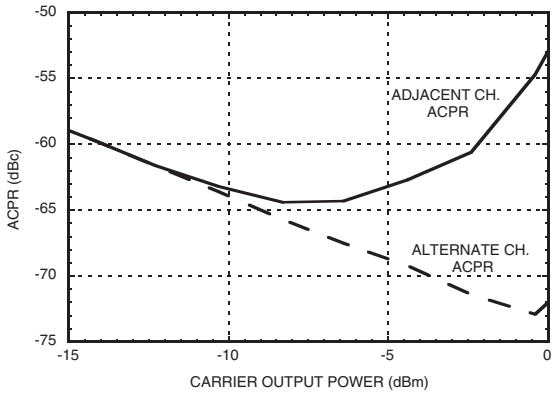
LO Return Loss vs. Frequency



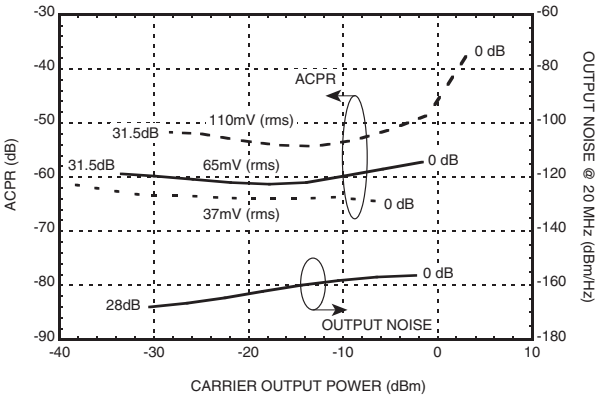
RF Return Loss vs. Frequency Offset, VGA Attenuation 0 dB



ACPR for W-CDMA @ 2140 MHz vs. Output Power for Various Input Levels, VGA Attenuation 0 dB [1]



ACPR for W-CDMA @ 2140 MHz vs. Output Power & VGA Attenuation for Various Input Levels [1]



[1] W-CDMA (Modulation Set-up for ACPR Mode): The baseband I and Q input signals were generated using “Test Model 1 with 64 channels

HMC795LP5E

SiGe WIDEBAND DIRECT QUADRATURE MODULATOR w/ VGA, 50 - 2800 MHz

Absolute Maximum Ratings

VCCMIX, VCCBG, VCCRF, VCCDAC	-0.3V to +5.5V
VDD3	-0.3V to +3.6V
LO Input Power	+18 dBm
Baseband Input Voltage (DC)	0V to +1.4V
Baseband Input Voltage (AC + DC)	0V to +1.8V
Maximum Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (derate 25 mW/°C above 85°C)	1W
Thermal Resistance (R_{th}) (junction to ground paddle)	40 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
Reflow Soldering Peak Temperature	260 °C
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

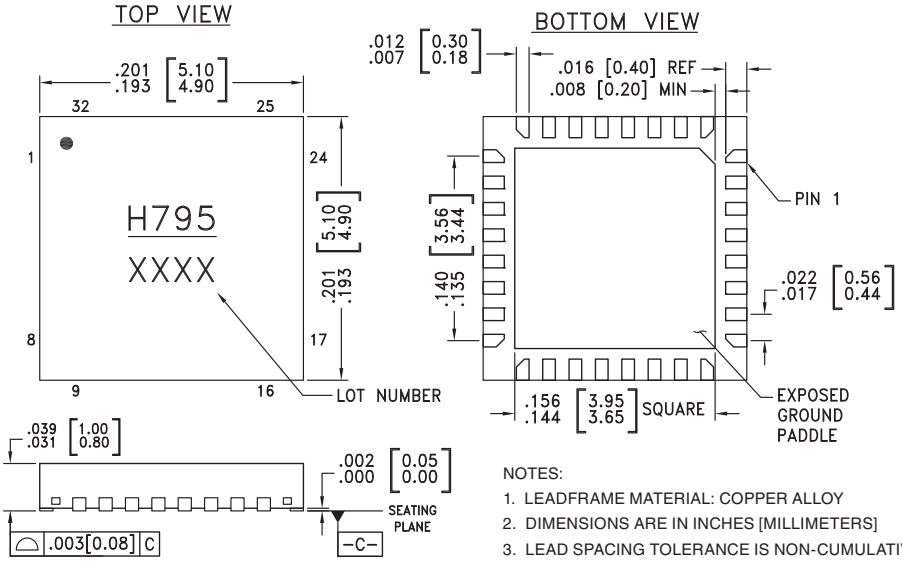
Truth Table

Control Voltage Input						Attenuation
AGC5	AGC4	AGC3	AGC2	AGC1	AGC1	
Low	Low	Low	Low	Low	Low	0 dB
Low	Low	Low	Low	Low	High	0.5 dB
Low	Low	Low	Low	High	Low	1 dB
Low	Low	Low	High	Low	Low	2 dB
Low	Low	High	Low	Low	Low	4 dB
Low	High	Low	Low	Low	Low	8 dB
High	Low	Low	Low	Low	Low	16 dB
High	High	High	High	High	High	31.5 dB

Any combination of the above states will provide an increase in the attenuation approximately equal to the sum of the bits selected

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



NOTES:

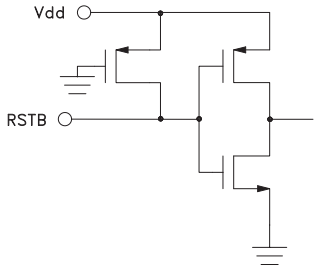
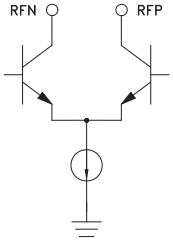
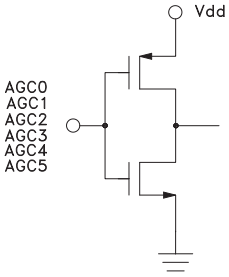
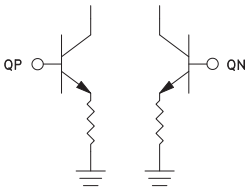
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS]
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED LAND PATTERN.

Package Information

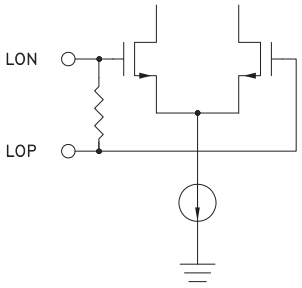
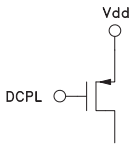
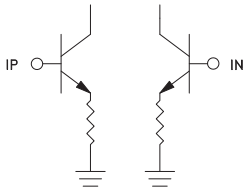
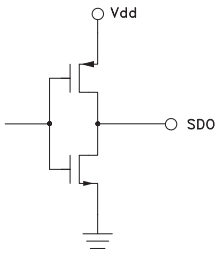
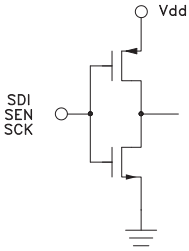
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC795LP5E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H795 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

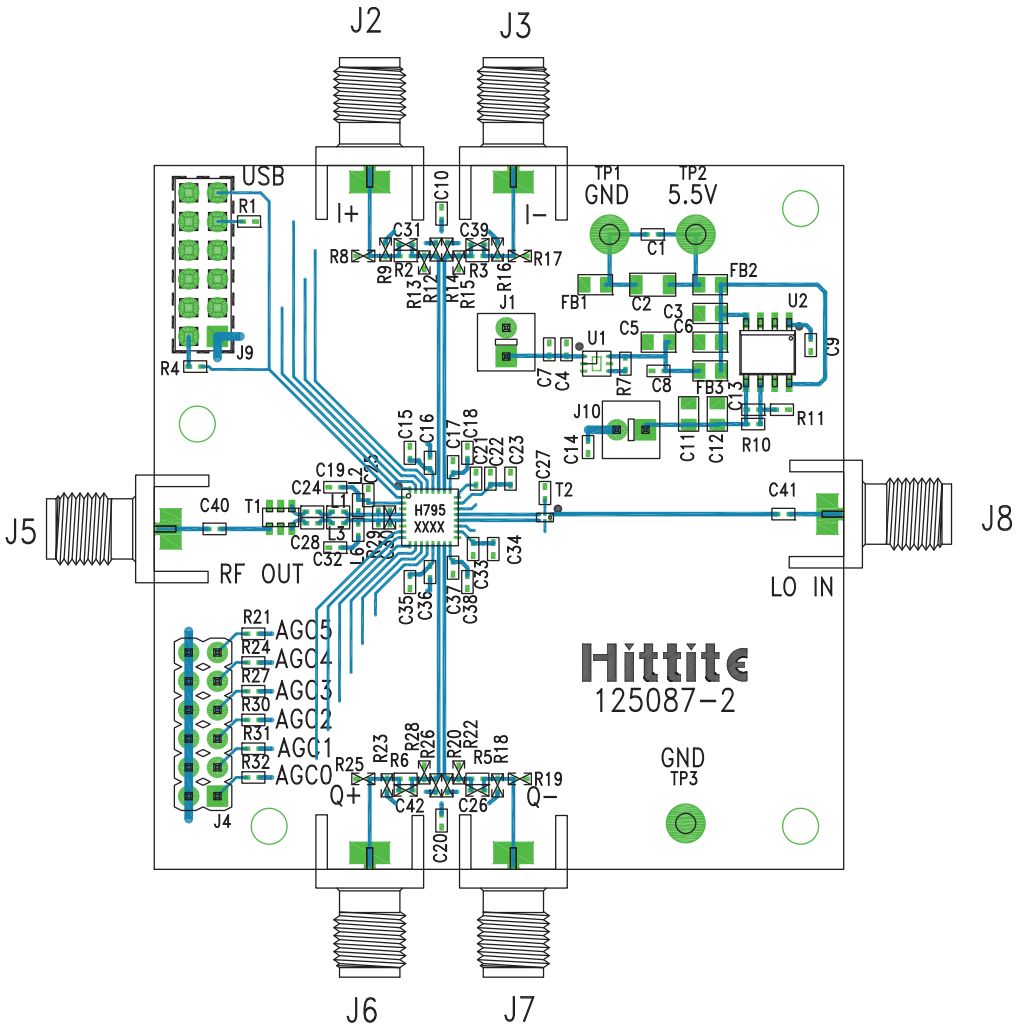
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1	RstB	Digital reset input, active low	
2	VCCRF	Supply voltage for the output driver, 5V, 24mA @ max gain, 0.7mA @ min gain	
3, 6, 19, 22	GND	These pins and the ground paddle should be connected to a high quality RF/DC ground.	
4, 5	RFN, RFP	Differential RF open collector output, needs pull up inductor to VCCRF and DC coupling capacitor on both pins, 5V, 0.5mA @min gain, 24.4mA @ max gain	
7, 8, 9, 10, 11, 12	AGC0, AGC1, AGC2, AGC3, AGC4, AGC5	Parallel binary input gain control word	
13	VCCDAC	Supply voltage for the DAC, 3.9mA @ 5V	
14, 15	QP, QN	Q channel differential baseband input. These high impedance ports should be biased at 1.3V. Nominal recommended baseband input is 1.4V pp differential	
16, 25	VCCMIX	Supply voltage for the I/Q mixers, 31.7mA @ 5V	
17	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.	
18	VCCLO	Supply voltage for the LO chain, 65.2mA @ 5V	

Pin Descriptions *(Continued)*

Pin Number	Function	Description	Interface Schematic
20, 21	LOP, LON	LO inputs. Need DC decoupling capacitors. The ports could be driven single ended or differentially	
23	VCCBG	Supply voltage for the bandgap, 4.3mA @ 5V	
24	DECOUPLE	External bypass decoupling for precision bias circuits, 3.80V NOTE: BIAS ref voltage cannot drive an external load. Must be measured with 10GOhm meter such as Agilent 34410A, normal 10Mohm DVM will read erroneously.	
26, 27	IN, IP	I channel differential baseband input. These high impedance ports should be biased at 1.3V. Nominal recommended baseband input is 1.4V pp differential	
28	VDD3	Supply voltage for the digital	
29	SDO	Main Serial port data output	
30	SDI	Main Serial port data input	
31	SEN	Main Serial port latch enable input	
32	SCK	Main Serial port clock input	

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

List of Materials for Evaluation PCB [1]

Item	Description
J1, J10	2 Pin DC Connector
J2, J3, J5 - J8	PCB Mount SMA Connector
J4	12 Pin DC Connector
J9	12 Pin Socket Connector
C1, C4, C8, C10, C14, C15, C18, C20, C23, C34, C35, C38	1 µF Capacitor, 0402 Pkg
C2	10 µF Capacitor, 1206 Pkg
C3, C5, C6, C11, C12	4.7 µF Capacitor, 0805 Pkg
C7, C16, C17, C22, C24, C25, C28, C33, C36, C37, C40	1 nF Capacitor, 0402 Pkg
C9, C21	10 nF Capacitor, 0402 Pkg
C13	1.2 nF Capacitor, 0402 Pkg
C19, C27, C32, C41	100 pF Capacitor, 0402 Pkg
C26, C30 - C31, C39, C42	Do Not Populate
R1, R4, R21, R24, R27, R30 - R32	100 kOhm Resistor, 0402 Pkg
R2, R3, R5, R6	0 Ohm Resistor, 0402 Pkg
R7	10 kOhm Resistor, 0402 Pkg
R8, R9, R12 - R20, R22, R23, R25, R26, R28, R29	Do Not Populate
R10	4 kOhm Resistor, 0402 Pkg
R11	1 kOhm Resistor, 0402 Pkg
T1, T2	RF Transformer
TP1 - TP3	DC Pin
FB1 - FB3	1 kOhms Ferrite Bead, 0805 Pkg
L1, L3	10 nH Inductor, 0402 Pkg
L2, L6	4.7 nH Inductor, 0402 Pkg
U1	Linear Regulator, 3.3V
U2	Linear Regulator, 5V
U3	HMC795LP5E Modulator
PCB [2]	125087 Eval Board

[1] When requesting an evaluation board, please reference the appropriate PCB number listed in the table “Components for the Selected Frequencies”

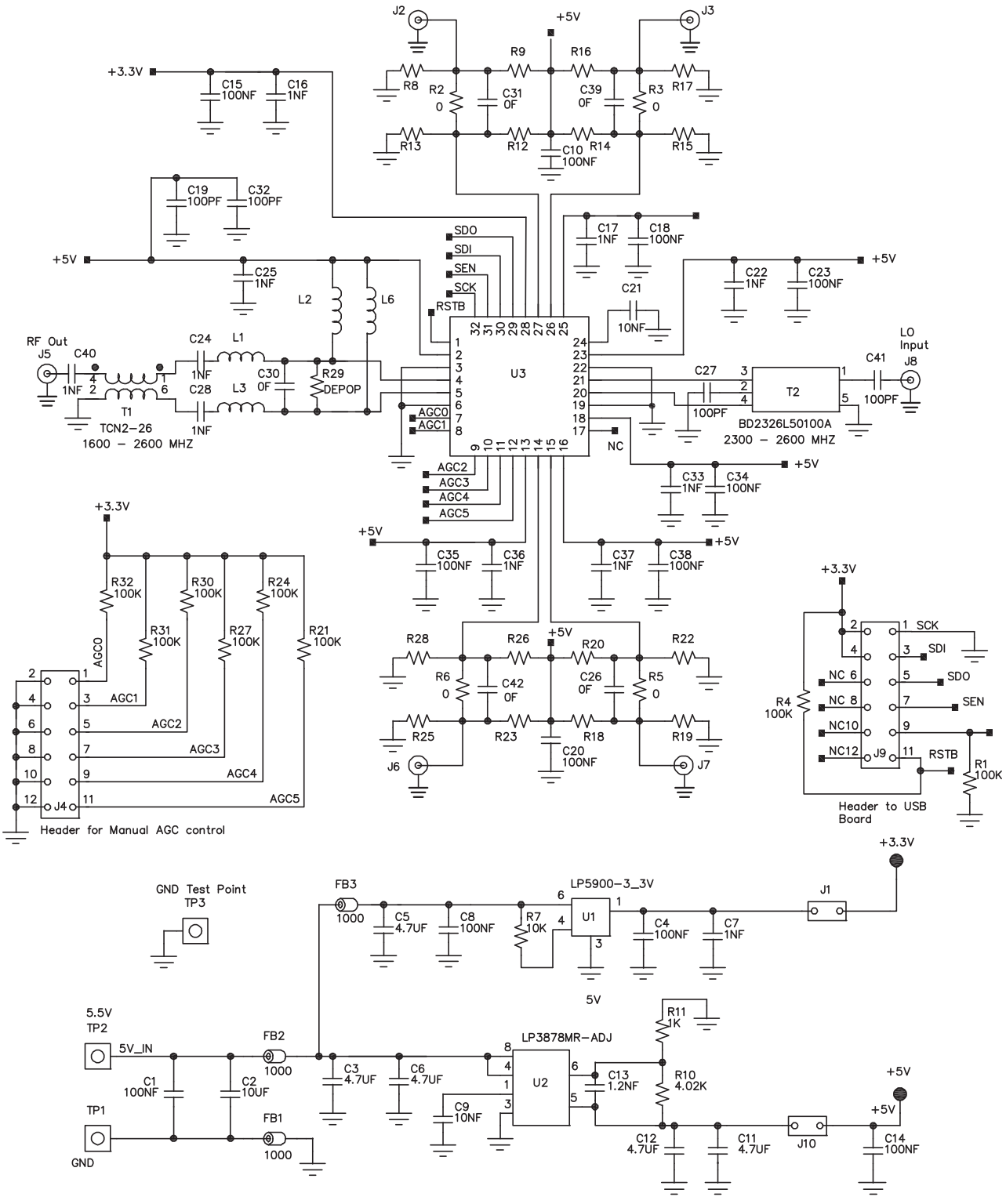
[2] Circuit Board Material: Arlon 25FR / FR4

Table 9. Components for Selected Frequencies

Tuned Frequency	850 MHz	1950 MHz	2960 MHz
Evaluation Board Number	127433	125370	130190
Evaluation Kit Number [1]	129934	129935	130186
L2, L6	47 nH	4.7 nH	1.8 nH
L1, L3	27 nH	10 nH	5.6 nH
R29	2.5 kOhms	DEPOP	DEPOP
T1	TCN2-14	TCN2-26	TCN2-26

[1] Evaluation Kit includes evaluation board, USB controller board, USB cable and evaluation software.

Application & Evaluation PCB Schematic



Theory of Operation

The HMC795LP5E modulator consists of the following functional blocks

1. LO Interface
2. I/Q modulator
3. Digitally controlled variable gain amplifier
4. Gain control DAC
5. Bias Circuit
6. Serial Port interface

LO Interface

The LO interface consists of a gain stage followed by a divide by 2 stage that generates two carrier signals in quadrature which are used to drive the mixers. As a result, the LO path is immune to large variations in the LO signal level and the modulator performance does not vary much with LO power. Due to the on chip divider, the input LO frequency must be twice that of the desired carrier frequency. This offers the advantage of significantly lowering carrier feedthrough.

The LO port can be driven differentially or single ended if the unused side is AC grounded. However, when driven single-endedly, the carrier feedthrough and sideband rejection can be degraded by either large 2nd order LO tones, such as when driven by a VCO with a divider output, or, by large half-harmonic tones, such as when driven by a VCO with a doubler output.

The LO interface can be enabled/disabled separately through the serial port interface using Reg01h <0> and can be used to disable the modulator output. The RF output signal is suppressed by 100 dB when only the LO interface is disable and the LO signal itself is suppressed approximately 60 dB. In addition, the LO buffer bias can be increased using Reg02h <7>. This setting is recommended for LO frequencies above 5 GHz.

I/Q Modulator

The HMC795LP5E has two double-balanced mixers, one for the in-phase channel and one for the quadrature channel. The differential baseband inputs (QP, QN, IP, and IN) consist of the bases of NPN transistors, which present a high impedance. The DC common mode voltage at the baseband inputs sets the currents in the two mixer cores. Varying the baseband common mode voltage varies the current in the mixers and affects the overall modulators performance. The recommended DC voltage for the baseband common mode voltage is 1.3V DC, ± 0.1V.

The output of the two mixers are summed together differentially and then used to drive the differential input of the VGA stage. The mixer can be enabled/disabled with Reg01h <1>. The external baseband DC bias also need to be disabled to completely disable the mixers. Disabling the mixer enables a weak pull down at the mixer inputs which connects the mixer inputs through a resistive path to ground. This may pull the external input low resulting in large current flow if the external bias is not disabled.

Digitally Controlled Variable Gain Amplifier

The output of the HMC795LP5E is a 6 bit, digitally controlled, variable gain amplifier that can provide very accurate linear- in-dB gain control over a 31.5 dB range in 0.5 dB steps. The VGA also provides relatively constant phase over the entire gain range, as shown in Figure 1. An 11 bit DAC is used to control the VGA. See the Gain Control DAC section for more detail about gain control.

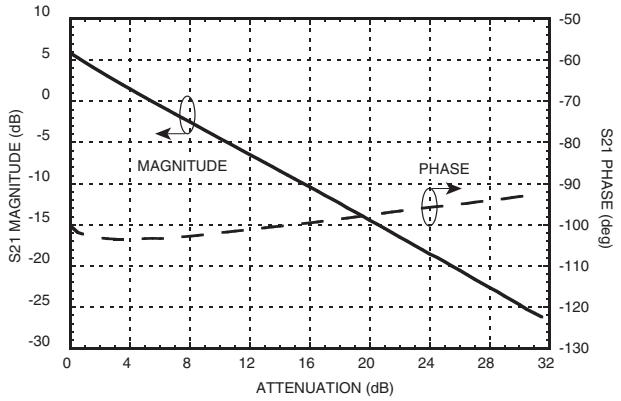


Figure 1. VGA S21 magnitude and phase @ 2 GHz vs attenuation

For maximum performance and flexibility, the output ports of the VGA are differential open collectors that require pull up inductors to the positive supply and external matching components. The evaluation board allows for several options for matching. See the Output Matching section for more details.

The VGA can be enabled/disabled separately through the SPI using Reg01h <2>. The ON/OFF isolation of the VGA is greater than 60 dB for RF output frequencies up to 2.5 GHz.

Gain Control DAC

An 11 bit DAC is used to control the VGA for linear-in-dB gain control, Figure 2 shows the control for the DAC.. The DAC is normally controlled by a look up table (LUT) that is in turn, controlled by the 6 bit parallel port. The values of the look up table are fixed to give 0.5 dB steps over a 31.5 dB gain range.

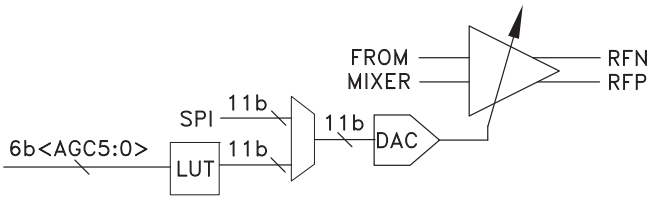


Figure 2. Simplified DAC control diagram

For increased flexibility, there are three methods to control the DAC and VGA gain.

1. **Parallel Mode** Use the 6 bit parallel port to provide fixed 0.5 dB gain steps. In this mode the DAC is controlled by a look up table with 64 states that map the 6 bit parallel port to fixed 11-Bit gain words for each state. The values of the LUT are fixed to give nominally 0.5 dB attenuation steps over a 31.5 dB gain range.

2. **Correction Mode** Use the SPI port in conjunction with the 6 bit parallel port to apply a 4 bit, 2's complement, correction factor to any attenuation step. This option can be used to compensate the gain control for systematic variations in the transmit chain by adding negative or positive correction factors to any of the fixed LUT values to either slightly increase or decrease the gain step for that particulate state. This mode requires the host controller to write the desired corrections to the SPI after the chip is powered up. The correction factors are then applied to the desired gain steps when ever the parallel port gain control changes, until the chip is powered down.

The 4 bit, 2's compliment, correction factor for each line in the LUT are set by Reg4h to Reg13h. The correction factor for 0 dB attenuation (line 0) is set in Reg4h <3:0>, 0.5 dB (line 1) is set by Reg4h <7:4>, 1.0 dB (line 2) by Reg4h<11:8> and so on until Reg13h <15:12> which sets the correction factor for 31.5 dB attenuation. If more adjustment is needed, the LUT correction values can be increased by a factor of 2, 3, or 4 times by using Reg2h <15:8>. Reg2h <9:8> sets the multiplication factor for the first quadrant of the LUT, lines 0 to 15, <11:10> for lines 16 to 31, <13:12> for lines 32 to 47 and <15:14> for the last quadrant, lines 48 to 63. The correction in dB can be estimated by

$$COR(dB) = 10 \cdot \log10 \left[\left(1 + \frac{(CORword \cdot mult)}{LUTword} \right)^{-1} \right]$$

where mult is the correction multiplication factor, and CORword and LUTword are the decimal equivalent of the binary correction and LUT word. An expression for determining the LUTword is given in the bypass mode section below. Figures 3, 4 and 5 show the range of correction in dB for 4 dB, 16 dB and 31.5 dB attenuation and Figure 6 shows the output power versus attenuation for no correction, maximum positive and maximum negative correction applied to all states in the LUT. The LUT value for 0 dB attenuation can only be decreased since it already at maximum. Increasing the word value will cause an overflow resulting in maximum attenuation instead.

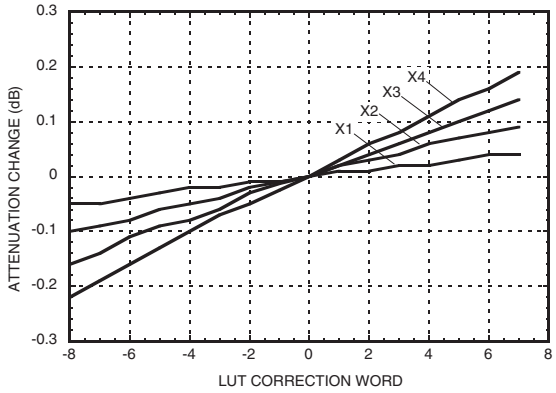


Figure 3. Attenuation Change from 4 dB Attenuation vs. LUT Correction Word over Different Multiplication Factors

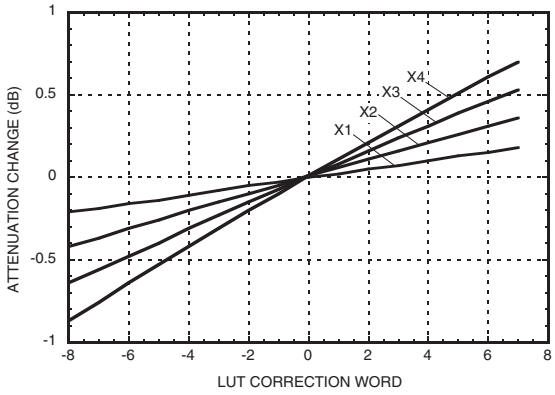


Figure 4. Attenuation Change from 16 dB Attenuation vs. LUT Correction Word over Different Multiplication Factors

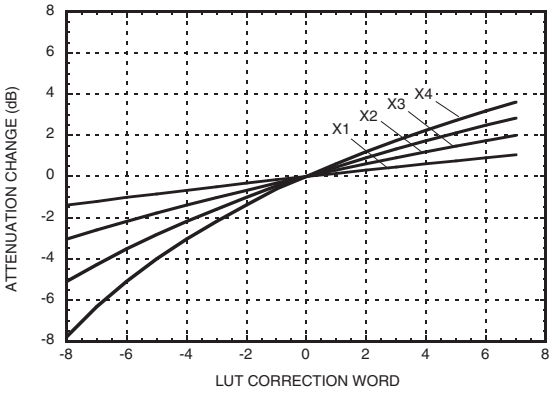


Figure 5. Attenuation Change from 31.5 dB Attenuation vs. LUT Correction Word over Different Multiplication Factors

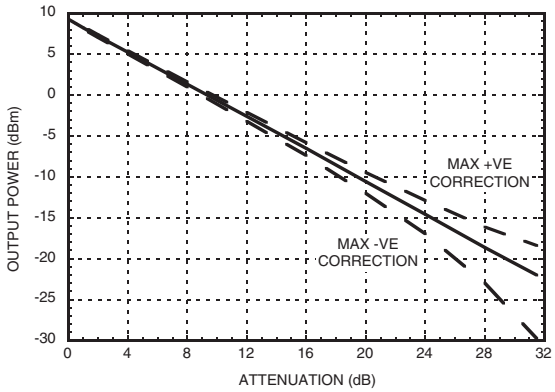


Figure 6. Output Power @ 850 MHz vs. VGA Attenuation for no Correction, Maximum Positive & Maximum Negative Correction Values

3. **Bypass Mode**. Use the SPI port to bypass the parallel port and LUT completely. In this mode Reg2h<4> is set to enable the bypass mode. The host controller can then write the desired gain word to the SPI using Reg3h<10:0> for each and every desired gain change. The input word can be determined from the desired gain (in dB) by

$$LUTword(10:0) = \text{dec2bin}[\text{round}[(2^{11} - 1) \cdot 10^{(-attn)/20}]]$$

and is plotted in Figure 7. In the this mode it is possible to use much lower attenuation steps over a reduced gain control range. The limit for reliable attenuation steps is 0.1 dB with a gain control range of approximately 22 dB.

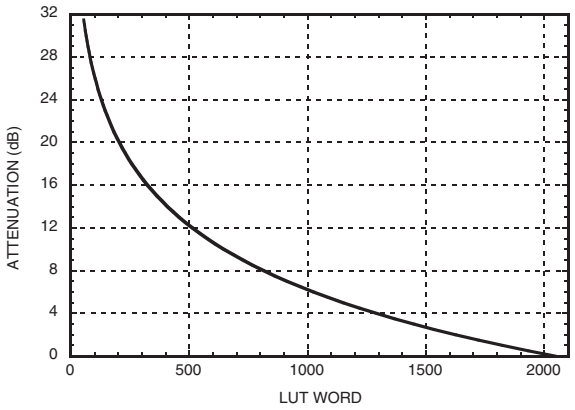


Figure 7. Attenuation vs. LUT word

The DAC can be enabled/disabled separately through the serial port interface using bit 3 of register 01h. Disabling the DAC will also disable the VGA.

For price, delivery, and to place orders, please contact Hittite Microwave Corporation:
20 Alpha Road, Chelmsford, MA 01824 Phone: 978-250-3343 Fax: 978-250-3373
Order On-line at www.hittite.com

Bias Circuit

A band gap reference circuit generates the reference currents used by the different sections. The bias circuit can be disabled with Reg01h <4>. Disabling the bias circuit will also disable the reference currents to all the other sections except the mixers, since they use an external bias. An external pin, pin 24, is also provided to allow for external decoupling for low noise performance, 100nF is recommended.

Power on Reset and Soft Reset

The HMC795LP5E features a hardware Power On Reset (POR). All chip registers will be reset to default states approximately 250 us after power up. The SPI registers may also be hardware reset by holding RSTB, pin 1, low, or software reset by writing 80h to Reg00h followed by writing 00h to Reg00h.

Serial Port Interface

The HMC795LP5E features a four wire serial port for simple communication with the host controller. Register types may be Read Only, Write Only, or Read/Write, as described in the registers descriptions. Typical serial port operation can be run with SCK at speeds up to 50 MHz. The HMC795LP5E chip address is fixed as “4d” or “100b”.

Serial Port WRITE Operation

A typical WRITE cycle is shown in Figure 8. It is 40 clock cycles long.

1. The host both asserts SEN (active low Serial Port Enable) and places the MSB of the data on SDI followed by a rising edge on SCLK.
2. HMC795LP5E reads SDI on the 1st rising edge of SCLK after SEN.
3. HMC795LP5E registers the data bits in the next 29 rising edges of SCLK.
4. Host places the seven register address bits on the next seven falling edges of SCLK, MSB first.
5. HMC795LP5E registers the register address bits in the next seven rising edges of SCLK.
6. Host places the 3 chip address bits <100> on the next 3 falling edges of SCLK, MSB first.
7. HMC795LP5E registers the chip address bits in the next 3 rising edges of SCLK.
8. SEN is de-asserted on the 40th falling edge of SCLK. This completes the WRITE cycle.
9. HMC795LP5E also exports data back on the SDO line. For details see the section on READ operation.

The host changes the data on the falling edge of SCLK and the HMC795LP5E reads the data on the rising edge.

Serial Port READ Operation

The SPI can read from the internal registers in the chip. The data is available on SDO line. This line itself is tri-stated after power up. After a WRITE cycle, the HMC795LP5E controls the SDO line and exports data on this line during the current WRITE cycle. The HMC795LP5E chip address is fixed as ‘4d’ or ‘100b’

A READ operation is always preceded by a WRITE operation to Register 0 to define the register to be queried. Every READ cycle is also a WRITE cycle in that data sent to the SPI while reading the data will also be stored by the HMC795LP5E when SEN goes high. If this is not desired then it is suggested to write to Register 0 during the READ operation as the status of the device will be unaffected.

A typical READ cycle is also shown in Figure 8. A read cycle is 40 clock cycles long. To specifically read a register, the address of that register must be written in the register 0. A read cycle can then be initiated as follows;

1. The host asserts SEN (active low Serial Port Enable) followed by a rising edge SCLK.
2. HMC795LP5E reads SDI (the MSB) on the 1st rising edge of SCK after SEN.

3. HMC795LP5E registers the data bits in the next 29 rising edges of SCLK (total of 30 data bits). The LSBs of the data bits represent the address of the register that is intended to be read.
4. Host places the 7 register address bits on the next 7 falling edges of SCLK (MSB to LSB) while the HMC795LP5E reads the address bits on the corresponding rising edge of SCK. For a read operation this is “0000000”.
5. Host places the 3 chip address bits <100> on the next 3 falling edges of SCK (MSB to LSB). Note the HMC795LP5E chip address is fixed as “4d” or “100b”.
6. SEN goes from low to high after the 40th rising edge of SCK. This completes the first portion of the READ cycle.
7. The host asserts SEN (active low Serial Port Enable) followed by a rising edge SCLK.
8. HMC795LP5E places the 30 data bits, 7 address bits, and 3 chip id bits on the SDO on each rising edge of the SCK commencing with the first rising edge beginning with MSB.
9. The host de-asserts SEN (i.e. sets SEN high) after reading the 40 bits from the SDO output. The 32 bits consists of 30 data bits, 7 address bits, and the 3 chip id bits. This completes the READ cycle.

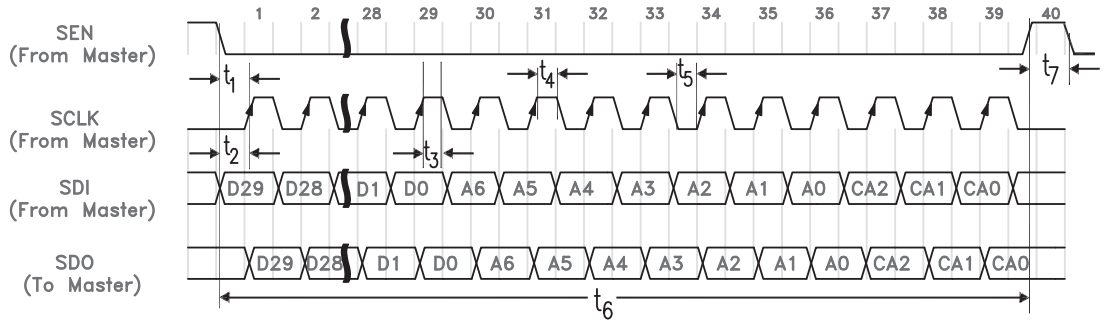


Figure 8. SPI Timing Diagram for write and read operation

Main SPI Timing Characteristics *DVDD = +3.3V ±10%, GND = 0V*

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SEN to SCK setup time	8			nsec
t_2	SDI to SCK setup time	8			nsec
t_3	SDI to CLK hold time	8			nsec
t_4	SCK high duration	8			nsec
t_5	SCK low duration	8			nsec
t_6	SEN low duration after 40th CLK	20			nsec
t_7	SEN high duration	20			nsec

Output Matching

The output ports of the VGA are differential open collectors that require pull up inductors to the positive supply and external matching components. The evaluation board uses a 2:1 impedance transformer to convert the differential output to single ended for evaluation purposes. Three options are available for the evaluation board, each with different matching components, one for 850 MHz, one for 1950 MHz, and another for 2690 MHz. When requesting an evaluation board, please reference the appropriate PCB number listed in the table "Components for the Selected Frequencies"

There are a number of ways to match the RF output of the HMC795LP5E for optimum performance. The most basic method is to use a 50 Ω resistor to Vcc and a 1 nF dc bypass capacitor connected in series as shown Figure 9(a). This option provides a good broadband match, see Figure 10, but limits the maximum output power, compared to a narrow band match, see Figure 11. Single-ended operation is possible by using a transformer, which can limit the bandwidth, as seen in the output power plot, or by using only one side of the differential output. However, biasing for the unused side is still required. For best performance it is recommended to terminate the unused side with the same matching and load impedance as the used side, see Figure 9(b). Output power is generally reduced by 2 to 3 dB for single-ended operation, as shown in Figure 11.

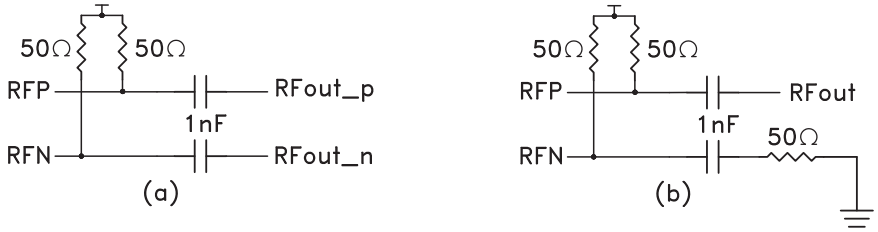


Figure 9. Simple output matching network

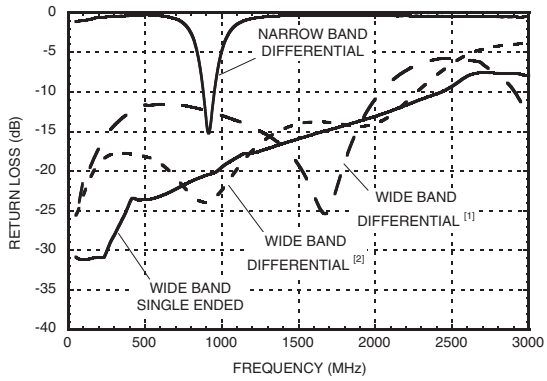


Figure 10. Output Return Loss for Various Matching Options

[1] With TCN2-14 Transformer

[2] With TCN2-26 Transformer

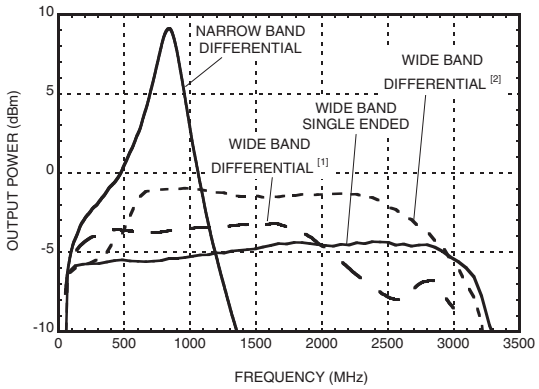


Figure 11. Output Power for Various Matching Options

[1] With TCN2-14 Transformer

[2] With TCN2-26 Transformer

A narrow band solution, with higher output power, is possible by using a simple L-match network, as shown in Figure 12. A shunt resistor is included to control the Q of the matching network and sets the output power of the HMC795LP5E. Consequently a low value resistor will result in a broadband match but lower output power than a high value resistor. The table below provides recommend component values for various output frequencies with a bandwidth of approximately 5-10%. It is also possible to use an LC matching network where L2 is removed and the DC blocking capacitor is used as a matching component. Experiments show that the output power is reduced approximately 1 -2 dB though and that values for the capacitors become unrealistic (< 500 fF) above 2 GHz.

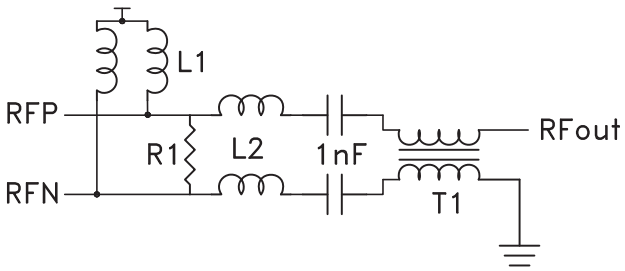


Figure 12. Simple output matching network

Recommending Matching Components

	450 MHz	850 MHz	1450 MHz	1850 MHz	1950 MHz	2400 MHz	2500 MHz	2690
L1	270 nH	47 nH	12 nH	5.6 nH	4.7 nH	2.7 nH	2.2 nH	1.8 nH
L2	82 nH	27 nh	12 nH	12 nH	10 nH	6.8 nH	5.6 nH	5.6 nH
R1	-	2.4K	2.4K	-	-	-	-	-
T1	Bypassed	TCN2-14	TCN2-14	TCN2-26	TCN2-26	TCN2-26	TCN2-26	TCN2-26

DAC Modulator Interface Network

The HMC795LP5Eis capable of interfacing with a variety of popular D/A Convertors. Most DAC have differential outputs with a source or sink current of 0 mA to 20 mA. However, most DACs require a different output compliance voltage than that of the DC input bias level for the HMC795LP5E. A passive interface network can be used to transform the common-mode voltage of the DAC to the desired DC input bias of the modulator of 1.3V. Figures 13 and 14 show the interface network for two different topologies.

1. Topology 1. DAC Vcm > HMC795LP5E Vcm. This topology is used shift the DAC output common mode voltage down to the required DC level at the modulator input.

2. Topology 2. DAC Vcm < HMC795LP5E Vcm. This topology is used shift the DAC output common mode voltage up to the required DC level at the modulator input.

The resistive level-shifting network is not frequency sensitive but the resistive divider network inherent in the network attenuates the baseband signal. The bypass capacitors shown Figures 13 and 14 will eliminate the attenuation for frequencies greater than 3 kHz. Either topology can be used on the HMC795LP5E evaluation board.

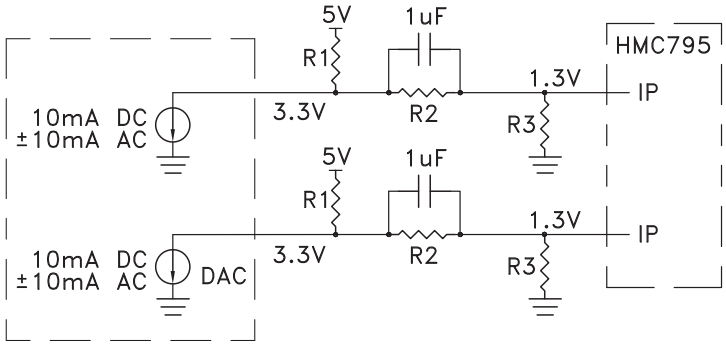


Figure 13. DAC Interface network topology 1

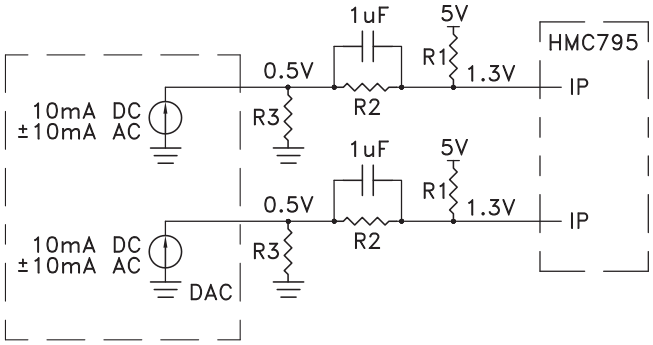


Figure 14. DAC Interface network topology 2

DAC Interface Network Values

	Topology 1	Topology 2
DAC Vcm	3.3	0.5
R1	62 Ω	36 Ω
R2	130 Ω	200 Ω
R3	82 Ω	910 Ω

Register Map

Reg 01h - Enable / Control Register

Bit	Name	Width	Default	Description
[0]	enLO	1	1	enables LO path
[1]	enMix	1	1	enables Mixer LO bias - see I/Q modulator section for more detail
[2]	enDrvr	1	1	enables output driver
[3]	enDAC	1	1	enables gain control DAC
[4]	enBias	1	1	enables bandgap and bias

Reg 02h - Function Register

Bit	Name	Width	Default	Description
[1:0}	Reserved	2	00	Reserved
[3:2]	Reserved	2	00	Reserved
[4]	LUT Bypass	1	0	Allows direct control of the gain control DAC via the DAC word in Reg03
[6:5]	Reserved	2	00	Reserved
[7]	LO Buffer Bias	1	0	Increases the LO buffer bias current by approximately 7.5mA
[9:8]	mult_0	2	00	Multiplication factor for correction to attenuation settings 0 to 7.5dB 00: x1 (default) 01: x2 10: x3 11: x4

Reg 02h - Function Register

Bit	Name	Width	Default	Description
[11:10]	mult_1	2	00	Multiplication factor for lines 16 - 31 of LUT (2nd Quadrant) 00: x1 (nom) 01: x2 10: x3 11: x4
[13:12]	mult_2	2	00	Multiplication factor for correction to attenuation settings 16 to 23.5dB 00: x1 (default) 01: x2 10: x3 11: x4
[15:13]	mult_3	2	00	Multiplication factor for correction to attenuation settings 24 - 31.5dB 00: x1 (default) 01: x2 10: x3 11: x4
[17:16]	Reserved	2	00	Reserved
[21:18]	Reserved	4	0000	Reserved

Reg 03h - Gain Control

Bit	Name	Width	Default	Description
[10:0]	idac	11	000h	Gain control DAC input word. LUT bypass bit in register 2h must be enabled. Gain control DAC word consists of an 11bit input word where 7FFh is maximum gain and 36h corresponds to minimum gain. Neglecting DAC error, the input word can be determined from the desired gain (in dB) as follows: idac<10:0>=dec2bin(round((2^(11) 1)*10^(gain/20)))

Reg 04h - LUT Correction 0 - 3

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 0 -15 (attenuation 0 to 7.5 dB) is set in Reg2 by bits mult_0 [9:8]

Bit	Name	Width	Default	Description
[3:0]	LUT_0	4	0000	2's complement 4bit correction to LUT line 0 (attenuation 0 dB)
[7:4]	LUT_1	4	0000	2's complement 4-bit correction to LUT line 1 (attenuation 0.5 dB)
[11:8]	LUT_2	4	0000	2's complement 4-bit correction to LUT line 2 (attenuation 1 dB)
[15:12]	LUT_3	4	0000	2's complement 4-bit correction to LUT line 3 (attenuation 1.5 dB)

Reg 05h - LUT Correction 4 - 7

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 0 -15 (attenuation 0 to 7.5 dB) is set in Reg2 by bits mult_0 [9:8]

Bit	Name	Width	Default	Description
[3:0]	LUT_4	4	0000	2's complement 4-bit correction to LUT line 4 (attenuation 2 dB)
[7:4]	LUT_5	4	0000	2's complement 4-bit correction to LUT line 5 (attenuation 2.5 dB)
[11:8]	LUT_6	4	0000	2's complement 4-bit correction to LUT line 6 (attenuation 3 dB)
[15:12]	LUT_7	4	0000	2's complement 4-bit correction to LUT line 7 (attenuation 3.5 dB)

Reg 06h - LUT Correction 8 - 11

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 0 -15 (attenuation 0 to 7.5 dB) is set in Reg2 by bits mult_0 [9:8]

Bit	Name	Width	Default	Description
[3:0]	LUT_8	4	0000	2's complement 4-bit correction to LUT line 8 (attenuation 4 dB)
[7:4]	LUT_9	4	0000	2's complement 4-bit correction to LUT line 9 (attenuation 4.5 dB)
[11:8]	LUT_10	4	0000	2's complement 4-bit correction to LUT line 10 (attenuation 5 dB)
[15:12]	LUT_11	4	0000	2's complement 4-bit correction to LUT line 11 (attenuation 5.5 dB)

Reg 07h - LUT Correction 12 - 15

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 0 -15 (attenuation 0 to 7.5 dB) is set in Reg2 by bits mult_0 [9:8]

Bit	Name	Width	Default	Description
[3:0]	LUT_12	4	0000	2's complement 4-bit correction to LUT line 12 (attenuation 6 dB)
[7:4]	LUT_13	4	0000	2's complement 4-bit correction to LUT line 13 (attenuation 6.5 dB)
[11:8]	LUT_14	4	0000	2's complement 4-bit correction to LUT line 14 (attenuation 7 dB)
[15:12]	LUT_15	4	0000	2's complement 4-bit correction to LUT line 15 (attenuation 7.5 dB)

Reg 08h - LUT Correction 16 - 19

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 16 - 31 (attenuation 8 to 15.5 dB) is set in Reg2 by bits mult_0 [11:10]

Bit	Name	Width	Default	Description
[3:0]	LUT_16	4	0000	2's complement 4-bit correction to LUT line 16 (attenuation 8 dB)
[7:4]	LUT_17	4	0000	2's complement 4-bit correction to LUT line 17 (attenuation 8.5 dB)
[11:8]	LUT_18	4	0000	2's complement 4-bit correction to LUT line 18 (attenuation 9 dB)
[15:12]	LUT_19	4	0000	2's complement 4-bit correction to LUT line 19 (attenuation 9.5 dB)

Reg 09h - LUT Correction 20 - 23

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 16 - 31 (attenuation 8 to 15.5 dB) is set in Reg2 by bits mult_0 [11:10]

Bit	Name	Width	Default	Description
[3:0]	LUT_20	4	0000	2's complement 4-bit correction to LUT line 20 (attenuation 10 dB)
[7:4]	LUT_21	4	0000	2's complement 4-bit correction to LUT line 21 (attenuation 10.5 dB)
[11:8]	LUT_22	4	0000	2's complement 4-bit correction to LUT line 22 (attenuation 11 dB)
[15:12]	LUT_23	4	0000	2's complement 4-bit correction to LUT line 23 (attenuation 11.5 dB)

Reg 0Ah - LUT Correction 24 - 27

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 16 - 31 (attenuation 8 to 15.5 dB) is set in Reg2 by bits mult_0 [11:10]

Bit	Name	Width	Default	Description
[3:0]	LUT_24	4	0000	2's complement 4-bit correction to LUT line 24 (attenuation 12 dB)
[7:4]	LUT_25	4	0000	2's complement 4-bit correction to LUT line 25 (attenuation 12.5 dB)
[11:8]	LUT_26	4	0000	2's complement 4-bit correction to LUT line 26 (attenuation 13 dB)
[15:12]	LUT_27	4	0000	2's complement 4-bit correction to LUT line 27 (attenuation 13.5 dB)

Reg 0Bh - LUT Correction 28 - 31

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 16 - 31 (attenuation 8 to 15.5 dB) is set in Reg2 by bits mult_0 [11:10]

Bit	Name	Width	Default	Description
[3:0]	LUT_28	4	0000	2's complement 4-bit correction to LUT line 28 (attenuation 14 dB)
[7:4]	LUT_29	4	0000	2's complement 4-bit correction to LUT line 29 (attenuation 14.5 dB)
[11:8]	LUT_30	4	0000	2's complement 4-bit correction to LUT line 30 (attenuation 15 dB)
[15:12]	LUT_31	4	0000	2's complement 4-bit correction to LUT line 31 (attenuation 15.5 dB)

Reg 0Ch - LUT Correction 32 - 35

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 32 - 47 (attenuation 15 to 23.5 dB) is set in Reg2 by bits mult_0 [13:12]

Bit	Name	Width	Default	Description
[3:0]	LUT_32	4	0000	2's complement 4-bit correction to LUT line 32 (attenuation 16 dB)
[7:4]	LUT_33	4	0000	2's complement 4-bit correction to LUT line 33 (attenuation 16.5 dB)
[11:8]	LUT_34	4	0000	2's complement 4-bit correction to LUT line 34 (attenuation 17 dB)
[15:12]	LUT_35	4	0000	2's complement 4-bit correction to LUT line 35 (attenuation 17.5 dB)

Reg 0Dh - LUT Correction 36 - 39

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 32 - 47 (attenuation 15 to 23.5 dB) is set in Reg2 by bits mult_0 [13:12]

Bit	Name	Width	Default	Description
[3:0]	LUT_36	4	0000	2's complement 4-bit correction to LUT line 36 (attenuation 18 dB)
[7:4]	LUT_37	4	0000	2's complement 4-bit correction to LUT line 37 (attenuation 18.5 dB)
[11:8]	LUT_38	4	0000	2's complement 4-bit correction to LUT line 38 (attenuation 19 dB)
[15:12]	LUT_39	4	0000	2's complement 4-bit correction to LUT line 39 (attenuation 19.5 dB)

Reg 0Eh - LUT Correction 40 - 43

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 32 - 47 (attenuation 15 to 23.5 dB) is set in Reg2 by bits mult_0 [13:12]

Bit	Name	Width	Default	Description
[3:0]	LUT_40	4	0000	2's complement 4-bit correction to LUT line 40 (attenuation 20 dB)
[7:4]	LUT_41	4	0000	2's complement 4-bit correction to LUT line 41 (attenuation 20.5 dB)
[11:8]	LUT_42	4	0000	2's complement 4-bit correction to LUT line 42 (attenuation 21 dB)
[15:12]	LUT_43	4	0000	2's complement 4-bit correction to LUT line 43 (attenuation 21.5 dB)

Reg 0Fh - LUT Correction 44 - 47

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 32 - 47 (attenuation 15 to 23.5 dB) is set in Reg2 by bits mult_0 [13:12]

Bit	Name	Width	Default	Description
[3:0]	LUT_44	4	0000	2's complement 4-bit correction to LUT line 44 (attenuation 22 dB)
[7:4]	LUT_45	4	0000	2's complement 4-bit correction to LUT line 45 (attenuation 22.5 dB)
[11:8]	LUT_46	4	0000	2's complement 4-bit correction to LUT line 46 (attenuation 23 dB)
[15:12]	LUT_47	4	0000	2's complement 4-bit correction to LUT line 47 (attenuation 23.5 dB)

Reg 10h - LUT Correction 48 - 51

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 48 - 63 (attenuation 24 to 31.5 dB) is set in Reg2 by bits mult_0 [15:14]

Bit	Name	Width	Default	Description
[3:0]	LUT_48	4	0000	2's complement 4-bit correction to LUT line 48 (attenuation 24 dB)
[7:4]	LUT_49	4	0000	2's complement 4-bit correction to LUT line 49 (attenuation 24.5 dB)
[11:8]	LUT_50	4	0000	2's complement 4-bit correction to LUT line 50 (attenuation 25 dB)
[15:12]	LUT_51	4	0000	2's complement 4-bit correction to LUT line 51 (attenuation 25.5 dB)

Reg 11h - LUT Correction 52 - 55

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 48 - 63 (attenuation 24 to 31.5 dB) is set in Reg2 by bits mult_0 [15:14]

Bit	Name	Width	Default	Description
[3:0]	LUT_52	4	0000	2's complement 4-bit correction to LUT line 52 (attenuation 26 dB)
[7:4]	LUT_53	4	0000	2's complement 4-bit correction to LUT line 53 (attenuation 26.5 dB)
[11:8]	LUT_54	4	0000	2's complement 4-bit correction to LUT line 54 (attenuation 27 dB)
[15:12]	LUT_55	4	0000	2's complement 4-bit correction to LUT line 55 (attenuation 27.5 dB)

Reg 12h - LUT Correction 56 - 59

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 48 - 63 (attenuation 24 to 31.5 dB) is set in Reg2 by bits mult_0 [15:14]

Bit	Name	Width	Default	Description
[3:0]	LUT_56	4	0000	2's complement 4-bit correction to LUT line 56 (attenuation 28 dB)
[7:4]	LUT_57	4	0000	2's complement 4-bit correction to LUT line 57 (attenuation 28.5 dB)
[11:8]	LUT_58	4	0000	2's complement 4-bit correction to LUT line 58 (attenuation 29 dB)
[15:12]	LUT_59	4	0000	2's complement 4-bit correction to LUT line 59 (attenuation 29.5 dB)

Reg 13h - LUT Correction 60 - 63

LUT correction values below can also be multiplied by 1,2,3, or 4 if more correction is needed. Multiplication factor for LUT lines 48 - 63 (attenuation 24 to 31.5 dB) is set in Reg2 by bits mult_0 [15:14]

Bit	Name	Width	Default	Description
[3:0]	LUT_60	4	0000	2's complement 4-bit correction to LUT line 60 (attenuation 30 dB)
[7:4]	LUT_61	4	0000	2's complement 4-bit correction to LUT line 61 (attenuation 30.5 dB)
[11:8]	LUT_62	4	0000	2's complement 4-bit correction to LUT line 62 (attenuation 31 dB)
[15:12]	LUT_63	4	0000	2's complement 4-bit correction to LUT line 63 (attenuation 31.5 dB)

Characterization Set-up