HMC829LP6GE

v01.0911

FRACTIONAL-N PLL WITH INTEGRATED VCO
45 - 1050, 1400 - 2100, 2800 - 4200 MHz

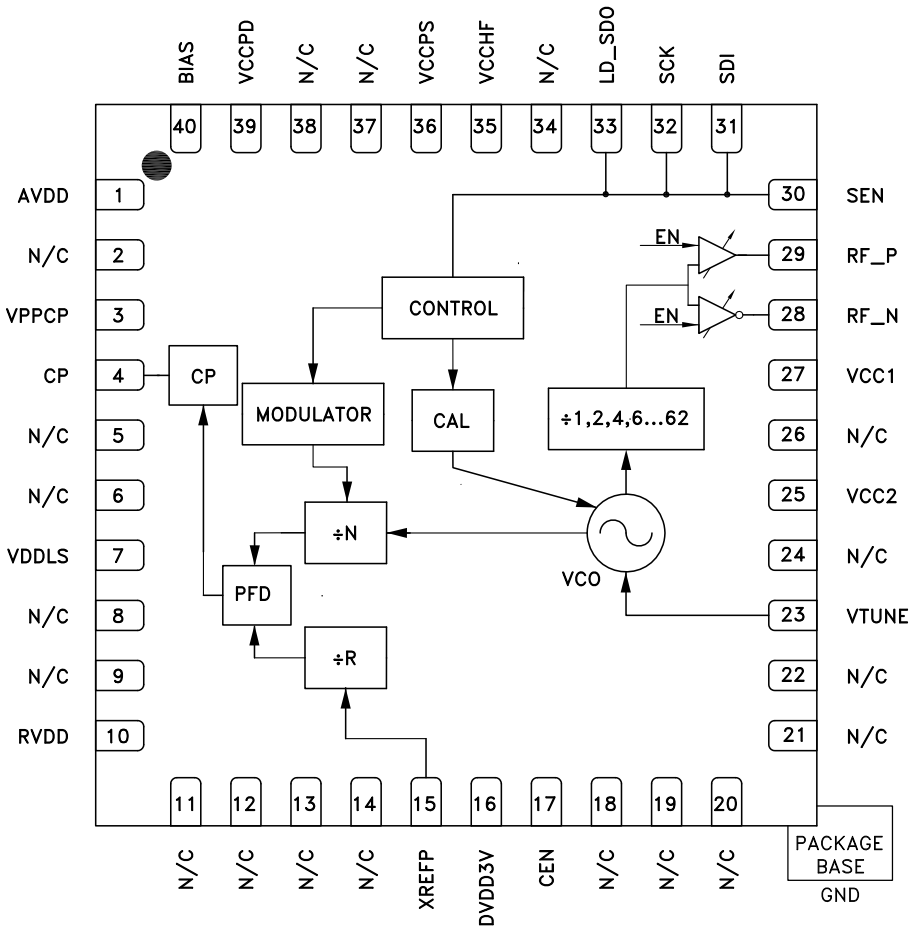
Features

- RF Bandwidth:
  45 - 1050, 1400 - 2100, 2800 - 4200 MHz
- Maximum Phase Detector Rate
  100 MHz
- Ultra Low Phase Noise
  -110 dBc/Hz in Band Typ.
- Figure of Merit (FOM) -227 dBc/Hz
- <180 fs RMS Jitter
- 24-bit Step Size, Resolution 3 Hz typ
- Exact Frequency Mode
- Built in Digital Self Test
- 40 Lead 6x6 mm SMT Package: 36 mm^2

Typical Applications

- Cellular/4G, WiMax Infrastructure
- Repeaters and Femtocells
- Communications Test Equipment
- CATV Equipment
- Phased Array Applications
- DDS Replacement
- Very High Data Rate Radios
- Tunable Reference Source for Spurious-Free Performance

Functional Diagram



FRACTIONAL-N PLL WITH INTEGRATED VCO
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General Description

The is a low noise, wide band, Fractional-N Phase-Locked-Loop (PLL) that features an integrated Voltage Controlled Oscillator (VCO) with a fundamental frequency of 2800 MHz - 4200 MHz, and an integrated VCO Output Divider (divide by 1/2/4/6.../60/62), that together allow the to generate frequencies from 45 MHz to 1050 MHz, from 1400 MHz to 2100 MHz, and from 2800 MHz to 4200 MHz. The integrated Phase Detector (PD) and delta-sigma modulator, capable of operating at up to 100 MHz, permit wider loop-bandwidths with excellent spectral performance.

The features industry leading phase noise and spurious performance, across all frequencies, that enable it to minimize blocker effects, and improve receiver sensitivity and transmitter spectral purity. The superior noise floor (< -170 dBc/Hz) makes the an ideal source for a variety of applications - such as; LO for RF mixers, a clock source for high-frequency data-converters, or a tunable reference source for ultra-low spurious applications.

Additional features of the include RF output power control from 0 to 6 dB (~2 dB steps), output Mute function, and a delta-sigma modulator Exact Frequency Mode which enables users to generate output frequencies with 0 Hz frequency error.

For theory of operation and register map refer to the "PLLs with Integrated VCOs - RF VCOs Operating Guide". To view the Operating Guide, please visit www.hittite.com and choose from the "Search by Part Number" pull down menu.

Electrical Specifications

VPPCP, VDDLS, VCC1, VCC2 = 5V; RVDD, AVDD, DVDD3V, VCCPD, VCCHF, VCCPS = 3.3V Min and Max Specified across Temp -40 °C to 85 °C

Parameter	Condition	Min.	Typ.	Max.	Units
RF Output Characteristics					
Output Frequency	Band 1	45		1050	MHz
	Band 2	1400		2100	MHz
	Band 3	2800		4200	MHz
VCO Frequency at PLL Input		2800		4200	MHz
RF Output Frequency at f_{VCO}		2800		4200	MHz
Output Power					
RF Output Power at f_{VCO} = 4000 MHz Across All Frequencies see Figure 9	Single-ended Power Broadband Matched Internally [1]	1	3	4.3	dBm
Output Power Control	~2 dB Steps	6		7.5	dB
Harmonics					
fo Mode at 4000 MHz	2nd / 3rd / 4th		-25/-29/-38		dBc
fo/2 Mode at 4000 MHz/2 = 2 GHz	2nd / 3rd / 4th		-25/-24/-35		dBc
fo/30 Mode at 2800 MHz/28 = 100 MHz	2nd / 3rd / 4th		-20/-10/-26		dBc
fo/62 Mode at 2800 MHz/62 = 45 MHz	2nd / 3rd / 4th		-14/-8/-21		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynamically max	20		524,283	

[1] Measured single-ended. Additional 3 dB possible with differential outputs.
[2] Measured with 100 Ω external termination. See Hittite PLL w/ Integraged VCOs Operating Guide Reference Input Stage section for more details.

FRACTIONAL-N PLL WITH INTEGRATED VCO
45 - 1050, 1400 - 2100, 2800 - 4200 MHz

Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled [2]	1	2	3.3	Vp-p
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	
Phase Detector (PD) [3]					
PD Frequency Fractional Mode B	[4]	DC		100	MHz
PD Frequency Fractional Mode A (and Register 6 [17:16] = 11)		DC		80	MHz
PD Frequency Integer Mode		DC		125	MHz
Charge Pump					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		µA
PD/Charge Pump SSB Phase Noise	50 MHz Ref, Input Referred				
1 kHz			-143		dBc/Hz
10 kHz	Add 1 dB for Fractional		-150		dBc/Hz
100 kHz	Add 3 dB for Fractional		-153		dBc/Hz
Logic Inputs					
Vsw		40	50	60	% DVDD
Logic Outputs					
VOH Output High Voltage			DVDD		V
VOL Output Low Voltage			0		V
Output Impedance		100		200	Ω
Maximum Load Current				1.5	mA
Power Supply Voltages					
3.3 V Supplies	AVDD, VCCHF, VCCPS, VCCPD, RVDD,DVDD	3.0	3.3	3.5	V
5 V Supplies	VPPCP, VDDLS, VCC1, VCC2	4.8	5	5.2	V
Power Supply Currents					
+5V Analog Charge Pump	VPPCP, VDDLS		8		mA
+5V VCO Core and VCO Buffer	fo/1 Mode VCC2		105		mA
	fo/N Mode VCC2		80		mA
+5V VCO Divider and RF/PLL Buffer	Single-Ended Output Mode fo/1 Mode VCC1		25		mA
	Differential Output Mode fo/1 Mode VCC1		40		mA
	Single-Ended Output Mode fo/N Mode VCC1	80		100	mA
	Differential Output Mode fo/N Mode VCC1	95		115	mA

[3] Slew rate of greater or equal to 0.5 ns/V is recommended, see PLL with Integrated RF VCOs Operating Guide for more details. Frequency is guaranteed across process voltage and temperature from -40 °C to 85 °C.
[4] This maximum phase detector frequency can only be achieved if the minimum N value is respected. eg. In the case of fractional feedback mode, the maximum PFD rate = fvco/20 or 100 MHz, whichever is less.

Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
+3.3V	AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD3V		52		mA
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked		10		µA
Power Down - Crystal On, 100 MHz	Reg01h =0, Crystal Clocked 100 MHz		10	30	mA
Power on Reset					
Typical Reset Voltage on DVDD			700		mV
Min DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		µs
VCO Open Loop Phase Noise at fo @ 4 GHz					
10 kHz Offset			-78		dBc/Hz
100 kHz Offset			-108		dBc/Hz
1 MHz Offset			-134.5		dBc/Hz
10 MHz Offset			-156		dBc/Hz
100 MHz Offset			-171		dBc/Hz
VCO Open Loop Phase Noise at fo @ 4 GHz/2 = 2 GHz					
10 kHz Offset			-83		dBc/Hz
100 kHz Offset			-113		dBc/Hz
1 MHz Offset			-139.5		dBc/Hz
10 MHz Offset			-165.5		dBc/Hz
100 MHz Offset			-167		dBc/Hz
VCO Open Loop Phase Noise at fo @ 2.8 GHz/28 = 100 MHz					
10 kHz Offset			-111		dBc/Hz
100 kHz Offset			-141		dBc/Hz
1 MHz Offset			-163.5		dBc/Hz
10 MHz Offset			-170		dBc/Hz
100 MHz Offset			-173		dBc/Hz
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
VCO Characteristics					
VCO Tuning Sensitivity at 4053 MHz	Measured at 2.5 V		15		MHz/V
VCO Tuning Sensitivity at 3777 MHz	Measured at 2.5 V		13		MHz/V
VCO Tuning Sensitivity at 3411 MHz	Measured at 2.5 V		12		MHz/V
VCO Tuning Sensitivity at 2943 MHz	Measured at 2.5 V		11.5		MHz/V
VCO Supply Pushing	Measured at 2.5 V		2		MHz/V

RoHS✓ EARTH FRIENDLY

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Figure 1. Typical Closed Loop Integer Phase Noise ["Loop Filter Configuration Table"]

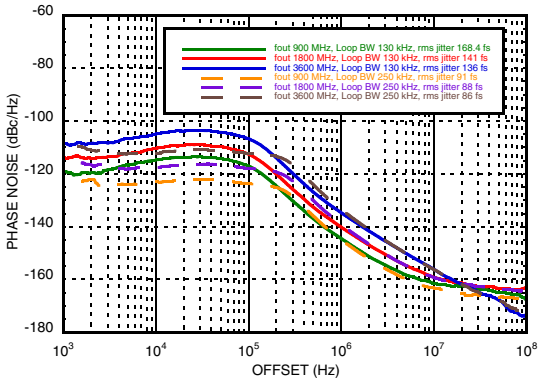


Figure 2. Typical Closed Loop Fractional Phase Noise ["Loop Filter Configuration Table"]

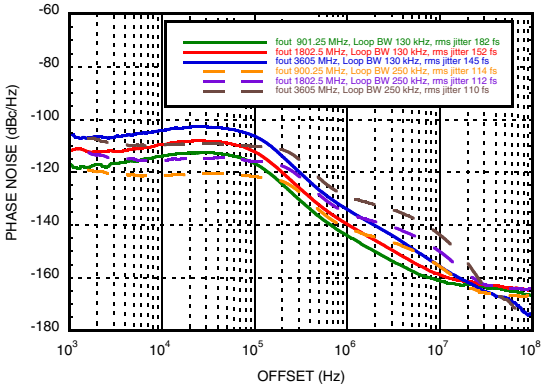


Figure 3. Free Running Phase Noise

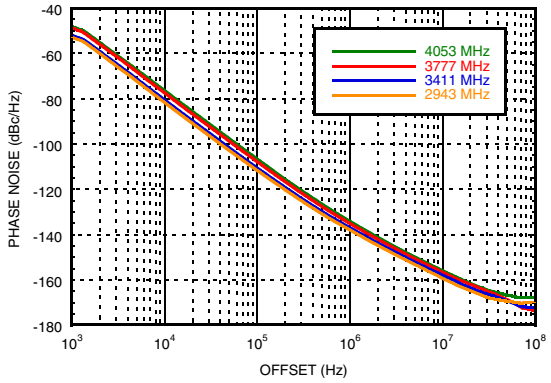


Figure 4. Free Running VCO Phase Noise vs. Temperature

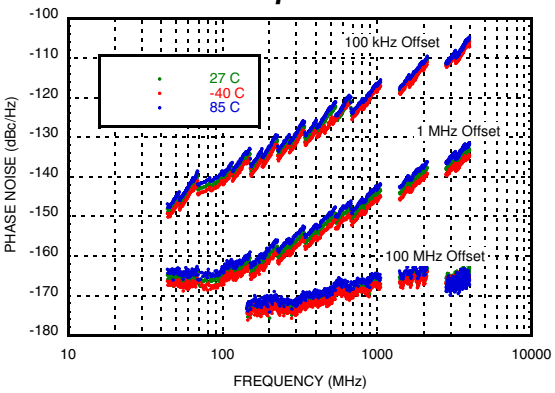


Figure 5. Typical VCO Sensitivity

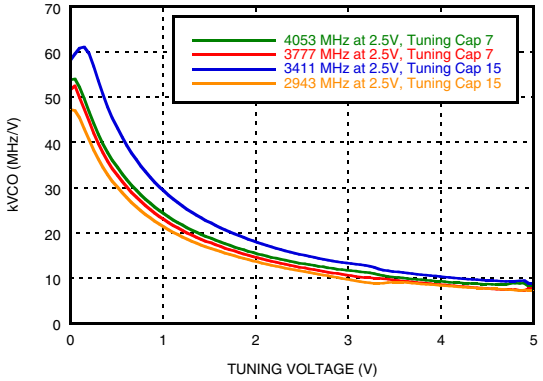


Figure 6. Typical Tuning Voltage After Calibration

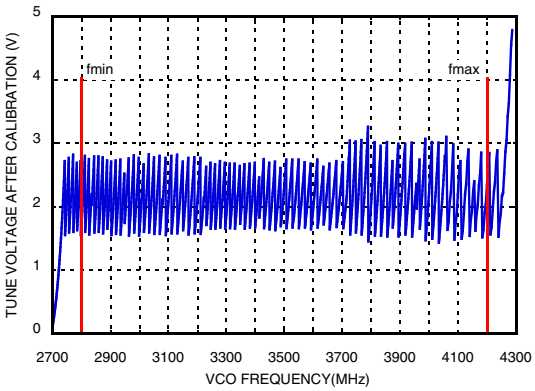


Figure 7. Integrated RMS Jitter[1]

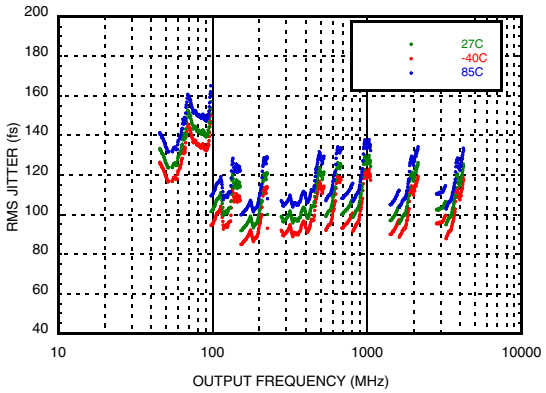


Figure 8. Figure of Merit

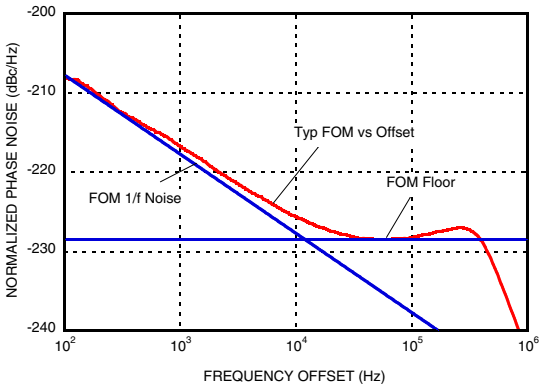


Figure 9. Typical Single-Ended Output Power

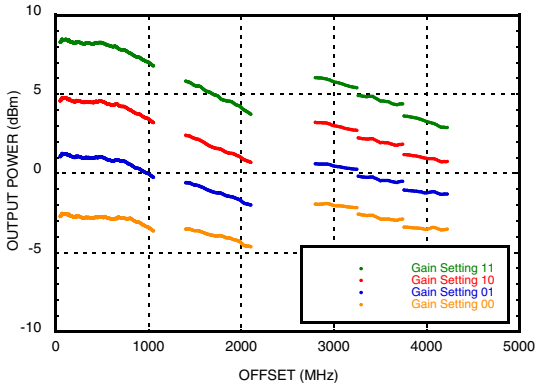


Figure 10. Typical Single-Ended Output Power vs. Temperature, Maximum Gain

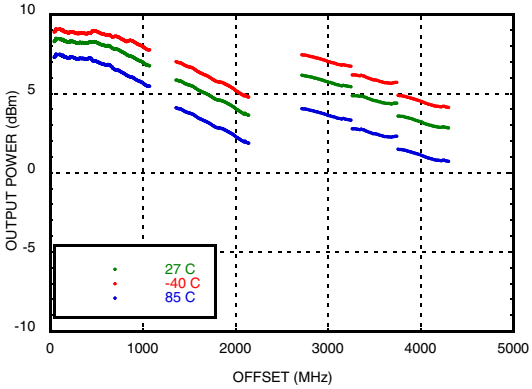


Figure 11. RF Output Return Loss

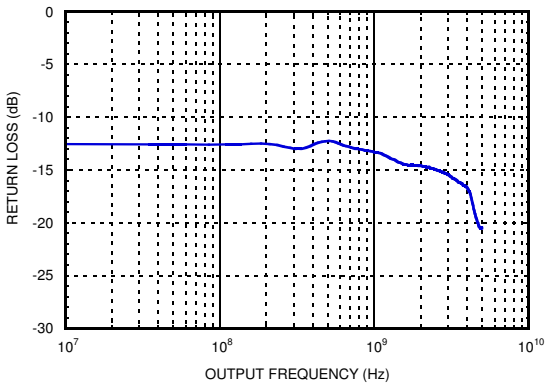
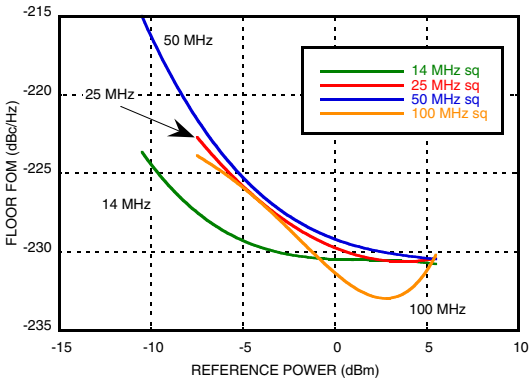


Figure 12. Reference Input Sensitivity, Square Wave, 50 Ω [2]



[1] RMS Jitter data is measured in fractional mode with 250 kHz Loop bandwidth using 100 MHz reference, PD 50 MHz. Integration bandwidth from 1 kHz to 100 MHz.

[2] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

Figure 13. Reference Input Sensitivity Sinusoid Wave, 50 Ω[3]

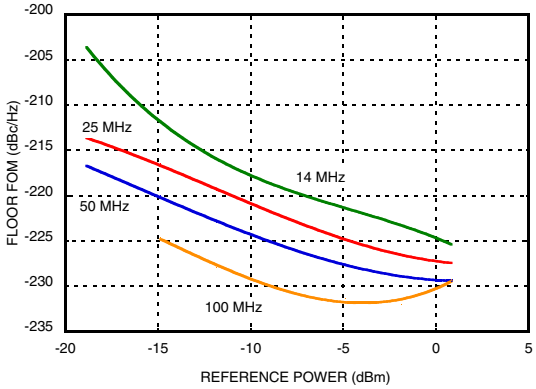


Figure 14. Integer Boundary Spur at 3600.2 MHz[4]

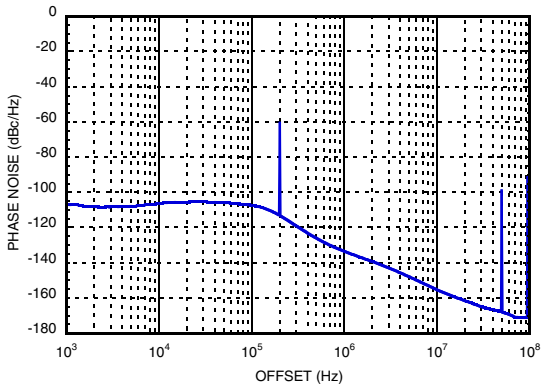


Figure 15. Integer-N, Exact Frequency Mode ON, Performance at 900 MHz[5]

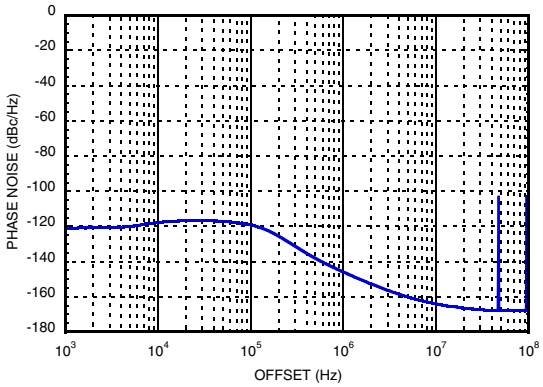


Figure 16. Fractional-N, Exact Frequency Mode ON, Performance at 1813.5 MHz[6]

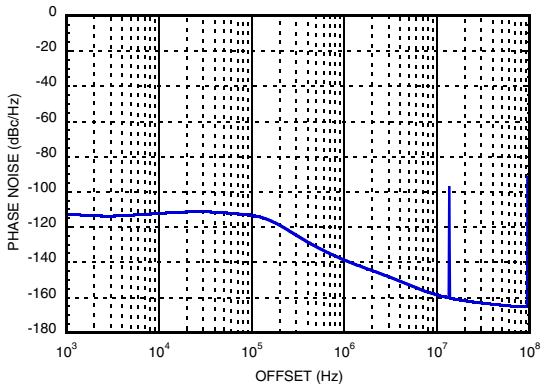


Figure 17. Fractional-N, Exact Frequency Mode ON, Performance at 3591 MHz[7]

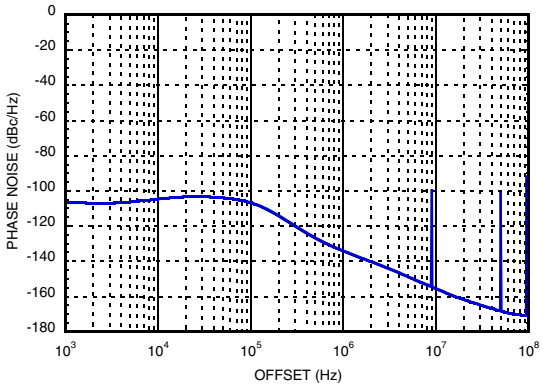
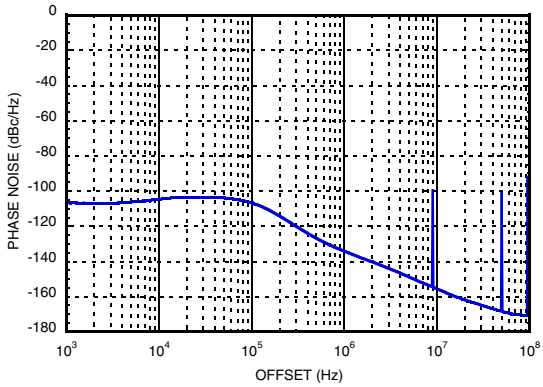


Figure 18. Fractional-N, Exact Frequency Mode OFF, Performance at 3591 MHz[8]



[3] Measured from a 50 Ω source with a 100 Ω external resistor termination. See PLL with Integrated RF VCOs Operating Guide Reference Input Stage section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

[4] Fractional Mode Mode B, Integer Boundary Spur at 3600.2 MHz, Loop Filter bandwidth 130 kHz, REF in 100 MHz, 50 MHz PD

[5] REF in 100 MHz, 50 MHz PD, Output Divider 4 Selected, Loop Filter bandwidth 130 kHz, Channel Spacing 100 kHz

[6] Exact Frequency Mode, REF in 100 MHz, 50 MHz PD, Output Divider 2 Selected, Loop Filter bandwidth = 130 kHz, Channel Spacing = 100 kHz

[7] Exact Frequency Mode, Channel Spacing 100 kHz, RF out = 3951 MHz, REF in 100 MHz, 50 MHz PD, Output Divider 1 selected, Loop Filter bandwidth 130 kHz,

[8] Fractional Mode B, RF out 3591 MHz, REF in 100 MHz, 50 MHz PD, Output Divider 1 selected, Loop Filter bandwidth 130 kHz.

Figure 19. Worst Spur, Fixed 50 MHz Reference, Output Freq. = 3900.1 MHz[9]

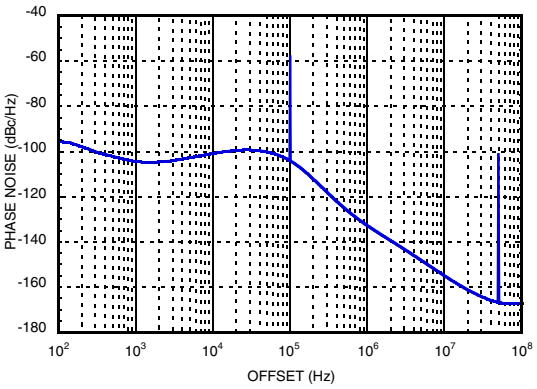


Figure 20. Worst Spur, Tunable Reference 47.5 MHz, Output Frequency = 3900.1 MHz [9]

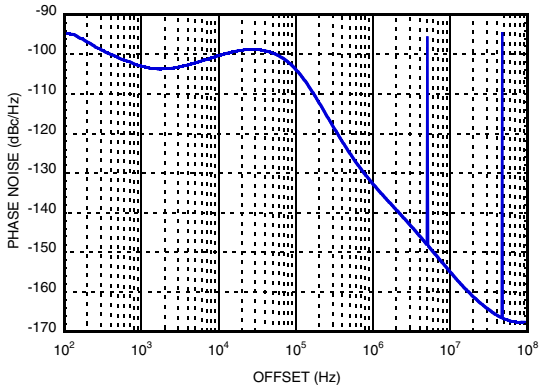


Figure 21. Worst Spur, Fixed vs. Tunable Reference [10]

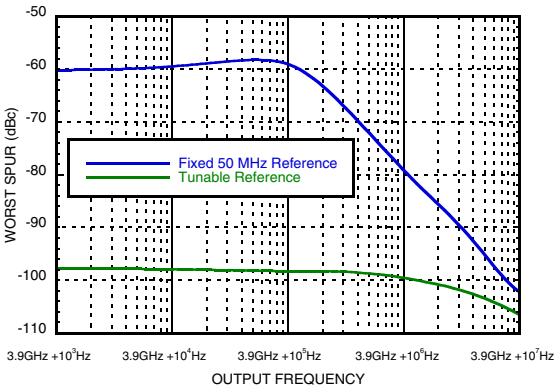
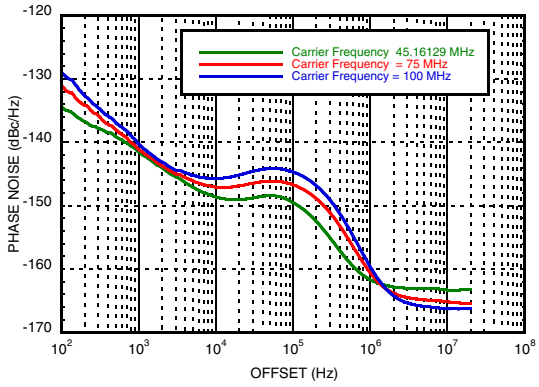
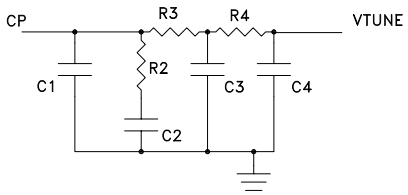


Figure 22. Low Frequency Performance [11]



Loop Filter Configuration Table

Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
130	100	8.2	120	120	1	1.2	1.2	
250	150	3.3	18	18	2.2	1	1	

[9] Capability of to generate low frequencies (as low as 45 MHz), enables the to be used as a tunable reference source into another Hittite PLL. This maximizes spur performance of Hittite PLLs. Please see "Application Information" for more information.

[10] The graph is generated by observing, and plotting, the magnitude of only the worst spur (largest magnitude), at any offset, at each output frequency, while using a fixed 50 MHz reference and a tunable reference tuned to 47.5 MHz. See "Application Information" for more details.

[11] Phase noise performance of the when used as a tunable reference source. is operating at 4.2 GHz/42, 4.2 GHz/56, and 2.8 GHz/62 for the 100 MHz, 75 MHz, and 45.16129 MHz curves respectively, using a second order loop filter with 230 kHz bandwidth.

Pin Descriptions

Pin Number	Function	Description
1	AVDD	DC Power Supply for analog circuitry.
2, 5, 6, 8, 9, 11 - 14, 18 - 22, 24, 26, 34, 37, 38	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
3	VPPCP	Power Supply for charge pump analog section
4	CP	Charge Pump Output
7	VDDLS	Power Supply for the charge pump digital section
10	RVDD	Reference Supply
15	XREFP	Reference Oscillator Input
16	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry
17	CEN	Chip Enable. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning Port Input.
25	VCC2	VCO Analog Supply 2
27	VCC1	VCO Analog Supply 1
28	RF_N	RF Negative Output (On in differential and single-ended configuration)
29	RF_P	RF Positive Output (Off in single-ended, On in differential configuration)
30	SEN	PLL Serial Port Enable (CMOS) Logic Input
31	SDI	PLL Serial Port Data (CMOS) Logic Input
32	SCK	PLL Serial Port Clock (CMOS) Logic Input
33	LD_SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)
35	VCCHF	DC Power Supply for Analog Circuitry
36	VCCPS	DC Power Supply for Analog Prescaler
39	VCCPD	DC Power Supply for Phase Detector
40	BIAS	External bypass decoupling for precision bias circuits. Note: 1.920V ±20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10GΩ meter such as Agilent 34410A, normal 10MΩ DVM will read erroneously.

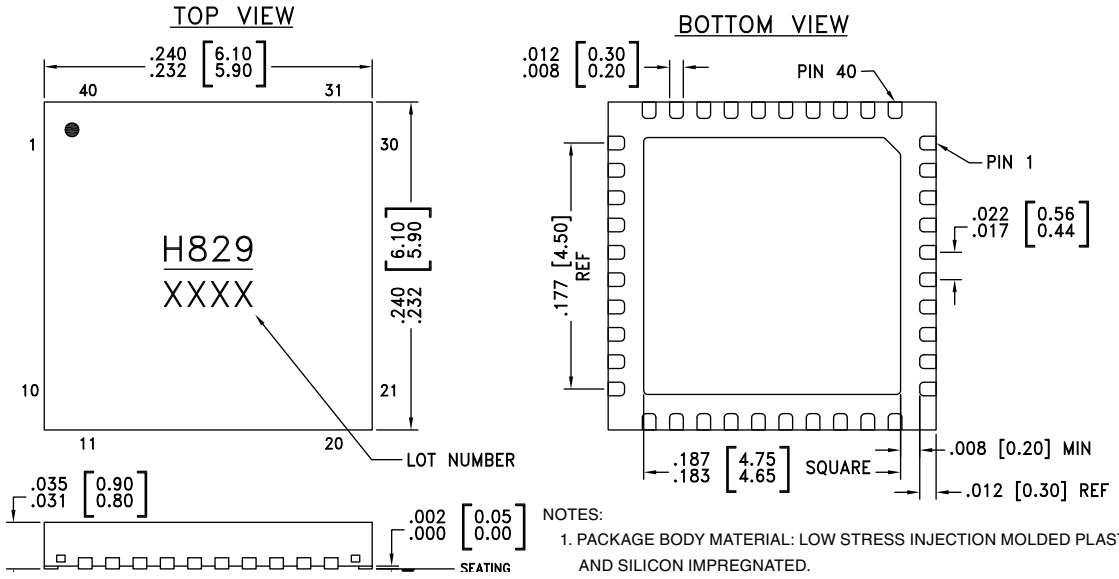
FRACTIONAL-N PLL WITH INTEGRATED VCO
45 - 1050, 1400 - 2100, 2800 - 4200 MHz

Absolute Maximum Ratings

AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS	-0.3V to +3.6V
VPPCP, VDDLS, VCC1, VCC2	-0.3V to +5.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to 150°C
Maximum Junction Temperature	125 °C
Thermal Resistance (R_{TH}) (junction to ground paddle)	20 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Outline Drawing



NOTES:

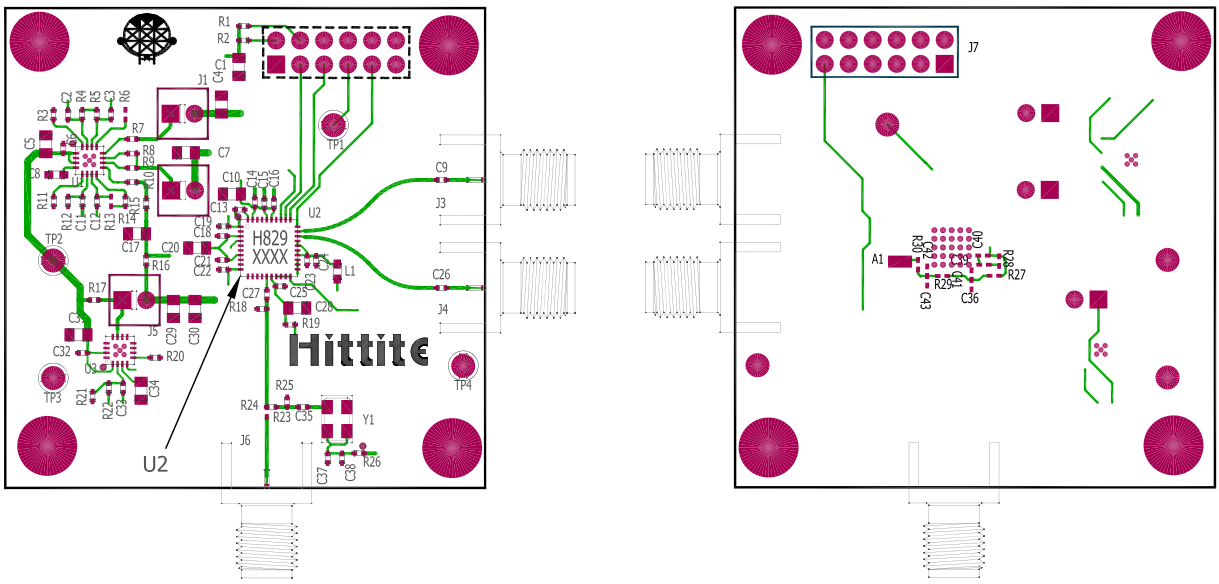
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H829 XXXX

[1] 4-Digit lot number XXXX

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Order Information

Item	Contents	Part Number
Evaluation PCB Only	Evaluation PCB	EVAL01-
Evaluation Kit	Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-

Application Information

Large bandwidth, industry leading phase noise and spurious performance, excellent noise floor (<-170 dBc/Hz), coupled with a high level of integration make the ideal for a variety of applications; as an RF or IF stage LO, a clock source for high-frequency data-converters, or a tunable reference source for extremely low spurious applications (~ -100 dBc/Hz spurs).

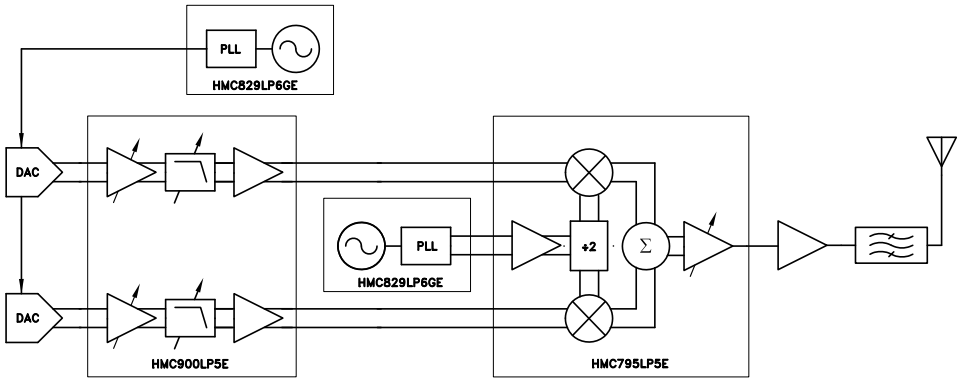


Figure 23. in a typical transmit chain

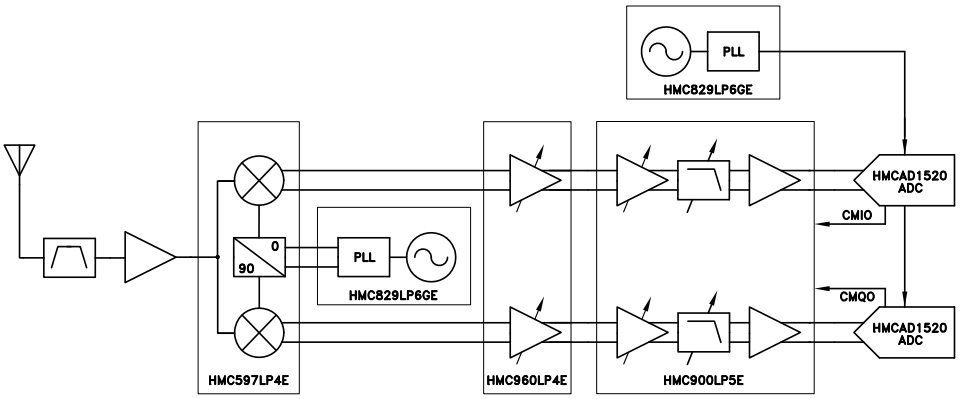


Figure 24. in a typical receive chain

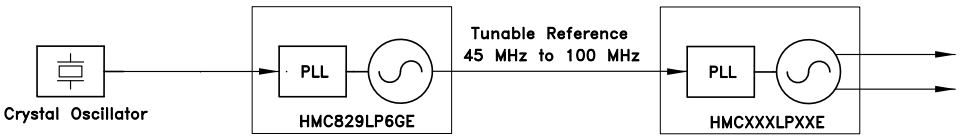


Figure 25. used as a tunable reference for second

Using the with a tunable reference as shown in Figure 25, it is possible to drastically improve spurious emissions performance across all frequencies. Example shown in Figure 21 graph shows that it is possible to have spurious emissions ~ -100 dBc/Hz across all frequencies. For more information about spurious emissions, how they are related to the reference frequency, and how to tune the reference frequency for optimal spurious performance please see the “Spurious Performance” section of Hittite PLL w/ Integraged VCOs Operating Guide. Note that at very low output frequencies < 100 MHz, harmonics increase due to small internal AC coupling. Applications which are sensitive to harmonics may require external low pass filtering.