HMC851LC3C

v00.0610

28 Gbps, XOR / XNOR GATE w/ PROGRAMMABLE OUTPUT VOLTAGE

Typical Applications

The HMC851LC3C is ideal for:

- RF ATE Applications
- Broadband Test & Measurement
- Serial Data Transmission up to 28 Gbps

Features

Inputs Terminated Internally in 50 Ohms

Differential & Singe-Ended Operation

Fast Rise and Fall Times: 15 / 14 ps

Low Power Consumption: 241 mW typ.

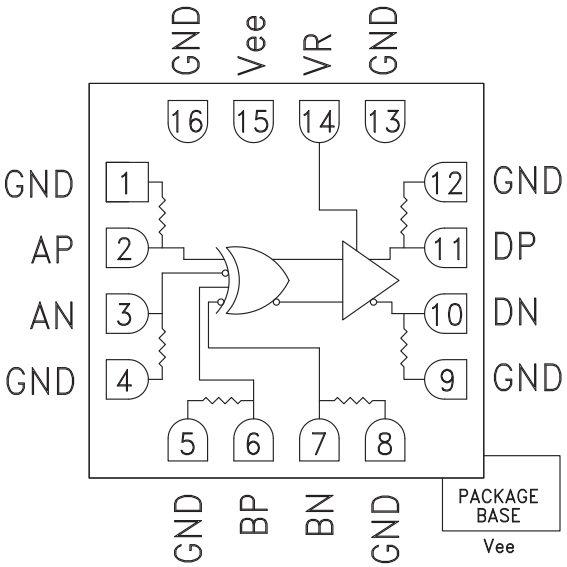
Programmable Differential
Output Voltage Swing: 500 - 1300 mV

Propagation Delay: 97 ps

Single Supply: -3.3V

16 Lead Ceramic 3x3 mm SMT Package: 9 mm^2

Functional Diagram



General Description

The HMC851LC3C is a XOR/XNOR gate function designed to support data transmission rates of up to 28 Gbps, and clock frequencies as high as 28 GHz. The HMC851LC3C also features an output level control pin, VR, which allows for loss compensation or for signal level optimization.

All input signals to the HMC851LC3C are terminated with 50 Ohms to ground on-chip, and may be either AC or DC coupled. The differential outputs of the HMC851LC3C may be either AC or DC coupled. Outputs can be connected directly to a 50 Ohm to ground terminated system, while DC blocking capacitors may be used if the terminating system is 50 Ohms to a non-ground DC voltage. The HMC851LC3C operates from a single -3.3V DC supply, and is available in a ceramic RoHS compliant 3x3 mm SMT package.

Electrical Specifications, T_A = +25°C, Vee = -3.3V, VR = 0

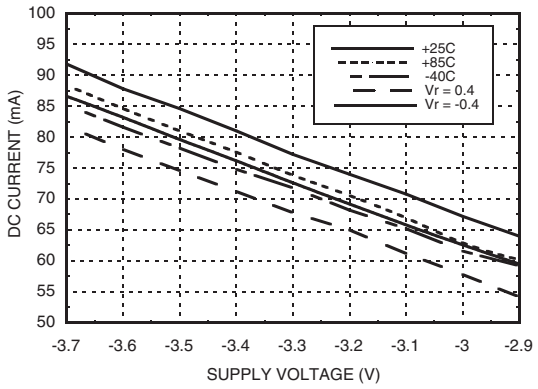
Parameter	Conditions	Min.	Typ.	Max	Units
Power Supply Voltage		-3.6	-3.3	-3.0	V
Power Supply Current			73		mA
Maximum Data Rate			28		Gbps
Maximum Clock Rate			28		GHz
Input High Voltage		-0.5		0.5	V
Input Low Voltage		-1.0		0.0	V
Input Return Loss	Frequency <20 GHz		10		dB
Output Amplitude	Single-Ended, peak-to-peak		545		mVp-p
	Differential, peak-to-peak		1090		mVp-p
Output High Voltage			-15		mV

Electrical Specifications, (continued)

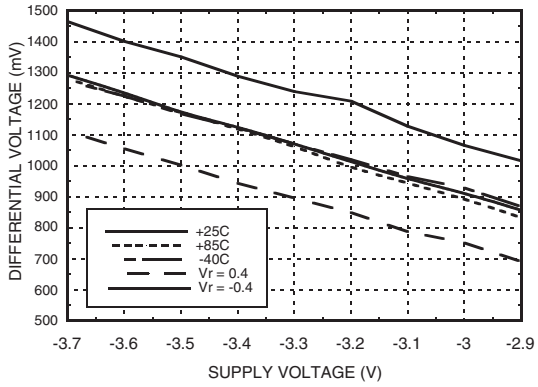
Parameter	Conditions	Min.	Typ.	Max	Units
Output Low Voltage			-560		mV
Output Rise / Fall Time	Differential, 20% - 80%		15 / 14		ps
Output Return Loss	Frequency < 18 GHz		10		dB
Small Signal Gain			30		dB
Random Jitter Jr	rms			0.2	ps rms
Deterministic Jitter, Jd	peak-to-peak, 2^{15}-1 PRBS input [1]		2		ps, p-p
Propagation Delay, A to D, Tpda			97		ps
Propagation Delay, B to D, Tpdb			102		ps

[1] Deterministic jitter calculated by simultaneously measuring the jitter of a 300 mV, 28 Gbps, 2^{15}-1 PRBS input, and a single-ended output

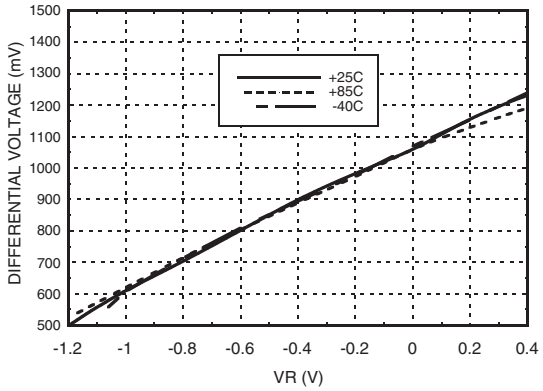
DC Current vs. Supply Voltage [1] [2]



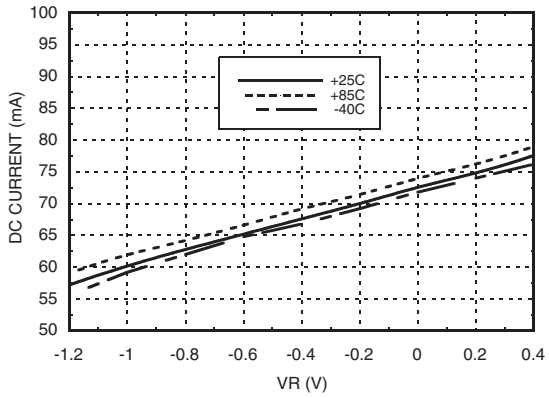
Output Differential vs. Supply Voltage [1] [2]



Output Differential vs. VR [2][3]

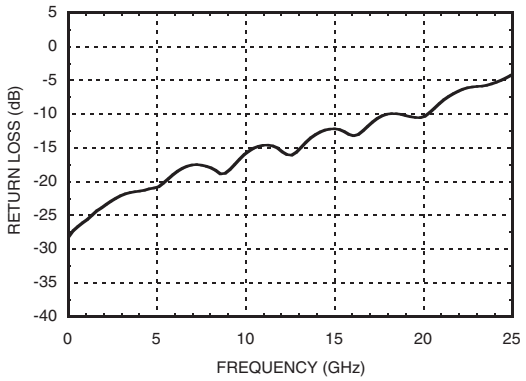


DC Current vs. VR [2][3]

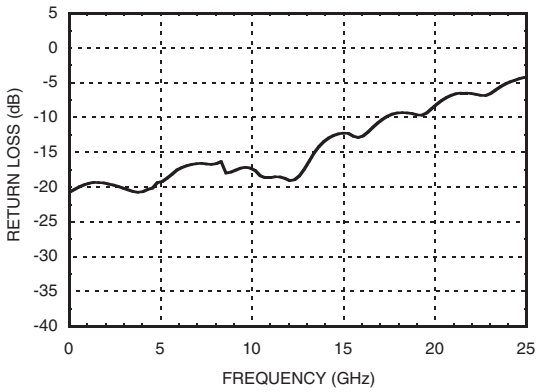


[1] VR = 0.0V [2] Frequency = 28 GHz [3] Vee = -3.3

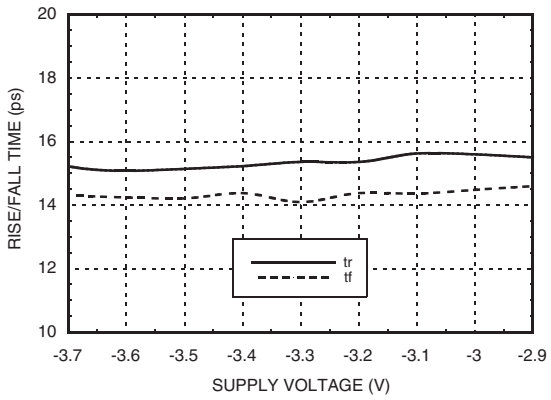
Input Return Loss vs. Frequency [1][3][5]



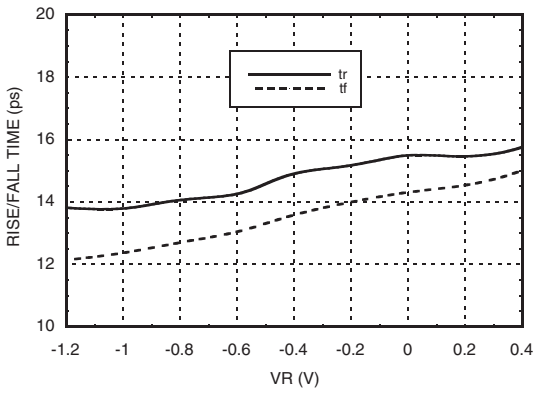
Output Return Loss vs. Frequency [1][3][5]



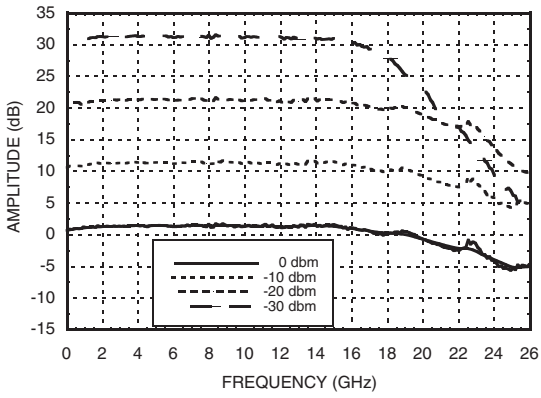
Rise / Fall Time vs. Supply Voltage [1][2]



Rise / Fall Time vs. VR [2][5]

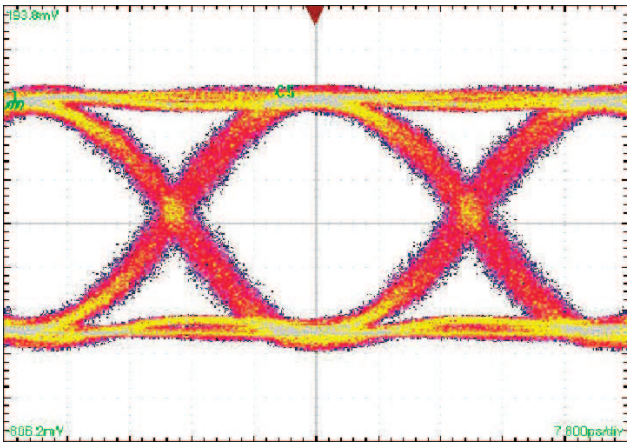


Amplitude vs. Input Power [1][4][5]



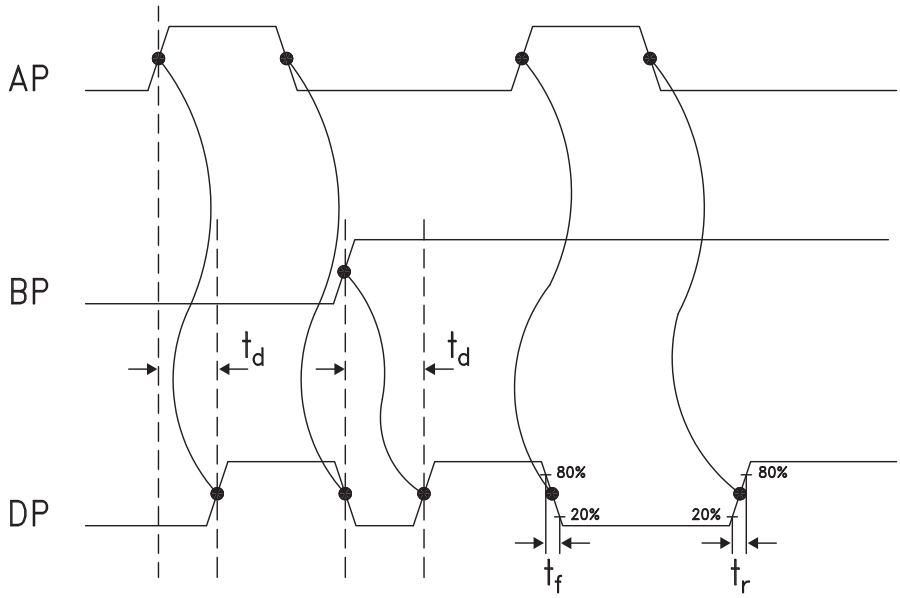
[1] VR = 0.0V [2] Frequency = 28 GHz [3] Device measured on evaluation board with single-ended time domain gating.
[4] Device measured on evaluation board with single ended time domain port extensions [5] Vee = -3.3V

Eye Diagram



[1] Test Conditions:
Single ended 400 mV data input. Pattern generated with 2^{15} -1 PN patterns applied to the inputs resulting in a Quasi-Periodic PRBS pattern at 28 Gbps. Measured using Tektronix CSA 8000.

Timing Diagram



Truth Table

Input		Outputs
A	B	D
L	L	L
L	H	H
H	L	H
H	H	L
Notes: A = AP - AN B = BP - BN D = DP - DN	H - Positive voltage level L - Negative voltage level	

HMC851LC3C

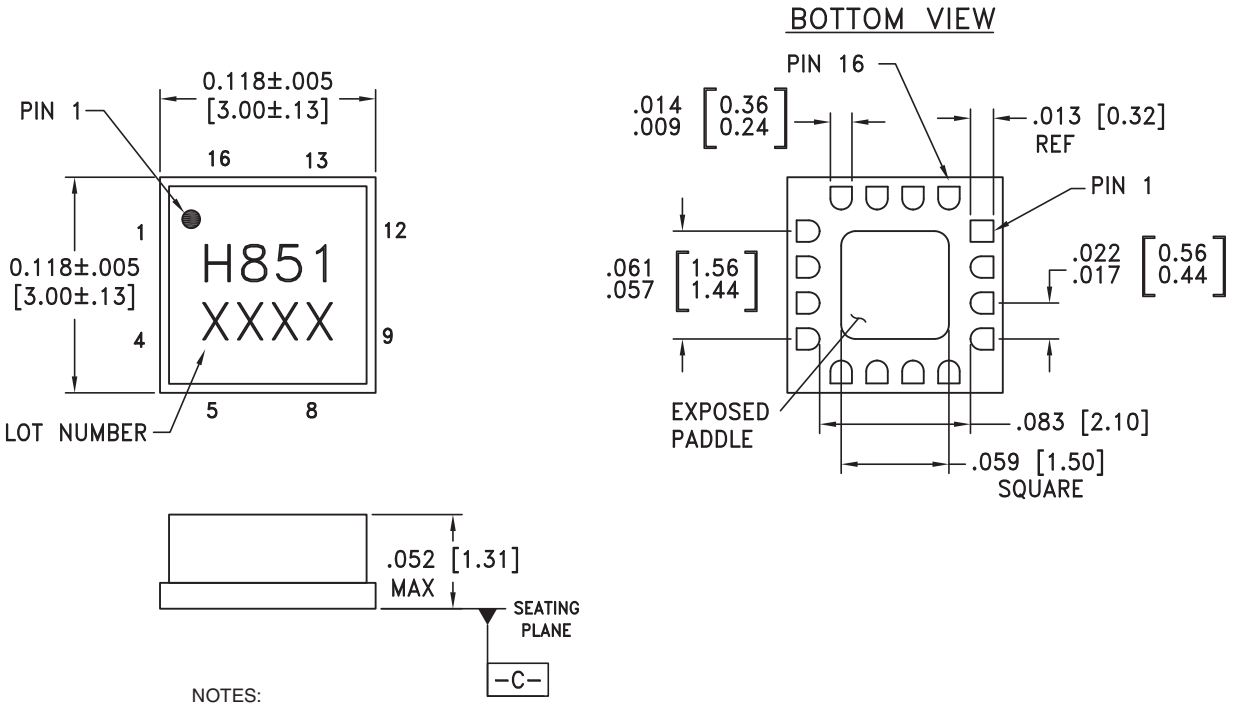
28 Gbps, XOR / XNOR GATE w/ PROGRAMMABLE OUTPUT VOLTAGE

Absolute Maximum Ratings

Power Supply Voltage (Vee)	-3.75V to +0.5V
Input Signals	-2V to +0.5V
Output Signals	-1.5V to +1V
Continuous Pdiss (T = 85 °C) (derate 17 mW/°C above 85 °C)	0.68 W
Thermal Resistance ($R_{th\ j\text{-}p}$) Worst case junction to package paddle	59 °C/W
Storage Temperature	-65 °C to +150 °C
Operating Temperature	-40 °C to +85 °C

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

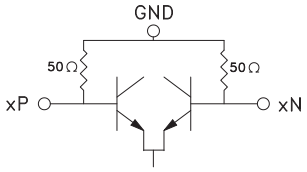
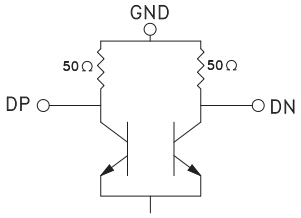
Outline Drawing



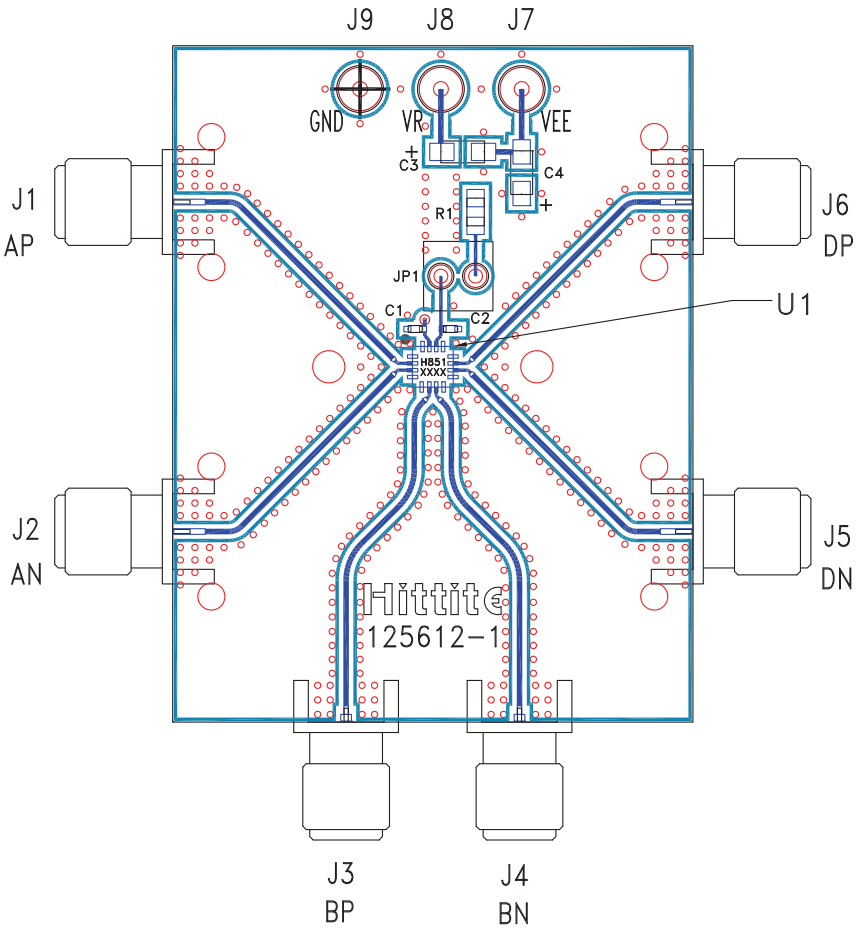
NOTES:

1. PACKAGE BODY MATERIAL: ALUMINA
2. LEAD AND GROUND PADDLE PLATING:
   30-80 MICROINCHES GOLD OVER 50 MICROINCHES MINIMUM NICKEL.
3. DIMENSIONS ARE IN INCHES [MILLIMETERS].
4. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm DATUM -C-
6. ALL GROUND LEADS MUST BE SOLDERED TO PCB RF GROUND.
7. PADDLE MUST BE SOLDERED TO Vee.

Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 4, 5, 8, 9, 12, 13, 16	GND	These pins must be connected to a high quality RF/DC ground.	
2, 3 6, 7	AP, AN BP, BN	Differential Data Inputs: Current Mode Logic (CML) referenced to positive supply.	
10, 11	DN, DP	Differential Data Outputs: Current Mode Logic (CML) referenced to positive supply.	
14	VR	Output level control. Output level may be increased or decreased by applying a voltage to VR per “Output Differential vs. VR” plot.	
15, Package Base	Vee	This pin and the exposed paddle must be connected to the negative voltage supply.	

Evaluation PCB



List of Materials for Evaluation PCB 125614 [1]

Item	Description
J1 - J6	PCB Mount K RF Connectors
J7 - J9	DC Pin
JP1	0.1" Header with Shorting Jumper
C1, C2	100 pF Capacitor, 0402 Pkg.
C3, C4	4.7 µF Capacitor, Tantalum
R1	10 Ohm Resistor, 0603 Pkg.
U1	HMC851LC3C High Speed Logic, XOR / XNOR Gate
PCB [2]	125612 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to Vee. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request. Install jumper on JP1 to short VR to GND for normal operation.

Application Circuit