

Low-power Single-channel Decimation Filter

Features

- Single-channel Digital Decimation Filter
 - ◆ Multiple On-chip FIR and IIR Coefficient Sets
 - ◆ Programmable Coefficients for Custom Filters
 - ◆ Synchronous Operation
- Integrated PLL for Clock Generation
 - ◆ 1.024 MHz, 2.048 MHz, or 4.096 MHz Input
 - ◆ Standard Clock or Manchester Input
- Selectable Output Word Rate
 - ◆ 4000, 2000, 1000, 500, 333, 250 SPS
 - ◆ 200, 125, 100, 50, 40, 25, 20, 10, 5, 1 SPS
- Digital Gain and Offset Corrections
- Test DAC Bit-stream Generator
 - ◆ Digital Sine Wave Output
- Time Break Controller, General-purpose I/O
- Microcontroller or EEPROM Configuration
- Small-footprint, 28-pin SSOP Package
- Low Power Consumption
 - ◆ 16 mW at 500 SPS OWR
- Flexible Power Supplies
 - ◆ I/O Interface and PLL: 3.3 V or 5.0 V
 - ◆ Digital Logic Core: 2.5 V, 3.3 V or 5.0 V

Description

The CS5378 is a multi-function digital filter utilizing a low power signal processing architecture to achieve efficient filtering for a delta-sigma-type modulator. By combining the CS5378 with a CS3301A/02A differential amplifier and a CS5373A modulator + test DAC, a synchronous high-resolution, self-testing, single-channel measurement system can be designed quickly and easily.

Digital filter coefficients for the CS5378 FIR and IIR filters are included on-chip for a simple setup, or they can be programmed for custom applications. Selectable digital filter decimation ratios produce output word rates from 4000 SPS to 1 SPS, resulting in measurement bandwidths ranging from 1600 Hz down to 400 mHz when using the on-chip coefficient sets.

The CS5378 includes integrated peripherals to simplify system design: a low-jitter PLL for standard clock or Manchester inputs, offset and gain corrections, a test DAC bit stream generator, a time break controller, and eight general-purpose I/O pins.

ORDERING INFORMATION

See [page 86](#).

