CS5571

±2.5 V / 5 V, 100 kSps, 16-bit, High-throughput ΔΣ ADC

Features

- Single-ended Analog Input
- On-chip Buffers for High Input Impedance
- Conversion Time = 10 µS
- Settles in One Conversion
- Linearity Error = 0.0008%
- Signal-to-Noise = 92 dB
- S/(N + D) = 91 dB
- DNL = ±0.1 LSB Max.
- Simple three/four-wire serial interface
- Power Supply Configurations:
  - Analog: +5V/GND; IO: +1.8V to +3.3V
  - Analog: ±2.5V; IO: +1.8V to +3.3V
- Power Consumption:
  - ADC Input Buffers On: 85 mW
  - ADC Input Buffers Off: 60 mW

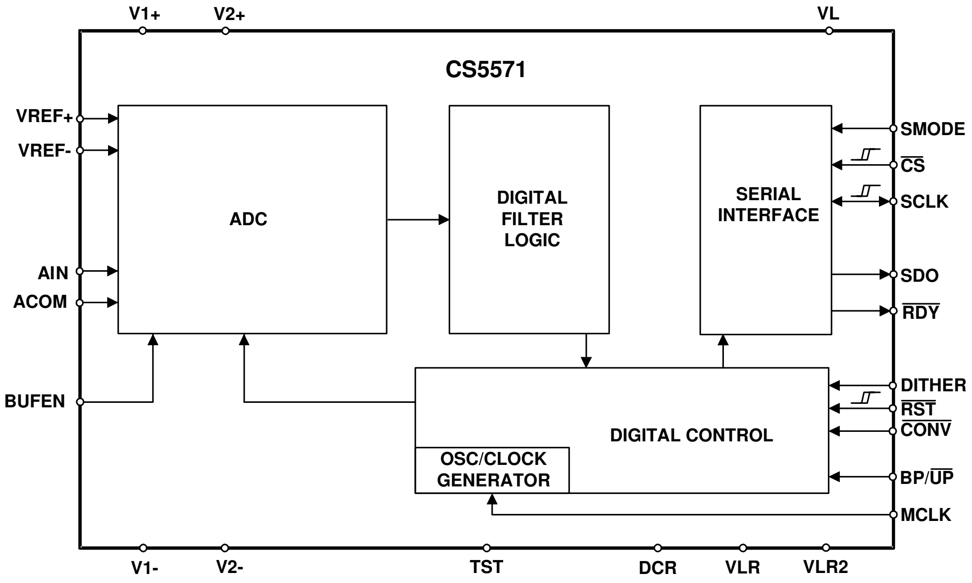
General Description

The CS5571 is a single-channel, 16-bit analog-to-digital converter capable of 100 kSps conversion rate. The input accepts a single-ended analog input signal. On-chip buffers provide high input impedance for both the AIN input and the VREF+ input. This significantly reduces the drive requirements of signal sources and reduces errors due to source impedances. The CS5571 is a delta-sigma converter capable of switching multiple input channels at a high rate with no loss in throughput. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion. The converter's 16-bit data output is in serial format, with the serial port acting as either a master or a slave. The converter is designed to support bipolar, ground-referenced signals when operated from ±2.5V analog supplies.

The converter can operate from an analog supply of 0-5V or from ±2.5V. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

ORDERING INFORMATION:

See *Ordering Information* on page 34.



Preliminary Product Information

This document contains information for a new product.
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1. CHARACTERISTICS AND SPECIFICATIONS

- Min / Max characteristics and specifications are guaranteed over the specified operating conditions.
- Typical characteristics and specifications are measured at nominal supply voltages and T_A = 25°C.
- VLR = 0 V. All voltages measured with respect to 0 V.

ANALOG CHARACTERISTICS

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%; VL -VLR = 3.3 V, ±5%; VREF = (VREF+) - (VREF-) = 4.096V; MCLK = 16 MHz; SMODE = VL. DITHER = VL unless otherwise stated; BUFEN = V1+ unless otherwise stated. Connected per Figure 6. Bipolar mode unless otherwise stated.

Parameter		Min	Typ	Max	Unit
Accuracy					
Linearity Error		-	0.0008	-	±%FS
Differential Linearity Error	(Note 1)	-	-	±0.1	LSB_{16}
Positive Full-scale Error		-	1.0	-	%FS
Negative Full-scale Error		-	1.0	-	%FS
Full-scale Drift	(Note 2, 3)	-	±1	-	LSB_{16}
Bipolar Offset	(Note 2)	-	±15	-	LSB_{16}
Bipolar Offset Drift	(Note 2, 3)	-	±1	-	LSB_{16}
Noise	(Note 4)	-	36	-	µVrms
Dynamic Performance					
Peak Harmonic or Spurious Noise	1 kHz, -0.5 dB Input 12 kHz, -0.5 dB Input	- -	-96 -96	- -	dB dB
Total Harmonic Distortion	1 kHz, -0.5 dB Input	-	-94	-82	dB
Signal-to-Noise		91	92	-	dB
S/(N + D) Ratio	-0.5 dB Input, 1 kHz -60 dB Input, 1 kHz	- -	91 32	- -	dB dB
-3 dB Input Bandwidth	(Note 5)	-	84	-	kHz

1. No missing codes is guaranteed at 16 bits resolution over the specified temperature range.
2. One LSB is equivalent to VREF ÷ 2^{16} or 4.096 ÷ 65536 = 62.5 µV.
3. Total drift over specified temperature range after reset at power-up, at 25º C.
4. With DITHER off the output will be dominated by quantization.
5. Scales with MCLK.

ANALOG CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%; VL -VLR = 3.3 V, ±5%; VREF = (VREF+) - (VREF-) = 4.096V; MCLK = 16 MHz; SMODE = VL. DITHER = VL unless otherwise stated; BUFEN = V1+ unless otherwise stated. Connected per Figure 6.

Parameter		Min	Typ	Max	Unit
Analog Input					
Analog Input Range	Unipolar Bipolar		0 to +VREF / 2 ±VREF / 2		V V
Input Capacitance		-	10	-	pF
CVF Current (Note 6)	AIN Buffer On (BUFEN = V+) AIN Buffer Off (BUFEN = V-) ACOM	- - -	600 130 130	- - -	nA µA µA
Voltage Reference Input					
Voltage Reference Input Range (VREF+) – (VREF-)	(Note 7)	2.4	4.096	4.2	V
Input Capacitance		-	10	-	pF
CVF Current	VREF+ Buffer On (BUFEN = V+) VREF+ Buffer Off (BUFEN = V-) VREF-	- - -	3 1 1	- - -	µA mA mA
Power Supplies					
DC Power Supply Currents	I_{V1} I_{V2} I_{VL}	- - -	- - -	18 1.8 0.6	mA mA mA
Power Consumption	Normal Operation Buffers On Buffers Off	- -	85 60	101 80	mW mW
Power Supply Rejection	(Note 8) V1+ , V2+ Supplies V1-, V2- Supplies	- -	80 80	- -	dB dB

6. Measured using an input signal of 1 V DC.
7. For optimum performance, VREF+ should always be less than (V+) - 0.2 volts to prevent saturation of the VREF+ input buffer.
8. Tested with 100 mVp-p on any supply up to 1 kHz. V1+ and V2+ supplies at the same voltage potential, V1- and V2- supplies at the same voltage potential.

SWITCHING CHARACTERISTICS

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Frequency	Internal Oscillator External Clock	XIN f_{clk}	12 0.5	14 16	16 16.2	MHz MHz
Master Clock Duty Cycle			40	-	60	%
Reset						
$\overline{\text{RST}}$ Low Time	(Note 9)	t_{res}	1	-	-	µs
$\overline{\text{RST}}$ rising to $\overline{\text{RDY}}$ falling	Internal Oscillator External Clock	t_{wup}	- -	120 1536	- -	µs MCLKs
Conversion						
$\overline{\text{CONV}}$ Pulse Width		t_{cpw}	4	-	-	MCLKs
BP/$\overline{\text{UP}}$ setup to $\overline{\text{CONV}}$ falling	(Note 10)	t_{scn}	0	-	-	ns
$\overline{\text{CONV}}$ low to start of conversion		t_{scn}	-	-	2	MCLKs
Perform Single Conversion ($\overline{\text{CONV}}$ high before $\overline{\text{RDY}}$ falling)		t_{bus}	20	-	-	MCLKs
Conversion Time	(Note 11) Start of Conversion to $\overline{\text{RDY}}$ falling	t_{buh}	-	-	164	MCLKs

9. Reset must not be released until the power supplies and the voltage reference are within specification.
10. BP/$\overline{\text{UP}}$ can be changed coincident to $\overline{\text{CONV}}$ falling. BP/$\overline{\text{UP}}$ must remain stable until $\overline{\text{RDY}}$ falls.
11. If $\overline{\text{CONV}}$ is held low continuously, conversions occur every 160 MCLK cycles.
    If $\overline{\text{RDY}}$ is tied to $\overline{\text{CONV}}$, conversions will occur every 162 MCLKs.
    If $\overline{\text{CONV}}$ is operated asynchronously to MCLK, a conversion may take up to 164 MCLKs.
    $\overline{\text{RDY}}$ falls at the end of conversion.

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)					
$\overline{\text{RDY}}$ falling to MSB stable	t_1	-	-2	-	MCLKs
Data hold time after SCLK rising	t_2	-	10	-	ns
Serial Clock (Out) Pulse Width (low)	t_3	50	-	-	ns
(Note 12, 13) Pulse Width (high)	t_4	50	-	-	ns
$\overline{\text{RDY}}$ rising after last SCLK rising	t_5	-	8	-	MCLKs

12. SDO and SCLK will be high impedance when $\overline{\text{CS}}$ is high. In some systems SCLK and SDO may require pull-down resistors.
13. SCLK = MCLK/2.

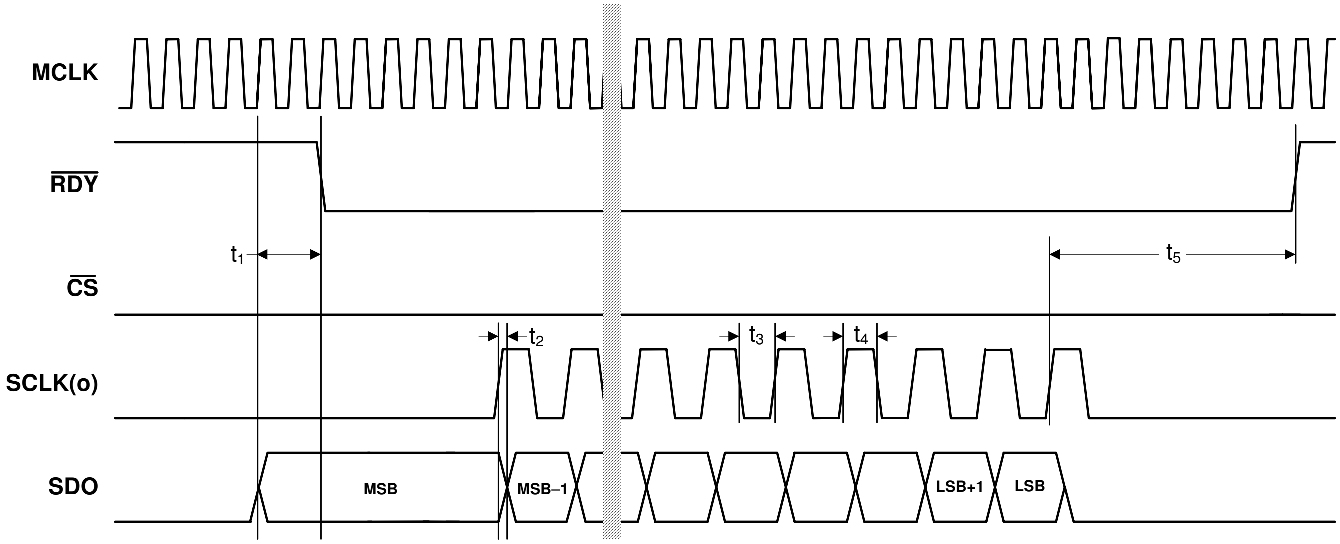

MCLK
$\overline{\text{RDY}}$
t_1
t_5
$\overline{\text{CS}}$
t_2
t_3
t_4
SCLK(o)
SDO
MSB
MSB–1
LSB+1
LSB

Figure 1. SSC Mode - Read Timing, $\overline{\text{CS}}$ remaining low (Not to Scale)

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

Parameter		Symbol	Min	Typ	Max	Unit
Serial Port Timing in SSC Mode (SMODE = VL)						
Data hold time after SCLK rising		t_7	-	10	-	ns
Serial Clock (Out) (Note 14, 15)	Pulse Width (low) Pulse Width (high)	t_8 t_9	50 50	- -	- -	ns ns
$\overline{\text{RDY}}$ rising after last SCLK rising		t_{10}	-	8	-	MCLKs
$\overline{\text{CS}}$ falling to MSB stable		t_{11}	-	10	-	ns
First SCLK rising after $\overline{\text{CS}}$ falling		t_{12}	-	8	-	MCLKs
$\overline{\text{CS}}$ hold time (low) after SCLK rising		t_{13}	10	-	-	ns
SCLK, SDO tri-state after $\overline{\text{CS}}$ rising		t_{14}	-	5	-	ns

14. SDO and SCLK will be high impedance when $\overline{\text{CS}}$ is high. In some systems SCLK and SDO may require pull-down resistors.
15. SCLK = MCLK/2.

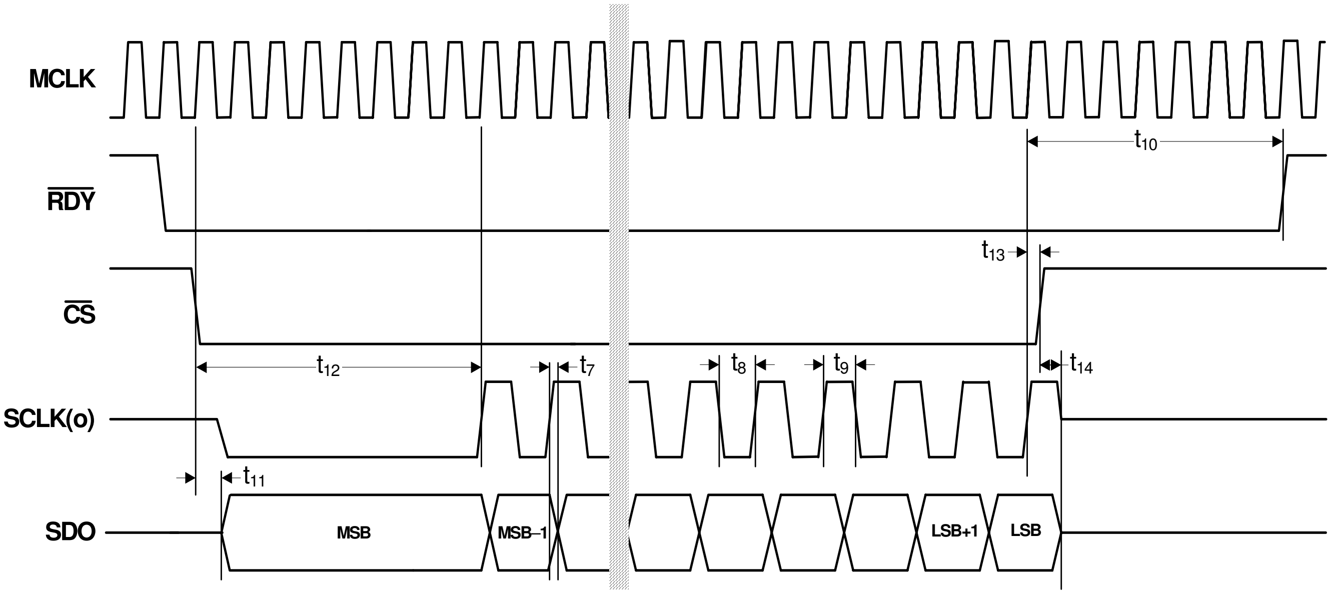


Figure 2. SSC Mode - Read Timing, $\overline{\text{CS}}$ falling after $\overline{\text{RDY}}$ falls (Not to Scale)

SWITCHING CHARACTERISTICS (CONTINUED)

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

Parameter	Symbol	Min	Typ	Max	Unit
Serial Port Timing in SEC Mode (SMODE = VLR)					
SCLK(in) Pulse Width (High)	-	30	-	-	ns
SCLK(in) Pulse Width (Low)	-	30	-	-	ns
$\overline{\text{CS}}$ hold time (high) after $\overline{\text{RDY}}$ falling	t_{15}	10	-	-	ns
$\overline{\text{CS}}$ hold time (high) after SCLK rising	t_{16}	10	-	-	ns
$\overline{\text{CS}}$ low to SDO out of Hi-Z (Note 16)	t_{17}	-	10	-	ns
Data hold time after SCLK rising	t_{18}	-	10	-	ns
Data setup time before SCLK rising	t_{19}	10	-	-	ns
$\overline{\text{CS}}$ hold time (low) after SCLK rising	t_{20}	10	-	$\frac{1}{\text{SCLK}}-10$	ns
$\overline{\text{RDY}}$ rising after SCLK falling	t_{21}	-	10	-	ns

16. SDO will be high impedance when $\overline{\text{CS}}$ is high. In some systems SDO may require a pull-down resistor.

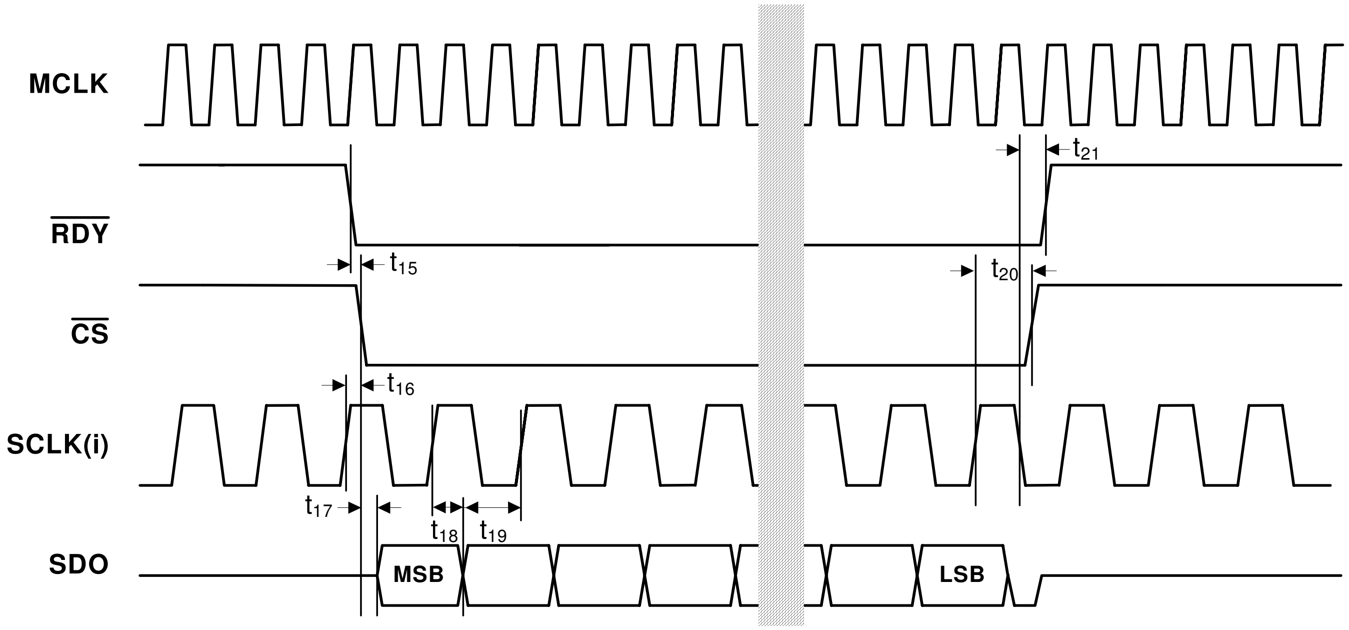


Figure 3. SEC Mode - Continuous SCLK Read Timing (Not to Scale)

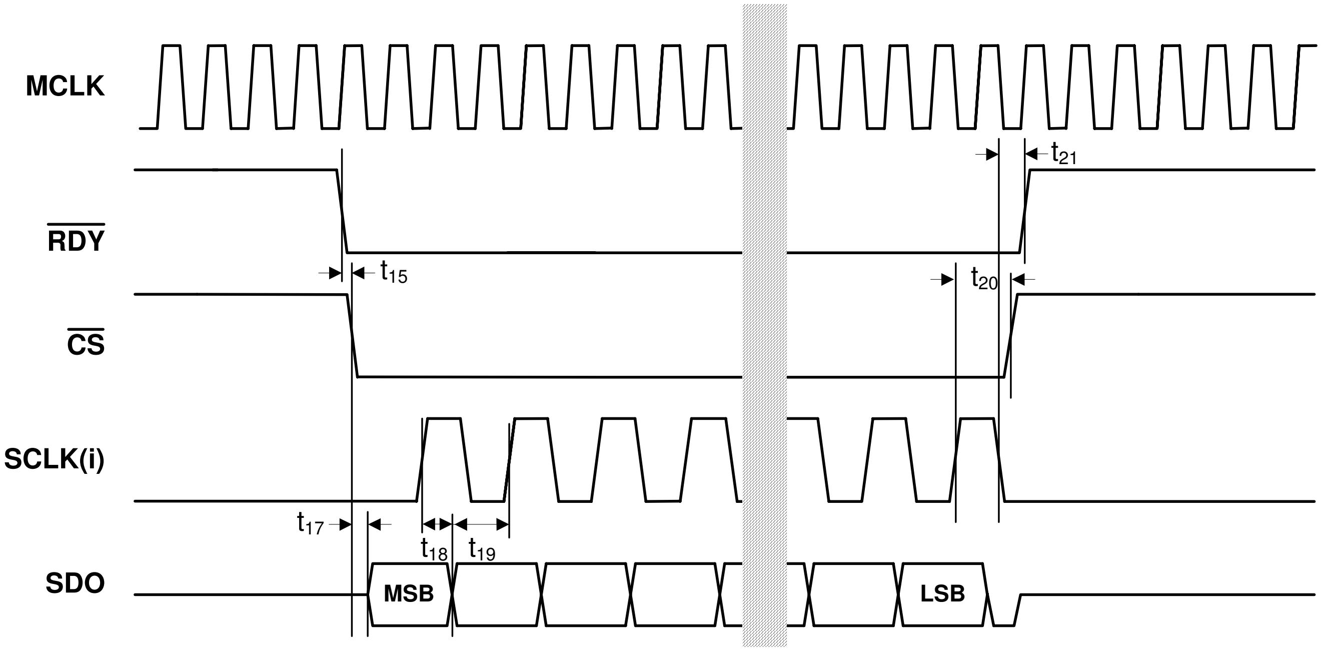

MCLK
RDY
CS
SCLK(i)
SDO
t15
t17
t18
t19
t20
t21
MSB
LSB

Figure 4. SEC Mode - Discontinuous SCLK Read Timing (Not to Scale)

DIGITAL CHARACTERISTICS

T_A = TMIN to TMAX; VL = 3.3V, ±5% or VL = 2.5V, ±5% or 1.8V, ±5%; VLR = 0V

Parameter	Symbol	Min	Typ	Max	Unit
Input Leakage Current	I_{in}	-	-	2	µA
Digital Input Pin Capacitance	C_{in}	-	3	-	pF
Digital Output Pin Capacitance	C_{out}	-	3	-	pF

GUARANTEED LOGIC LEVELS

T_A = -40 to +85 °C; V1+ = V2+ = +2.5 V, ±5%; V1- = V2- = -2.5 V, ±5%;
VL - VLR = 3.3 V, ±5%, 2.5 V, ±5%, or 1.8 V, ±5%
Input levels: Logic 0 = 0V = Low; Logic 1 = VD+ = High; CL = 15 pF.

			Guaranteed Limits				
Parameter	**Sym**	**VL**	**Min**	**Typ**	**Max**	**Unit**	**Conditions**
Logic Inputs							
Minimum High-level Input Voltage:	V_{IH}	3.3	1.9			V	
		2.5	1.6				
		1.8	1.2				
Maximum Low-level Input Voltage:	V_{IL}	3.3			1.1	V	
		2.5			0.95		
		1.8			0.6		
Logic Outputs							
Minimum High-level Output Voltage:	V_{OH}	3.3	2.9			V	I_{OH} = -2 mA
		2.5	2.1				
		1.8	1.65				
Maximum Low-level Output Voltage:	V_{OL}	3.3			0.36	V	I_{OH} = -2 mA
		2.5			0.36		
		1.8			0.44		

RECOMMENDED OPERATING CONDITIONS

(VLR = 0V, see Note 17)

Parameter	Symbol	Min	Typ	Max	Unit
Single Analog Supply					
DC Power Supplies: (Note 17)					
V1+	V1+	4.75	5.0	5.25	V
V2+	V2-	4.75	5.0	5.25	V
V1-	V1+	-	0	-	V
V2-	V2-	-	0	-	V
Dual Analog Supplies					
DC Power Supplies: (Note 17)					
V1+	V1+	+2.375	+2.5	+2.625	V
V2+	V2-	+2.375	+2.5	+2.625	V
V1-	V1+	-2.375	-2.5	-2.625	V
V2-	V2-	-2.375	-2.5	-2.625	V
Analog Reference Voltage (Note 18) [VREF+] – [VREF-]	VREF	2.4	4.096	4.2	V

17. The logic supply can be any value VL – VLR = +1.71 to +3.465 volts as long as VLR ≥ V2- and VL ≤ 3.465 V.
18. The differential voltage reference magnitude is constrained by the V1+ or V1- supply magnitude.

ABSOLUTE MAXIMUM RATINGS

(VLR = 0V)

Parameter	Symbol	Min	Typ	Max	Unit
DC Power Supplies:					
[V1+] – [V1-] (Note 19)	-	0	-	5.5	V
VL + [|V1-|] (Note 20)	-	0	-	6.1	V
Input Current, Any Pin Except Supplies (Note 21)	I_{IN}	-	-	±10	mA
Analog Input Voltage (AIN and VREF pins)	V_{INA}	(V1-) – 0.3	-	(V1+) + 0.3	V
Digital Input Voltage	V_{IND}	VLR – 0.3	-	VL + 0.3	V
Storage Temperature	T_{stg}	-65	-	150	°C

Notes:
19. V1+ = V2+; V1- = V2-
20. V1- = V2-
21. Transient currents of up to 100 mA will not cause SCR latch-up.

WARNING:

Recommended Operating Conditions indicate limits to which the device is functionally operational. Absolute Maximum Ratings indicate limits beyond which permanent damage to the device may occur. The Absolute Maximum Ratings are stress ratings only and the device should not be operated at these limits. Operation at conditions beyond the Recommended Operating Conditions may affect device reliability, and functional operation beyond Recommended Operating Conditions is not implied. Performance specifications are intended for the conditions specified for each table in the Characteristics and Specifications section.

2. OVERVIEW

The CS5571 is a 16-bit analog-to-digital converter capable of 100 kSps conversion rate. The analog input accepts a single-ended input with a magnitude of ±VREF / 2 volts. The device is capable of switching multiple input channels at a high rate with no loss in throughput. The ADC uses a low-latency digital filter architecture. The filter is designed for fast settling and settles to full accuracy in one conversion.

The converter is a serial output device. The serial port can be configured to function as either a master or a slave.

The converter can operate from an analog supply of 5V or from ±2.5V. The digital interface supports standard logic operating from 1.8, 2.5, or 3.3 V.

The CS5571 may convert at rates up to 100 kSps when operating from a 16 MHz input clock.

3. THEORY OF OPERATION

The CS5571 converter provides high-performance measurement of DC or AC signals. The converter can be used to perform single conversions or continuous conversions upon command. Each conversion is independent of previous conversions and settles to full specified accuracy, even with a full-scale input voltage step. This is due to the converter architecture which uses a combination of a high-speed delta-sigma modulator and a low-latency filter architecture.

Once power is established to the converter, a reset must be performed. A reset initializes the internal converter logic.

If $\overline{\text{CONV}}$ is held low, the converter will convert continuously with $\overline{\text{RDY}}$ falling every 160 MCLKs. This is equivalent to 100 kSps if MCLK = 16.0 MHz. If $\overline{\text{CONV}}$ is tied to $\overline{\text{RDY}}$, a conversion will occur every 162 MCLKs. If $\overline{\text{CONV}}$ is operated asynchronously to MCLK, it may take up to 164 MCLKs from $\overline{\text{CONV}}$ falling to $\overline{\text{RDY}}$ falling.

Multiple converters can operate synchronously if they are driven by the same MCLK source and $\overline{\text{CONV}}$ to each converter falls on the same MCLK falling edge. Alternately, $\overline{\text{CONV}}$ can be held low and all devices can be synchronized if they are reset with $\overline{\text{RST}}$ rising on the same falling edge of MCLK.

The output coding of the conversion word is a function of the BP/$\overline{\text{UP}}$ pin.

3.1 Converter Operation

The converter should be reset after the power supplies and voltage reference are stable.

The CS5571 converts at 100 kSps when synchronously operated ($\overline{\text{CONV}}$ = VLR) from a 16.0 MHz master clock. Conversion is initiated by taking $\overline{\text{CONV}}$ low. A conversion lasts 160 master clock cycles, but if $\overline{\text{CONV}}$ is asynchronous to MCLK there may be an uncertainty of 0-4 MCLK cycles after $\overline{\text{CONV}}$ falls to when a conversion actually begins. This may extend the throughput to 164 MCLKs per conversion.

When the conversion is completed, the output word is placed into the serial port and $\overline{\text{RDY}}$ goes low. To convert continuously, $\overline{\text{CONV}}$ should be held low. In continuous conversion mode with $\overline{\text{CONV}}$ held low, a conversion is performed in 160 MCLK cycles. Alternately $\overline{\text{RDY}}$ can be tied to $\overline{\text{CONV}}$ and a conversion will occur every 162 MCLK cycles.

To perform only one conversion, $\overline{\text{CONV}}$ should return high at least 20 master clock cycles before $\overline{\text{RDY}}$ falls.

Once a conversion is completed and RDY falls, RDY will return high when all the bits of the data word are emptied from the serial port or if the conversion data is not read and CS is held low, RDY will go high two MCLK cycles before the end of conversion. RDY will fall at the end of the next conversion when new data is put into the port register.

See *Serial Port* on page 26 for information about reading conversion data.

Conversion performance can be affected by several factors. These include the choice of clock source for the chip, the timing of CONV, the setting of the DITHER function, and the choice of the serial port mode.

The converter can be operated from an internal oscillator. This clock source has greater jitter than an external crystal-based clock. Jitter may not be an issue when measuring DC signals, or very-low-frequency AC signals, but can become an issue for higher frequency AC signals. For maximum performance when digitizing AC signals, a low-jitter MCLK should be used.

To achieve the highest resolution when measuring a DC signal with a single conversion the DITHER function should be off. If averaging is to be performed with multiple conversions of a DC signal, DITHER should be on. To maximize performance, the CONV pin should be held low in the continuous conversion state to perform multiple conversions, or CONV should occur synchronous to MCLK, falling when MCLK falls.

If the converter is operated at maximum throughput, the SSC serial port mode is less likely to cause interference to measurements as the SCLK output is synchronized to the MCLK. Alternately, any interference due to serial port clocking can also be minimized if data is read in the SEC serial port mode when a conversion is not in progress.

3.2 Clock

The CS5571 can be operated from its internal oscillator or from an external master clock. The state of MCLK determines which clock source will be used. If MCLK is tied low, the internal oscillator will start and be used as the clock source for the converter. If an external CMOS-compatible clock is input into MCLK, the converter will power down the internal oscillator and use the external clock. If the MCLK pin is held high, the internal oscillator will be held in the stopped state. The MCLK input can be held high to delete clock cycles to aid in synchronizing multiple converters in different phase relationships.

The internal oscillator can be used if the signals to be measured are essentially DC. The internal oscillator exhibits jitter at about 500 picoseconds rms. If the CS5571 is used to digitize AC signals, an external low-jitter clock source should be used.

If the internal oscillator is used as the clock for the CS5571, the maximum conversion rate will be dictated by the oscillator frequency.

If driven from an external MCLK source, the fast rise and fall times of the MCLK signal can result in clock coupling from the internal bond wire of the IC to the analog input. Adding a 50 ohm resistor on the external MCLK source significantly reduces this effect.

3.3 Voltage Reference

The voltage reference for the CS5571 can range from 2.4 volt to 4.2 volts. A 4.096 volt reference is required to achieve the specified signal-to-noise performance. Figure 6 and Figure 7 illustrate the connection of the voltage reference with either a single +5 V analog supply or with ±2.5 V.

For optimum performance, the voltage reference device should be one that provides a capacitor connection to provide a means of noise filtering, or the output should include some type of bandwidth-limiting filter.

Some 4.096 volt reference devices need only 5 volts total supply for operation and can be connected as shown in Figure 6 or Figure 7. The reference should have a local bypass capacitor and an appropriate output capacitor.

Some older 4.096 voltage reference designs require more headroom and must operate from an input voltage of 5.5 to 6.5 volts. If this type of voltage reference is used ensure that when power is applied to the system, the voltage reference rise time is slower than the rise time of the V1+ and V1- power supply voltage to the converter. An example circuit to slow the output startup time of the reference is illustrated in Figure 5.

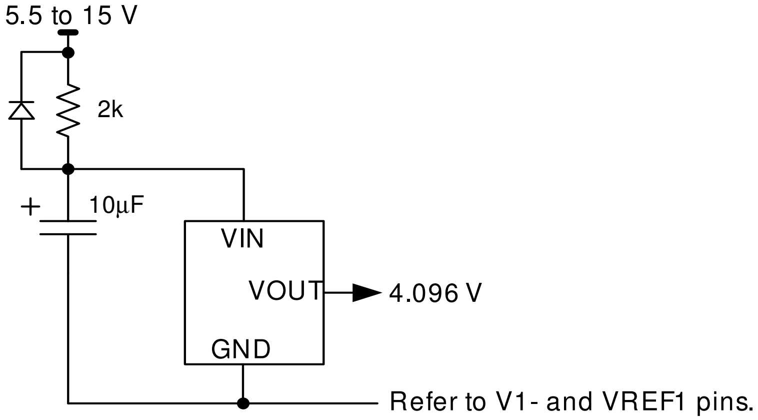


Figure 5. Voltage Reference Circuit

3.4 Analog Input

The analog input of the converter is single-ended with a full-scale input of ±2.048 volts, relative to the ACOM pin.. This is illustrated in Figure 6 and Figure 7. These diagrams also illustrate a differential buffer amplifier configuration for driving the CS5571.

The capacitors at the outputs of the amplifiers provide a charge reservoir for the dynamic current from the A/D inputs while the resistors isolate the dynamic current from the amplifier. The amplifiers can be powered from higher supplies than those used by the A/D but precautions should be taken to ensure that the op-amp output voltage remains within the power supply limits of the A/D, especially under start-up conditions.

3.5 Output Coding Format

The reference voltage directly defines the input voltage range in both the unipolar and bipolar configurations. In the unipolar configuration (BP/$\overline{\text{UP}}$ low), the first code transition occurs 0.5 LSB above zero, and the final code transition occurs 1.5 LSBs below VREF. In the bipolar configuration (BP/$\overline{\text{UP}}$ high), the first code transition occurs 0.5 LSB above -VREF and the last transition occurs 1.5 LSBs below +VREF. See Table 1 for the output coding of the converter.

Table 1. Output Coding, Two's Complement

Bipolar Input Voltage	Two's Complement
>(VREF-1.5 LSB)	7F FF
VREF-1.5 LSB	7F FF 7F FE
-0.5 LSB	00 00 FF FF
-VREF+0.5 LSB	80 01 80 00
<(-VREF+0.5 LSB)	80 00

NOTE: VREF = [(VREF+) - (VREF-)] / 2

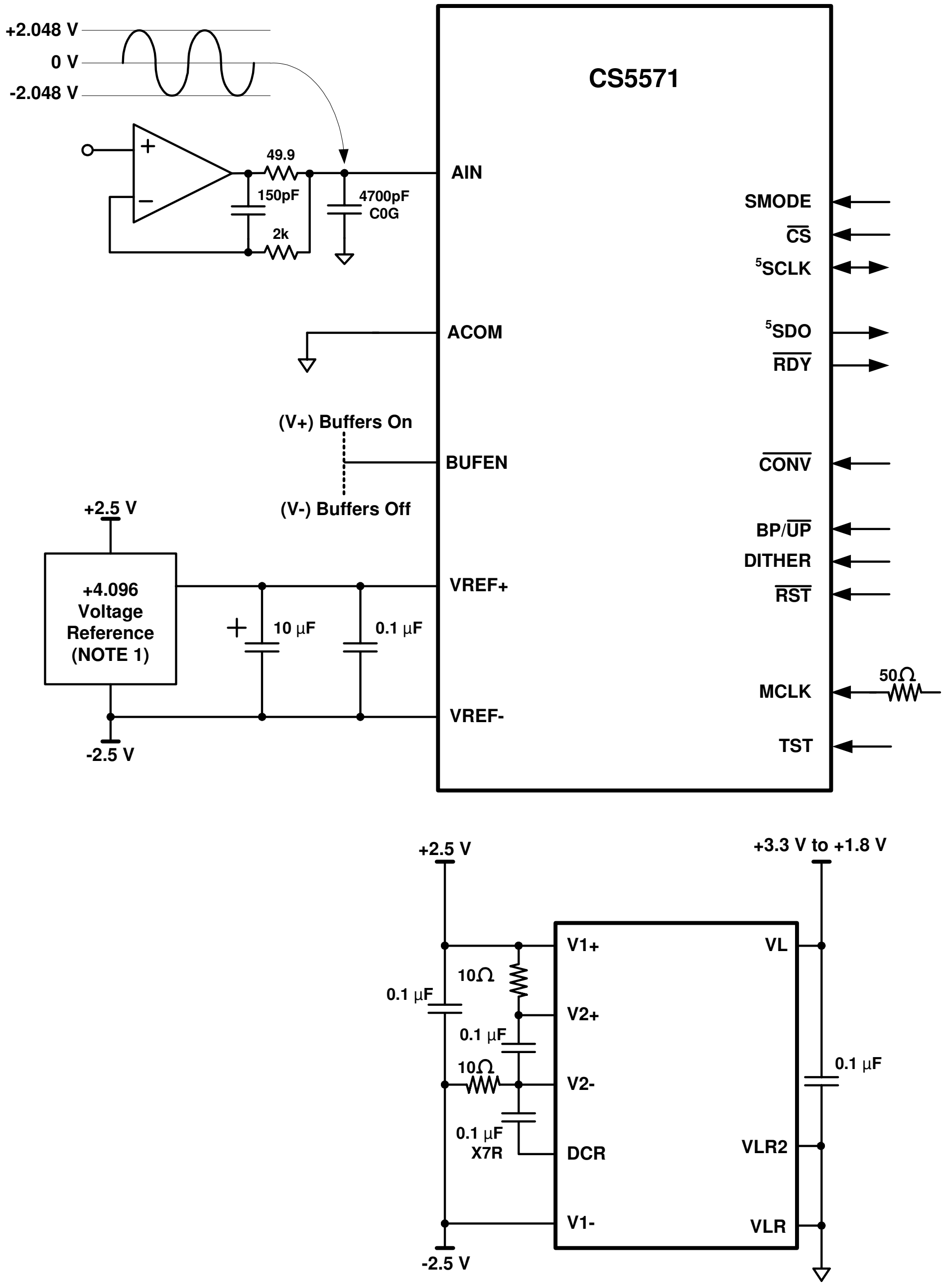
Table 2. Output Coding, Offset Binary

Unipolar Input Voltage	Offset Binary
>(VREF-1.5 LSB)	FF FF
VREF-1.5 LSB	FF FF FF FE
(VREF/2)-0.5 LSB	80 00 7F FF
+0.5 LSB	00 01 00 00
<(+0.5 LSB)	00 00

NOTE: VREF = [(VREF+) - (VREF-)] / 2

3.6 Typical Connection Diagrams

The following figure depicts the CS5571 powered from bipolar analog supplies, +2.5 V and - 2.5 V.

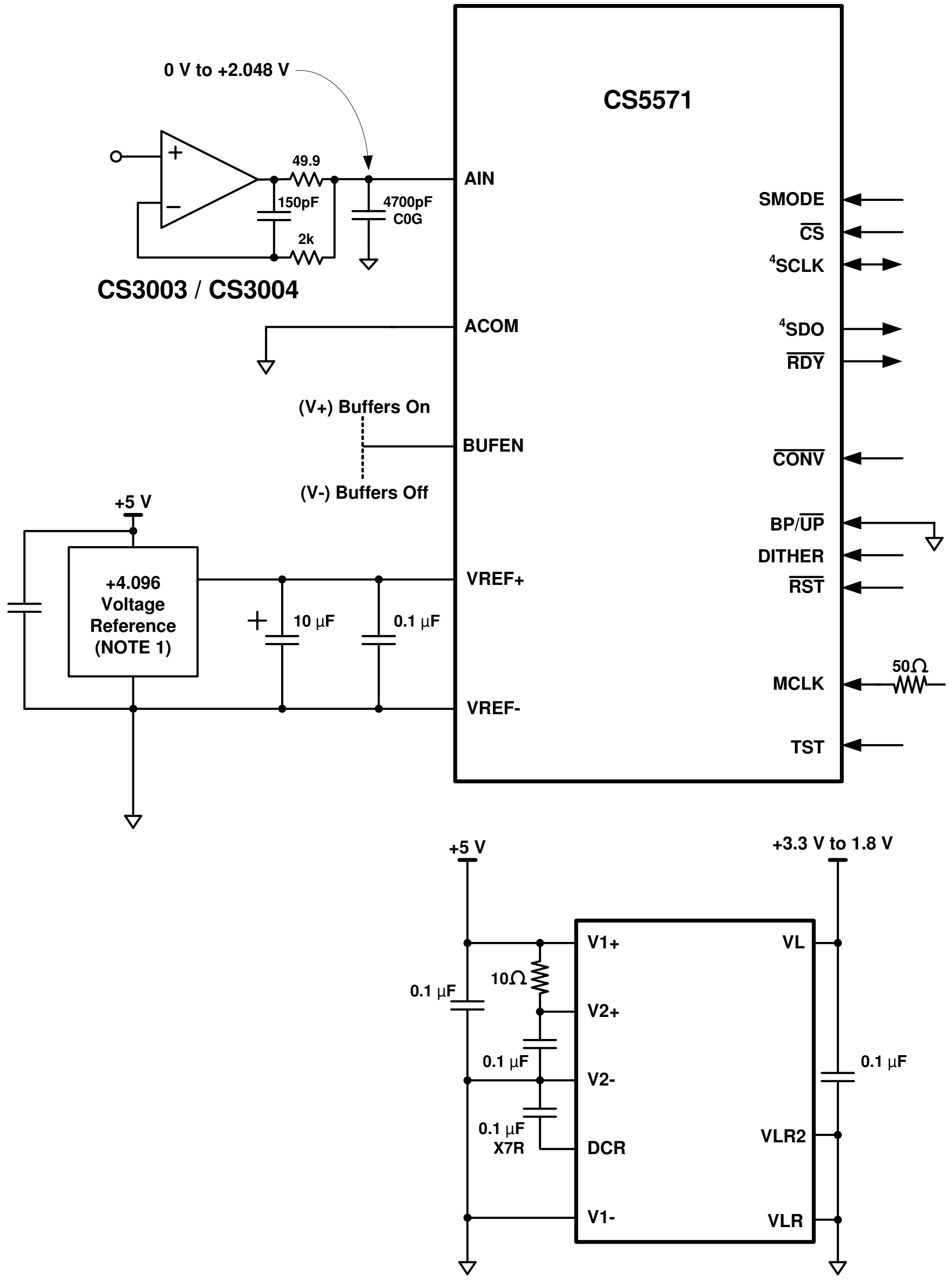

+2.048 V
0 V
-2.048 V
+
−
49.9
150pF
2k
4700pF
C0G
CS5571
AIN
ACOM
(V+) Buffers On
BUFEN
(V-) Buffers Off
+2.5 V
+4.096
Voltage
Reference
(NOTE 1)
+
10 µF
0.1 µF
VREF+
VREF-
-2.5 V
SMODE
CS
5SCLK
5SDO
RDY
CONV
BP/UP
DITHER
RST
MCLK
50Ω
TST
+2.5 V
+3.3 V to +1.8 V
V1+
VL
10Ω
0.1 µF
V2+
0.1 µF
10Ω
V2-
0.1 µF
X7R
DCR
VLR2
0.1 µF
V1-
VLR
-2.5 V

NOTES

1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. The ±2.5 V supplies should also be bypassed to ground at the converter.
4. VLR and the power supply ground for the ±2.5 V should be connected to the same ground plane under the chip.
5. SCLK and SDO may require pull-down resistors in some applications.

Figure 6. CS5571 Configured Using ±2.5V Analog Supplies

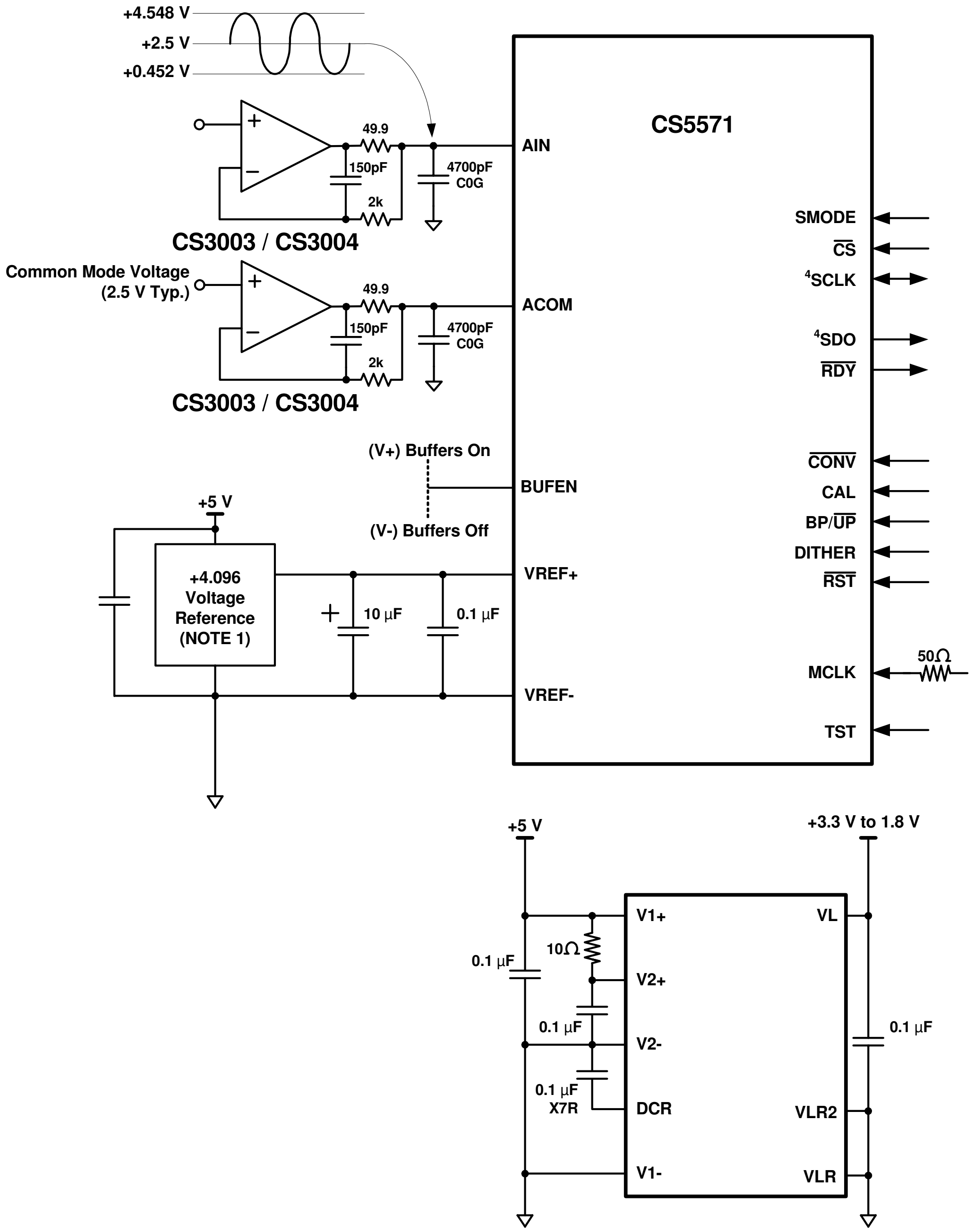
The following figure depicts the CS5571 part powered from a single 5V analog supply and configured for unipolar measurement.


CS5571
0 V to +2.048 V
49.9
150pF
2k
4700pF
C0G
CS3003 / CS3004
AIN
ACOM
(V+) Buffers On
BUFEN
(V-) Buffers Off
+5 V
+4.096
Voltage
Reference
(NOTE 1)
10 µF
0.1 µF
VREF+
VREF-
SMODE
CS
4SCLK
4SDO
RDY
CONV
BP/UP
DITHER
RST
MCLK
50Ω
TST
+5 V
+3.3 V to 1.8 V
V1+
V2+
V2-
DCR
V1-
VL
VLR2
VLR
10Ω
0.1 µF
0.1 µF
0.1 µF
X7R
0.1 µF

NOTES
1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. V1-, V2-, and VLR should be connected to the same ground plane under the chip.
4. SCLK and SDO may require pull-down resistors in some applications.

Figure 7. CS5571 Configured for Unipolar Measurement Using a Single 5V Analog Supply

The following figure depicts the CS5571 part powered from a single 5V analog supply and configured for bipolar measurement, referenced to a common mode voltage of 2.5 V.


+4.548 V
+2.5 V
+0.452 V
CS5571
49.9
150pF
4700pF
C0G
2k
AIN
CS3003 / CS3004
Common Mode Voltage
(2.5 V Typ.)
49.9
150pF
4700pF
C0G
2k
ACOM
CS3003 / CS3004
SMODE
CS
4SCLK
4SDO
RDY
(V+) Buffers On
BUFEN
(V-) Buffers Off
CONV
CAL
BP/UP
DITHER
RST
+5 V
+4.096
Voltage
Reference
(NOTE 1)
VREF+
10 µF
0.1 µF
VREF-
MCLK
50Ω
TST
+5 V
+3.3 V to 1.8 V
V1+
VL
10Ω
0.1 µF
V2+
0.1 µF
V2-
0.1 µF
0.1 µF
X7R
DCR
VLR2
V1-
VLR

NOTES

1. See Section 3.3 Voltage Reference for information on required voltage reference performance criteria.
2. Locate capacitors so as to minimize loop length.
3. V1-, V2-, and VLR should be connected to the same ground plane under the chip.
4. SCLK and SDO may require pull-down resistors in some applications.

Figure 8. CS5571 Configured for Bipolar Measurement Using a Single 5V Analog Supply

3.7 AIN & VREF Sampling Structures

The CS5571 uses on-chip buffers on the AIN and VREF+ inputs. Buffers provide much higher input impedance and therefore reduce the amount of drive current required from an external source. This helps minimize errors.

The Buffer Enable (BUFEN) pin determines if the on-chip buffers are used or not. If the BUFEN pin is connected to the V1+ supply, the buffers will be enabled. If the BUFEN pin is connected to the V1- pin, the buffers are off. The converter will consume about 30 mW less power when the buffers are off, but the input impedances of AIN, ACOM and VREF+ will be significantly less than with the buffers enabled.

3.8 Converter Performance

The CS5571 achieves excellent differential nonlinearity (DNL) as shown in figures 9 and 10. Figure 9 illustrates the code widths on a typical scale of ±1 LSB. Figure 10 illustrates a zoom view of figure 9 on a scale of ±0.1 LSB. Figure 10 also includes a DNL error histogram that indicates that the errors are equally distributed about the perfect code size; and most codes are accurate within ±0.01 LSB.

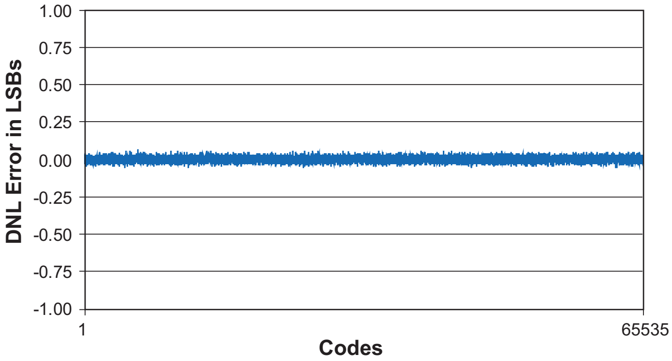


Figure 9. CS5571 DNL Plot

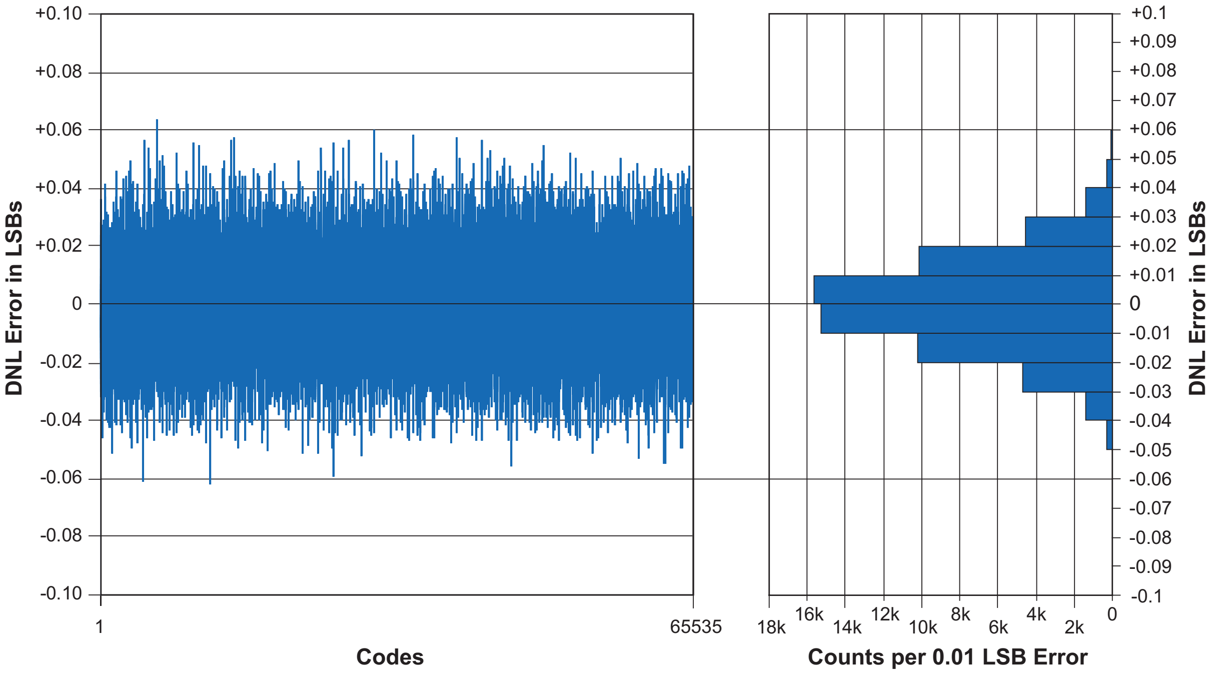


Figure 10. CS5581 DNL Error Plot with DNL Histogram

Figures 11, 12, and 13 indicate the spectral performance of the CS5571 with a 0 dB, -6 dB and - 12 dB 5.55 kHz input signal. In each case, the captured data was windowed with a seven-term window function that exhibits 4.3 dB of attenuation before being processed by the FFT.

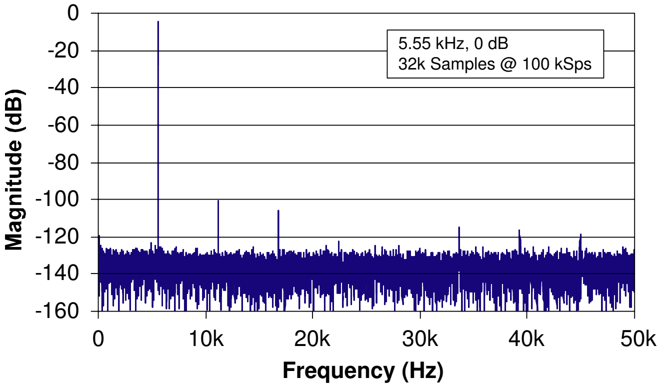


Figure 11. Spectral Performance, 0 dB

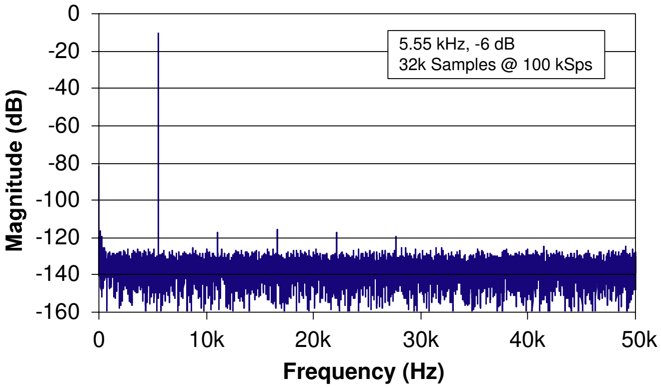


Figure 12. Spectral Performance, -6 dB

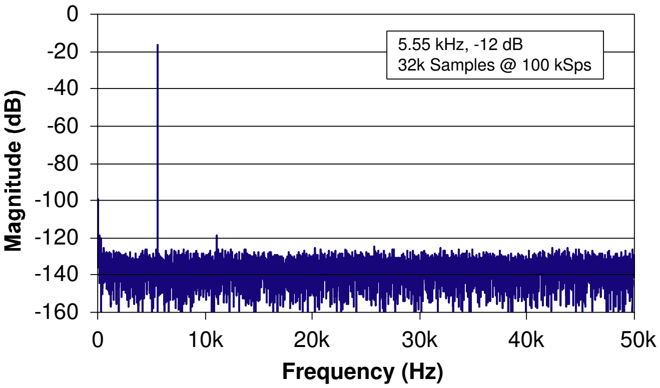


Figure 13. Spectral Performance, -12 dB

Figures 14 and 15 illustrate the small signal performance of the CS5571 with a 5.55 kHz signal at -80 dB down. Figure 14 is with DITHER on and Figure 15 is with DITHER off. At -80 dB the signal is 1/10,000 of full scale, having a peak-to-peak magnitude of only a few codes. For small signals, DNL errors and quantization errors can introduce distortion because the error in the code size, or the quantization error without adequate dither, are a much greater percentage of the signal than with a full-scale input. Figure 15, with DITHER off, illustrates that distortion components can be introduced when there is not adequate dither to randomize the quantization error.

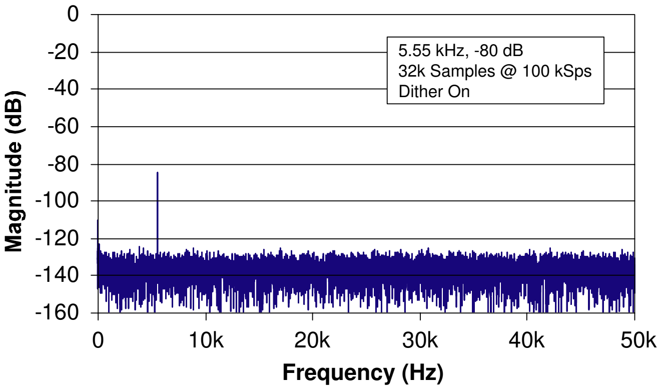


Figure 14. Spectral Performance, -80 dB Dither On

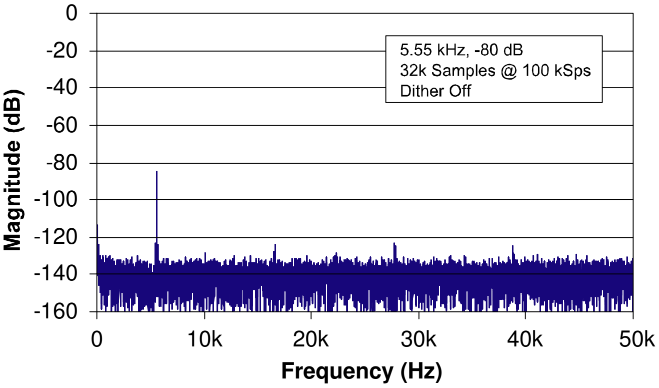


Figure 15. Spectral Performance, -80 dB Dither Off

Figures 16 and 17 illustrate DITHER on and DITHER off with a 5.55 kHz input at -100 dB. At -100 dB the signal is only about 41 microvolts peak to peak. This is less than the one code width which is about 62.5 microvolts.

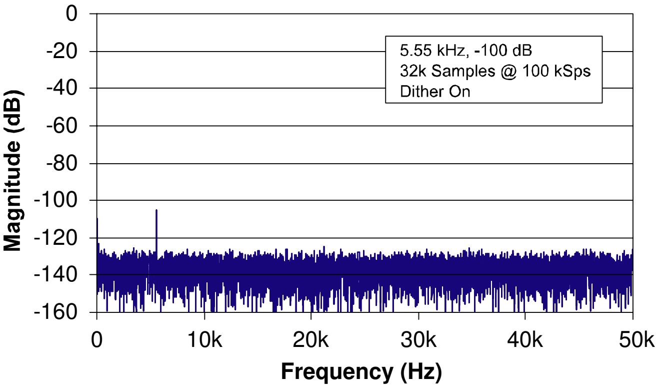


Figure 16. Spectral Performance, -100 dB Dither On

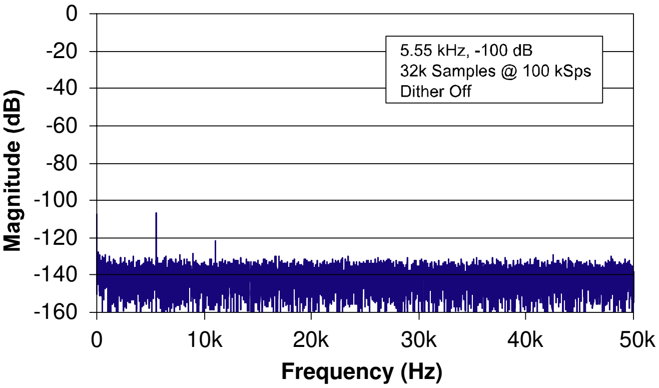


Figure 17. Spectral Performance, -100 dB Dither Off

Figure 18 illustrates a test signal of 5.55 kHz, 116.3 dB down, which is only 6.3 microvolts peak to peak, or about 1/10 of a code width. The converter can reliably digitize this signal because of its excellent DNL and proper dither.

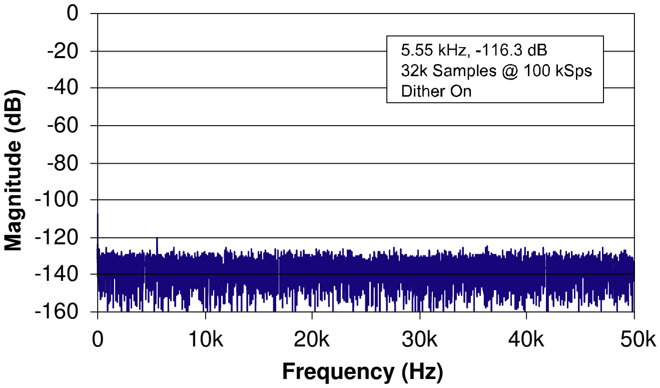


Figure 18. Spectral Performance, -116.3 dB Dither On

Figure 19 is a spectral plot of the converter with its input grounded. The spectral information is on a logarithmic frequency axis as this illustrates the very low frequency behavior of the converter. Figure 19 was produced from averaging the results of 16 FFT outputs using 2 million samples each. This plot also illustrates that the converter noise floor is free of spurious components that may be present in other converters due to on-chip digital interference.

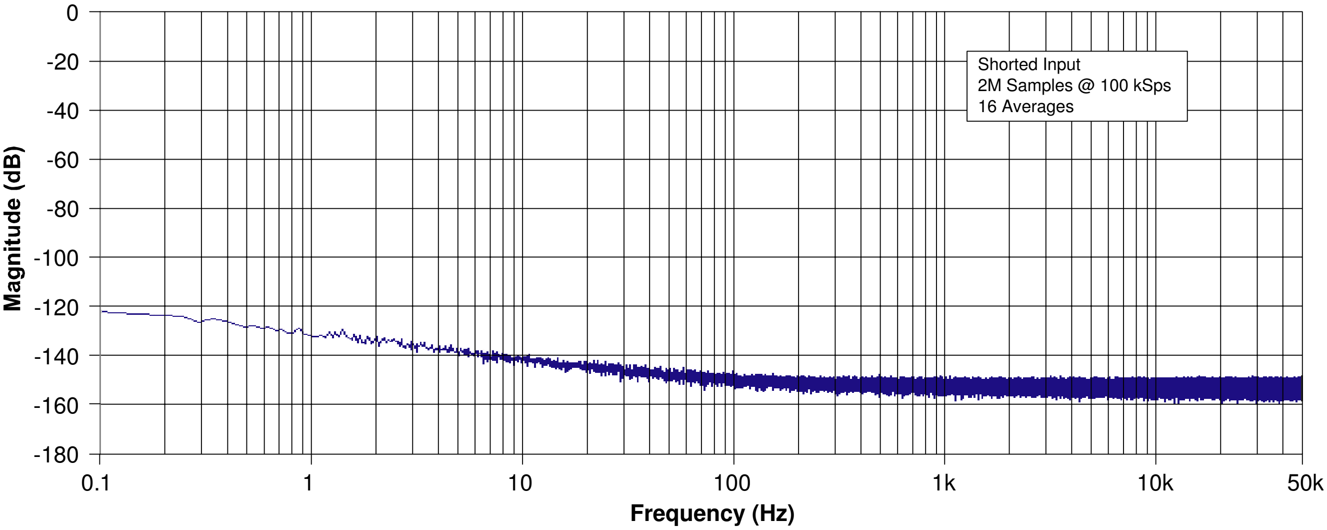


Figure 19. Spectral Plot of Noise with Shorted Input

Figure 20 illustrates a noise histogram of 4096 samples with the input signal adjusted to almost the exact center of a code with DITHER on. Figure 21 illustrates a noise histogram of 4096 samples with the input signal at the center of a code with DITHER off.

Notice that with a signal at the center of a code that the converter outputs the same code over 96% of the time. Figures 22 and 23 illustrate the noise histogram, DITHER on and then DITHER off with the input signal at a code boundary. Notice that in the DITHER off case the converter only exhibits two codes of noise.

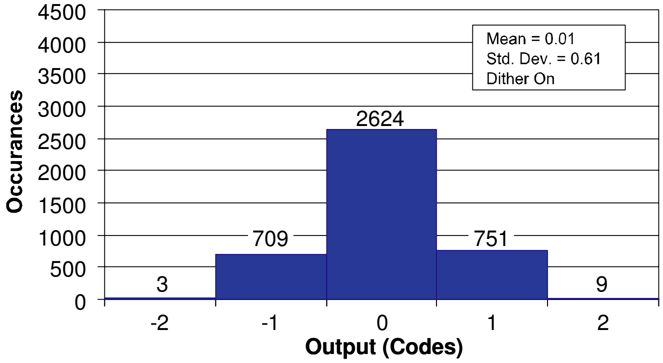


Figure 20. Noise Histogram, 4096 Samples Dither On, Code Center

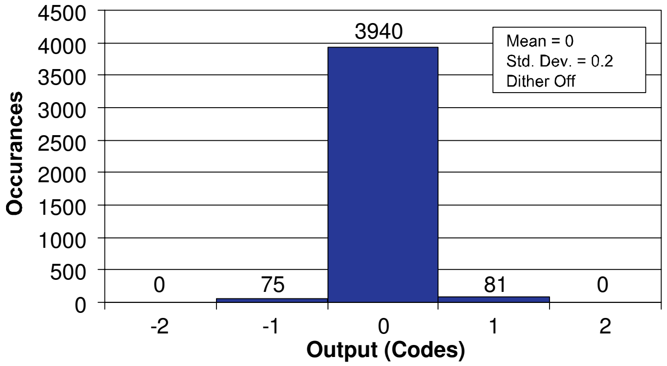


Figure 21. Noise Histogram, 4096 Samples Dither Off, Code Center

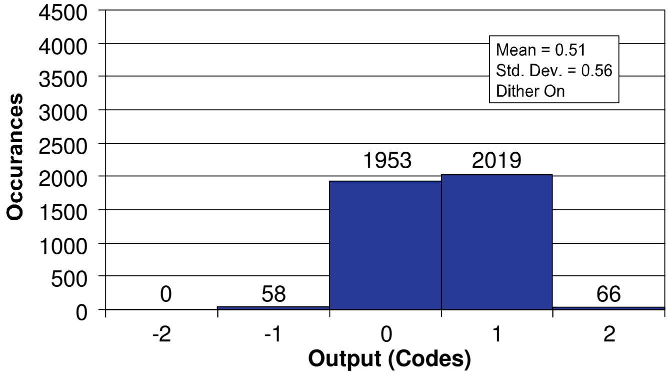


Figure 22. Noise Histogram, 4096 Samples Dither On, Input at Code Boundary

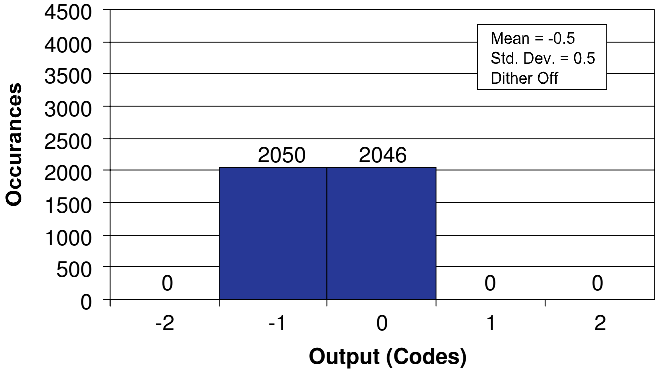


Figure 23. Noise Histogram, 4096 Samples Dither Off, Input at Code Boundary

3.9 DITHER

From the performance plots, one should conclude that the best AC performance for small signals occurs with DITHER on. For capturing multiple samples and performing averaging, DITHER should also be on because the dither will randomize the quantization noise of the converter and provide improved accuracy. However, if only one conversion is to be taken on a DC input, DITHER should be set to off. With DITHER off, the converter exhibits only two codes of noise if the signal is at any point other than the exact center of a code. This means that with DITHER off the converter will nominally yield over 32,000 noise-free counts.

3.10 Digital Filter Characteristics

The digital filter is designed for fast settling, therefore it exhibits very little in-band attenuation. The filter attenuation is 1.040 dB at 50 kHz when sampling at 100 kSps.

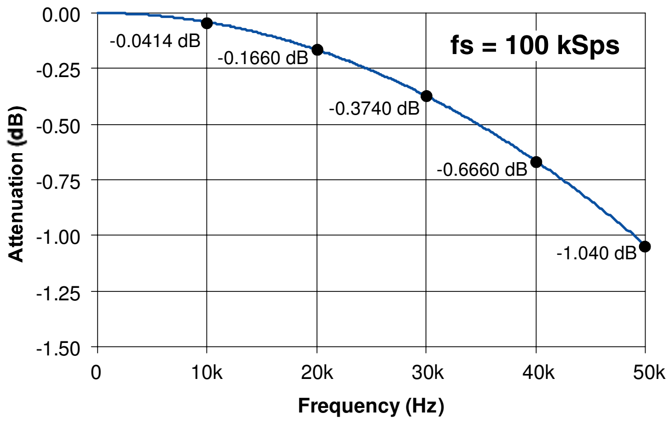


Figure 24. CS5571 Digital Filter Response (DC to fs/2)

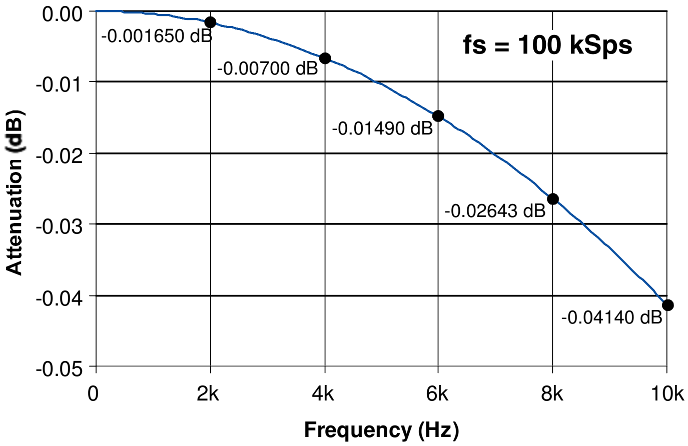


Figure 25. CS5571 Digital Filter Response (DC to 10 kHz)

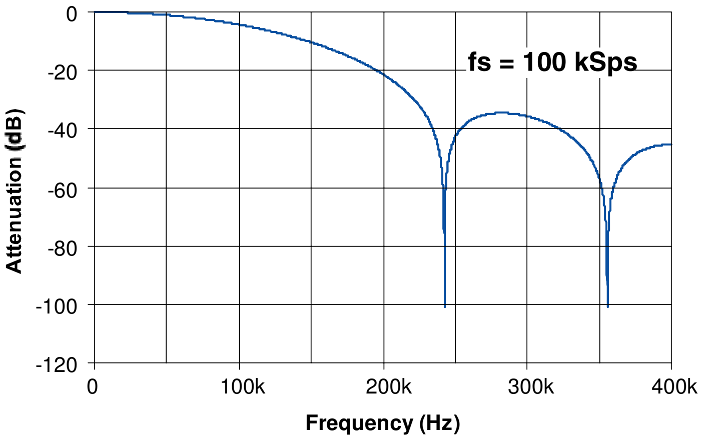


Figure 26. CS5571 Digital Filter Response (DC to 4fs)

3.11 Serial Port

The serial port on the CS5571 can operate in two different modes: synchronous self clock (SSC) mode & synchronous external clock (SEC) mode. The serial port must be placed into the SEC mode if the offset and gain registers of the converter are to be read or written. The converter must be idle when reading or writing to the on-chip registers.

3.11.1 SSC Mode

If the SMODE pin is high (SMODE = VL), the serial port operates in the SSC (Synchronous Self Clock) mode. In the SSC mode the port shifts out conversion data words with SCLK as an output. SCLK is generated inside the converter from MCLK. Data is output from the SDO (Serial Data Output) pin. If $\overline{\text{CS}}$ is high, the SDO and SCLK pins will stay in a high-impedance state. If $\overline{\text{CS}}$ is low when $\overline{\text{RDY}}$ falls, the conversion data word will be output from SDO MSB first. Data is output on the rising edge of SCLK and should be latched into the external logic on the subsequent rising edge of SCLK. When all bits of the conversion word are output from the port the $\overline{\text{RDY}}$ signal will return to high.

3.11.2 SEC Mode

If the SMODE pin is low (SMODE = VLR), the serial port operates in the SEC (Synchronous External Clock mode). In this mode, the user usually monitors $\overline{\text{RDY}}$. When $\overline{\text{RDY}}$ falls at the end of a conversion, the conversion data word is placed into the output data register in the serial port. $\overline{\text{CS}}$ is then activated low to enable data output. Note that $\overline{\text{CS}}$ can be held low continuously if it is not necessary to have the SDO output operate in the high impedance state. When $\overline{\text{CS}}$ is taken low (after $\overline{\text{RDY}}$ falls) the conversion data word is then shifted out of the SDO pin by driving the SCLK pin from system logic external to the converter. Data bits are advanced on rising edges of SCLK and latched by the subsequent rising edge of SCLK.

If $\overline{\text{CS}}$ is held low continuously, the $\overline{\text{RDY}}$ signal will fall at the end of a conversion and the conversion data will be placed into the serial port. If the user starts a read, the user will maintain control over the serial port until the port is empty. However, if SCLK is not toggled, the converter will overwrite the conversion data at the completion of the next conversion. If $\overline{\text{CS}}$ is held low and no read is performed, $\overline{\text{RDY}}$ will rise just prior to the end of the next conversion and then fall to signal that new data has been written into the serial port.

3.12 Power Supplies & Grounding

The CS5571 can be configured to operate with its analog supply operating from 5V, or with its analog supplies operating from ±2.5V. The digital interface supports digital logic operating from either 1.8V, 2.5V, or 3.3V.

Figure 6 on page 17 illustrates the device configured to operate from ±2.5V analog. Figure 7 on page 18 illustrates the device configured to operate from 5V analog.

To maximize converter performance, the analog ground and the logic ground for the converter should be connected at the converter. In the dual analog supply configuration, the analog ground for the ±2.5V supplies should be connected to the VLR pin at the converter with the converter placed entirely over the analog ground plane.

In the single analog supply configuration (+5V), the ground for the +5V supply should be directly tied to the VLR pin of the converter with the converter placed entirely over the analog ground plane. Refer to Figure 7 on page 18.

3.13 Using the CS5571 in Multiplexing Applications

The CS5571 is a delta-sigma A/D converter. Delta-sigma converters use oversampling as means to achieve high signal-to-noise performance. This means that once a conversion is started, the converter takes many samples to compute the resulting output word. The analog input for the signal to be converted must remain active during the entire conversion until $\overline{\text{RDY}}$ falls.

The CS5571 can be used in multiplexing applications, but the system timing for changing the multiplexer channel and for starting a new conversion will depend upon the multiplexer system architecture.

The simplest system is illustrated in Figure 27. Any time the multiplexer is changed, the analog signal presented to the converter must fully settle. After the signal has settled, the $\overline{\text{CONV}}$ signal is issued to the converter to start a conversion. Being a delta-sigma converter, the signal must remain present at the input of the converter until the conversion is completed. Once the conversion is completed, $\overline{\text{RDY}}$ falls. At this time the multiplexer can be changed to the next channel and the data can be read from the serial port. The $\overline{\text{CONV}}$ signal should be delayed until after the data is read and until the new analog signal has settled. In this configuration, the throughput of the converter will be dictated by the settling time of the analog input circuit and the conversion time of the converter. The conversion data can be read from the serial port after the multiplexer is changed to the new channel while the analog input signal is settling.

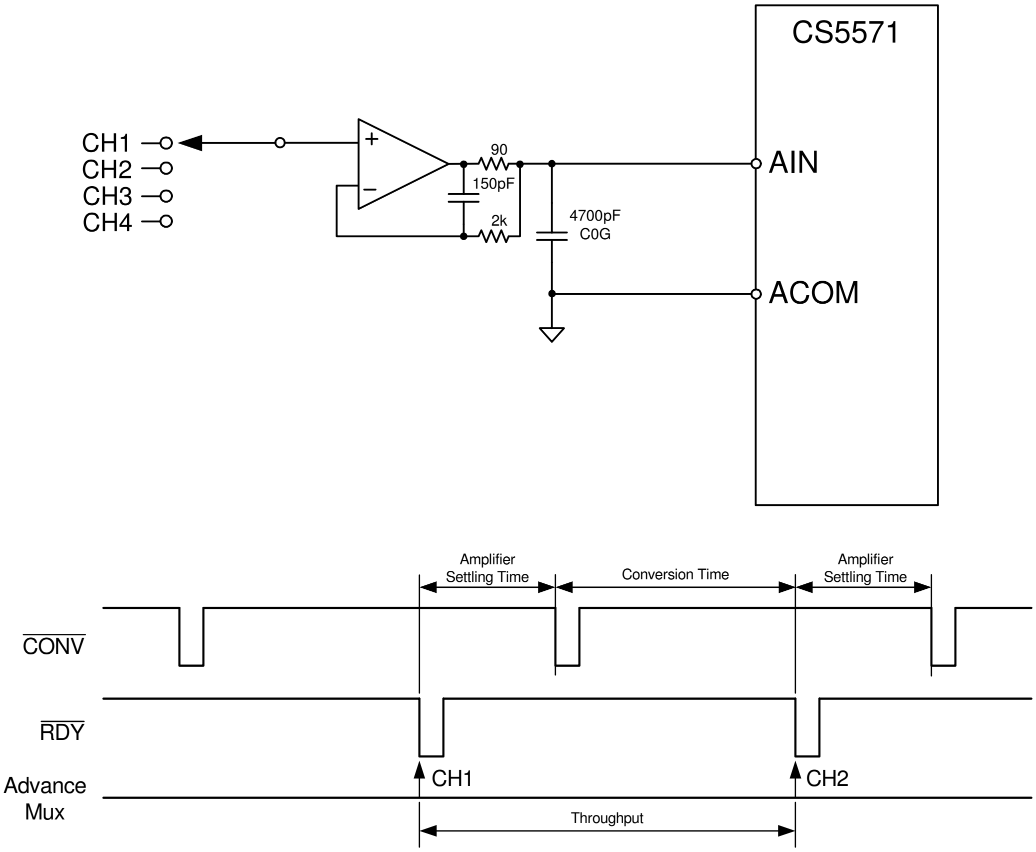


Figure 27. Simple Multiplexing Scheme

A more complex multiplexing scheme can be used to increase the throughput of the converter is illustrated in Figure 28. In this circuit, two banks of multiplexers are used.

At the same time the converter is performing a conversion on a channel from one bank of multiplexers, the second multiplexer bank is used to select the channel for the next conversion. This configuration allows the buffer amplifier for the second multiplexer bank to fully settle while a conversion is being performed on the channel from the first multiplexer bank. The multiplexer on the output of the buffer amplifier and the $\overline{\text{CONV}}$ signal can be changed at the same time in this configuration. This multiplexing architecture allows for maximum multiplexing throughput from the A/D converter. The following figure depicts the recommended analog input amplifier circuit.

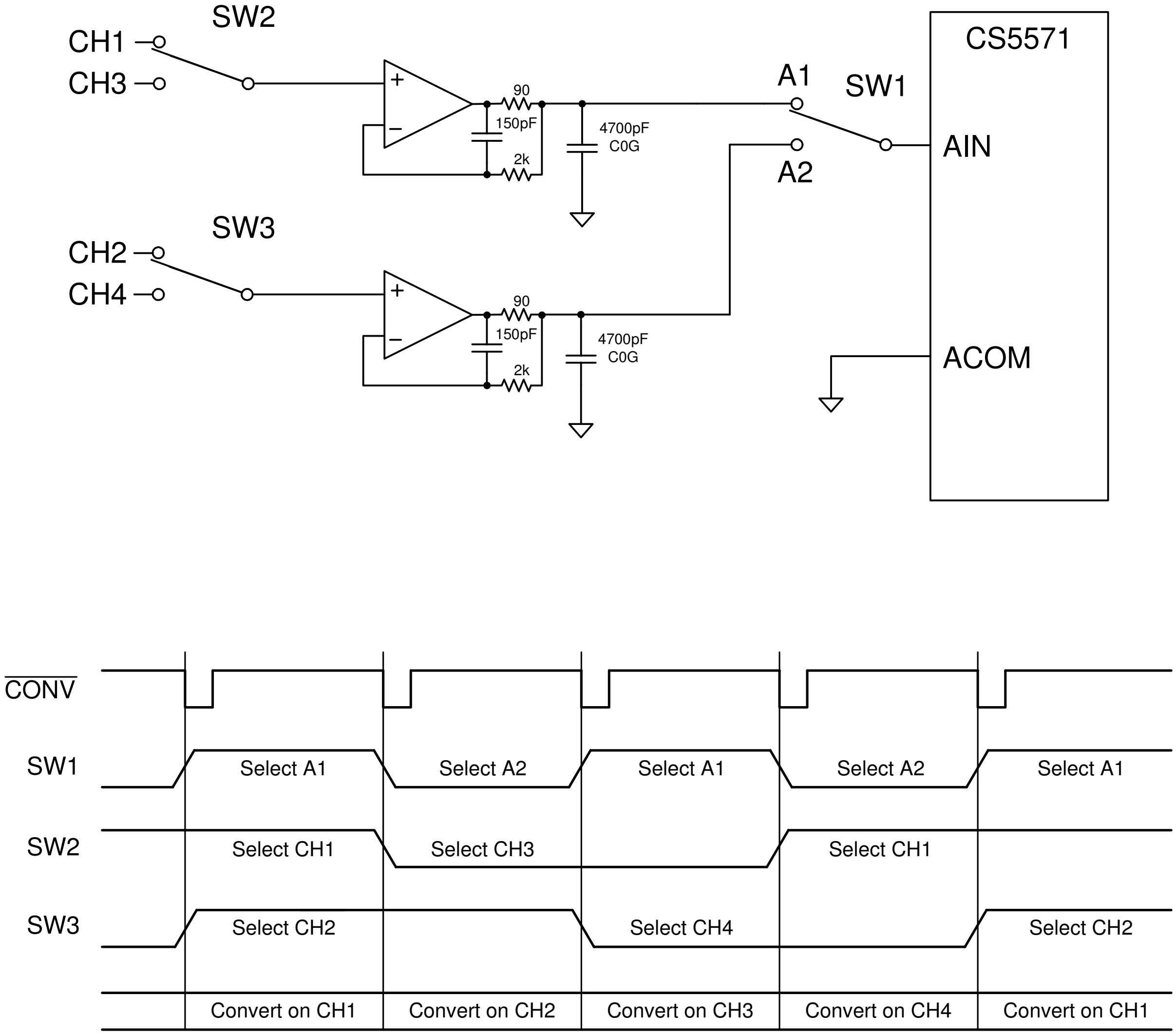
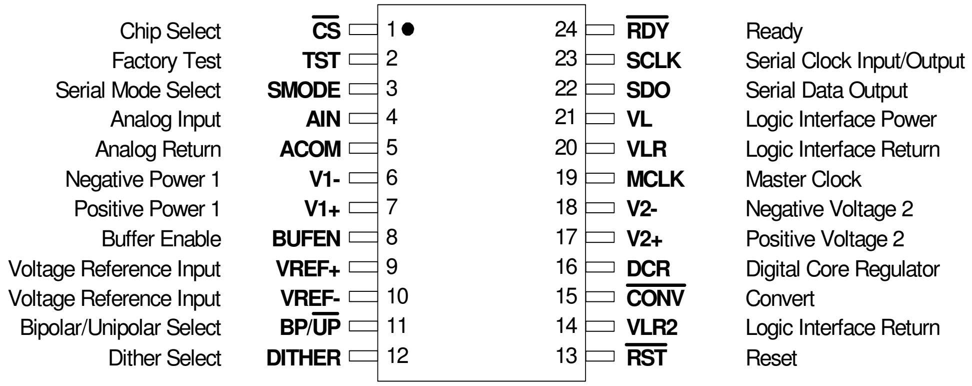

SW2
CH1
CH3
+
−
90
150pF
2k
4700pF
C0G
A1
SW1
A2
CS5571
AIN
ACOM
SW3
CH2
CH4
+
−
90
150pF
2k
4700pF
C0G
CONV
SW1
Select A1
Select A2
Select A1
Select A2
Select A1
SW2
Select CH1
Select CH3
Select CH1
SW3
Select CH2
Select CH4
Select CH2
Convert on CH1
Convert on CH2
Convert on CH3
Convert on CH4
Convert on CH1

Figure 28. More Complex Multiplexing Scheme

3.14 Synchronizing Multiple Converters

Many measurement systems have multiple converters that need to operate synchronously. The converters should all be driven from the same master clock. In this configuration, the converters will convert synchronously if the same $\overline{\text{CONV}}$ signal is used to drive all the converters, and $\overline{\text{CONV}}$ falls on a falling edge of MCLK. If $\overline{\text{CONV}}$ is held low continuously, reset ($\overline{\text{RST}}$) can be used to synchronize multiple converters if $\overline{\text{RST}}$ is released on a falling edge of MCLK.

4. PIN DESCRIPTIONS


Chip Select $\overline{\text{CS}}$ 1
Factory Test TST 2
Serial Mode Select SMODE 3
Analog Input AIN 4
Analog Return ACOM 5
Negative Power 1 V1- 6
Positive Power 1 V1+ 7
Buffer Enable BUFEN 8
Voltage Reference Input VREF+ 9
Voltage Reference Input VREF- 10
Bipolar/Unipolar Select BP/$\overline{\text{UP}}$ 11
Dither Select DITHER 12
24 $\overline{\text{RDY}}$ Ready
23 SCLK Serial Clock Input/Output
22 SDO Serial Data Output
21 VL Logic Interface Power
20 VLR Logic Interface Return
19 MCLK Master Clock
18 V2- Negative Voltage 2
17 V2+ Positive Voltage 2
16 DCR Digital Core Regulator
15 $\overline{\text{CONV}}$ Convert
14 VLR2 Logic Interface Return
13 $\overline{\text{RST}}$ Reset

$\overline{\text{CS}}$ – Chip Select, Pin 1

The Chip Select pin allows an external device to access the serial port. When held high, the SDO output will be held in a high-impedance output state.

TST – Factory Test, Pin 2

For factory use only. Connect to VLR.

SMODE – Serial Mode Select, Pin 3

The serial interface mode pin (SMODE) dictates whether the serial port behaves as a master or slave interface. If SMODE is tied high (to VL), the port will operate in the Synchronous Self-Clocking (SSC) mode. In SSC mode, the port acts as a master in which the converter outputs both the SDO and SCLK signals. If SMODE is tied low (to VLR), the port will operate in the Synchronous External Clocking (SEC) mode. In SEC mode, the port acts as a slave in which the external logic or microcontroller generates the SCLK used to output the conversion data word from the SDO pin.

AIN – Analog Input, Pin 4

AIN is the single-ended input.

ACOM – Analog Return, Pin 5

ACOM is the analog return for the input signal.

V1- – Negative Power 1, Pin 6

The V1- and V2- pins provide a negative supply voltage to the core circuitry of the chip. These two pins should be decoupled as shown in the application block diagrams. V1- and V2- should be supplied from the same source voltage. For single-supply operation, these two voltages are nominally 0 V (Ground). For dual-supply operation, they are nominally -2.5 V.

V1+ – Positive Power 1, Pin 7

The V1+ and V2+ pins provide a positive supply voltage to the core circuitry of the chip. These two pins should be decoupled as shown in the application block diagrams. V1+ and V2+ should be supplied from the same source voltage. For single supply-operation, these two voltages are nominally +5 V. For dual-supply operation, they are nominally +2.5 V.

BUFEN – Buffer Enable, Pin 8

Buffers on input pins AIN and ACOM are enabled if BUFEN is connected to V1+ and disabled if connected to V1-.

VREF+, VREF- – Voltage Reference Input, Pins 9, 10

A differential voltage reference input on these pins functions as the voltage reference for the converter. The voltage between these pins can range between 2.4 volts and 4.2 volts, with 4.096 volts being the nominal reference voltage value.

BP/$\overline{\text{UP}}$ – Bipolar/Unipolar Select, Pin 11

The BP/$\overline{\text{UP}}$ pin determines the span and the output coding of the converter. When set high to select BP (bipolar), the input span of the converter is -2.048 volts to +2.048 volts (assuming the voltage reference is 4.096 volts) and output data is coded in two's complement format. When set low to select $\overline{\text{UP}}$ (unipolar), the input span is 0 to +2.048 and the output data is coded in binary format.

DITHER – Dither Select, Pin 12

When DITHER is high (DITHER = VL), output conversion words will be dithered. When DITHER is low (DITHER = VLR), output words will be dominated by quantization.

$\overline{\text{RST}}$ – Reset, Pin 13

Reset is necessary after power is initially applied to the converter. When the $\overline{\text{RST}}$ input is taken low, the logic in the converter will be reset. When $\overline{\text{RST}}$ is released to go high, certain portions of the analog circuitry are started. $\overline{\text{RDY}}$ falls when reset is complete.

$\overline{\text{CONV}}$ – Convert, Pin 15

The $\overline{\text{CONV}}$ pin initiates a conversion cycle if taken low, a previous conversion is in progress. When the conversion cycle is completed, the conversion word is output to the serial port register and the $\overline{\text{RDY}}$ signal goes low. If $\overline{\text{CONV}}$ is held low and remains low when $\overline{\text{RDY}}$ falls, another conversion cycle will be started.

DCR – Digital Core Regulator, Pin 16

DCR is the output of the on-chip regulator for the digital logic core. DCR should be bypassed with a capacitor to V2-. The DCR pin is not designed to power any external load.

V2+ – Positive Power 2, Pin 17

The V1+ and V2+ pins provide a positive supply voltage to the circuitry of the chip. These two pins should be decoupled as shown in the application block diagrams. V1+ and V2+ should be supplied from the same source voltage. For single-supply operation, these two voltages are nominally +5 V. For dual-supply operation, they are nominally +2.5 V.

V2- – Negative Power 2, Pin 18

The V1- and V2- pins provide a negative supply voltage to the circuitry of the chip. These two pins should be decoupled as shown in the application block diagrams. V1- and V2- should be supplied from the same source voltage. For single-supply operation, these two voltages are nominally 0 V (Ground). For dual-supply operation, they are nominally -2.5 V.

MCLK – Master Clock, Pin 19

The master clock pin (MCLK) is a multi-function pin. If tied low (MCLK = VLR), the on-chip oscillator will be enabled. If tied high (MCLK = VL), all clocks to the internal circuitry of the converter will stop. When MCLK is held high the internal oscillator will also be stopped. MCLK can also function as the input for an external CMOS-compatible clock that conforms to supply voltages on the VL and VLR pins.

VLR2, VLR, VL – Logic Interface Power/Return, Pins 14, 20, 21

VL and VLR are the supply voltages for the digital logic interface. VL and VLR can be configured with a wide range of common mode voltage. The following interface pins function from the VL/VLR supply: SMODE, $\overline{\text{CS}}$, SCLK, TST, SDO, $\overline{\text{RDY}}$, DITHER, $\overline{\text{CONV}}$, $\overline{\text{RST}}$, BP/$\overline{\text{UP}}$, and MCLK.

SDO – Serial Data Output, Pin 22

SDO is the output pin for the serial output port. Data from this pin will be output at a rate determined by SCLK and in a format determined by the BP/$\overline{\text{UP}}$ pin. Data is output MSB first and advances to the next data bit on the rising edges of SCLK. SDO will be in a high impedance state when $\overline{\text{CS}}$ is high.

SCLK – Serial Clock Input/Output, Pin 23

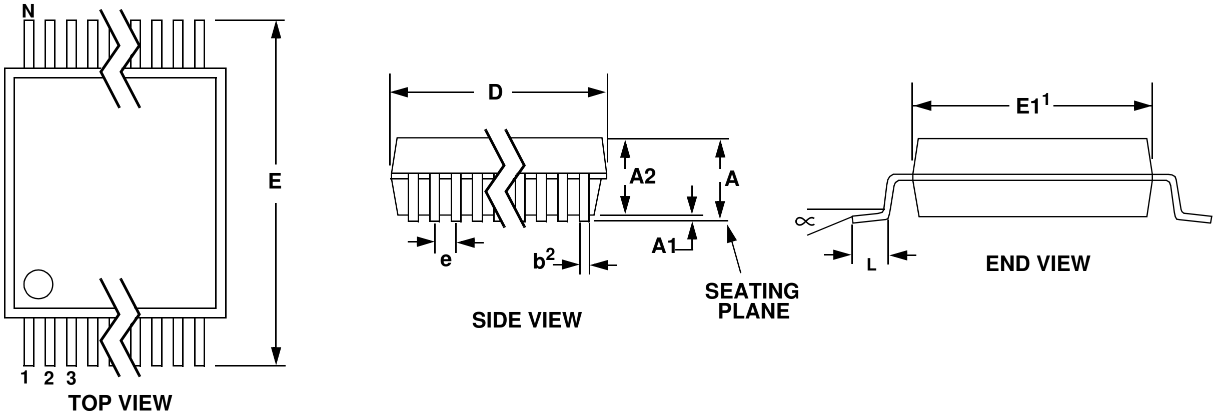
The SMODE pin determines whether the SCLK signal is an input or an output signal. SCLK determines the rate at which data is clocked out of the SDO pin. If the converter is in SSC mode, the SCLK frequency will be determined by the master clock frequency of the converter (either MCLK or the internal oscillator). In SEC mode, the user determines the SCLK frequency. If SCLK is an output (SMODE = VL), it will be in a high-impedance state when CS is high.

RDY – Ready, Pin 24

If CONV is low the converter will immediately start a conversion and RDY will remain high until the conversion is completed. At the end of any conversion RDY falls to indicate that a conversion word has been placed into the serial port. RDY will return high after all data bits are shifted out of the serial port or two master clock cycles before new data becomes available if the CS pin is inactive (high); or two master clock cycles before new data becomes available if the user holds CS low but has not started reading the data from the converter when in SEC mode.

5. PACKAGE DIMENSIONS

24L SSOP PACKAGE DRAWING



	INCHES			MILLIMETERS			NOTE
DIM	MIN	NOM	MAX	MIN	NOM	MAX	
A	--	--	0.084	--	--	2.13	
A1	0.002	0.006	0.010	0.05	0.13	0.25	
A2	0.064	0.068	0.074	1.62	1.73	1.88	
b	0.009	--	0.015	0.22	--	0.38	2,3
D	0.311	0.323	0.335	7.90	8.20	8.50	1
E	0.291	0.307	0.323	7.40	7.80	8.20	
E1	0.197	0.209	0.220	5.00	5.30	5.60	1
e	0.022	0.026	0.030	0.55	0.65	0.75	
L	0.025	0.03	0.041	0.63	0.75	1.03	
∝	0°	4°	8°	0°	4°	8°	

JEDEC #: MO-150

Controlling Dimension is Millimeters.

Notes:

1. "D" and "E1" are reference datums and do not included mold flash or protrusions, but do include mold mismatch and are measured at the parting line, mold flash or protrusions shall not exceed 0.20 mm per side.
2. Dimension "b" does not include dambar protrusion/intrusion. Allowable dambar protrusion shall be 0.13 mm total in excess of "b" dimension at maximum material condition. Dambar intrusion shall not reduce dimension "b" by more than 0.07 mm at least material condition.
3. These dimensions apply to the flat section of the lead between 0.10 and 0.25 mm from lead tips.

6. ORDERING INFORMATION

Model	Linearity	Temperature	Conversion Time	Throughput	Package
CS5571-ISZ	.0008%	-40 to +85 °C	10 µs	100 kSps	24-pin SSOP

7. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5571-ISZ	260 °C	3	7 Days

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

8. REVISION HISTORY

Revision	Date	Changes
PP1	MAR 2008	Preliminary release.

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.
To find the one nearest to you go to www.cirrus.com

IMPORTANT NOTICE

"Preliminary" product information describes products that are in production, but for which full characterization data is not yet available.

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