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## *Hall Effect Direction Detection Sensor IC*

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### **Last Time Buy**

These parts are in production but have been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: May 4, 2009

Deadline for receipt of LAST TIME BUY orders: November 4, 2009

#### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, refer to the [A3423](#).*

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NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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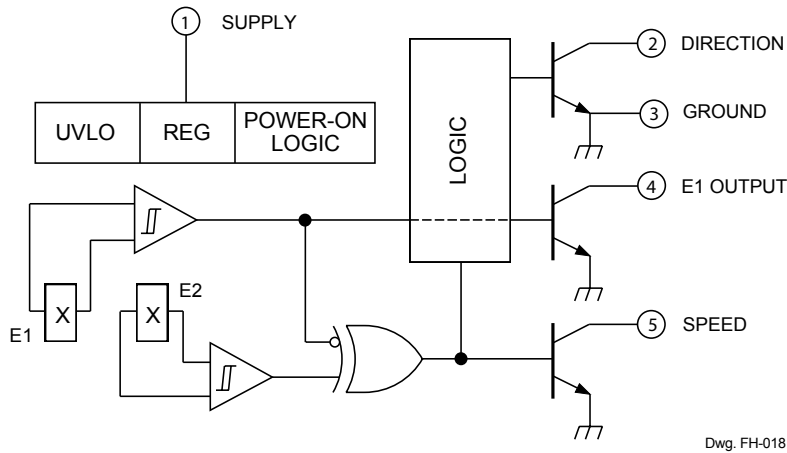
# 3422 HALL-EFFECT, DIRECTION-DETECTION SENSOR IC

## Selection Guide

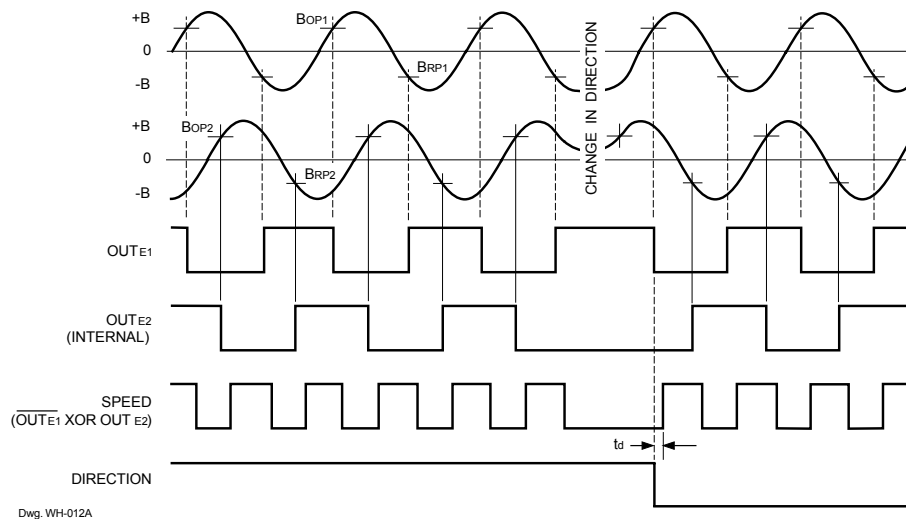
Part Number	Packing*	Mounting	Ambient, T <sub>A</sub> (°C)
A3422EKA-T	Bulk, 500 pieces/bag	5-pin SIP through hole	-40 to 85
A3422LKA-T	Bulk, 500 pieces/bag	5-pin SIP through hole	-40 to 150

\*Contact Allegro for additional packing options.

## FUNCTIONAL BLOCK DIAGRAM



## TIMING DIAGRAM

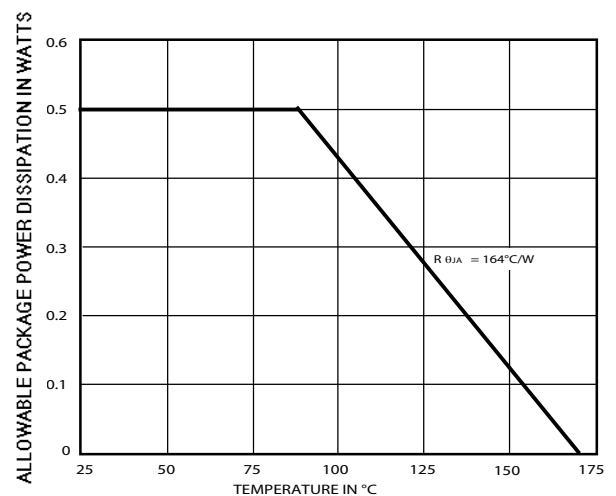


# 3422 HALL-EFFECT, DIRECTION-DETECTION SENSOR IC

## ELECTRICAL CHARACTERISTICS over operating temperature range.

Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Supply Voltage Range	$V_{CC}$	Operating, $T_J < 165^\circ\text{C}^1$	4.5	—	18	V
Output Leakage Current	$I_{OFF}$	$V_{OUT} = V_{CC} = 18\text{ V}$	—	<1.0	10	$\mu\text{A}$
Output Saturation Voltage	$V_{OUT(SAT)}$	$I_{OUT} = 20\text{ mA}$	—	0.21	0.50	V
Power-On State	POS	$V_{CC} = 0 \rightarrow 5\text{ V}$ , $B_{RP1} < B < B_{OP1}$ , $B_{RP2} < B < B_{OP2}$	OFF	OFF	OFF	—
Undervoltage Lockout	$V_{CC(UV)}$	$I_{OUT} = 20\text{ mA}$ , $V_{CC} = 0 \rightarrow 5\text{ V}$	—	3.5	—	V
Undervoltage Hysteresis	$V_{CC(hys)}$	Lockout ( $V_{CC(UV)}$ ) - Shutdown	—	0.5	—	V
Power-On Time	$t_{po}$	$V_{CC} > 4.5\text{ V}$	—	—	50	$\mu\text{s}$
Output Rise Time	$t_r$	$C_L = 20\text{ pF}$ , $R_L = 820$	—	200	—	ns
Output Fall Time	$t_f$	$C_L = 20\text{ pF}$ , $R_L = 820$	—	200	—	ns
Direction Change Delay	$t_d$	$C_L = 20\text{ pF}$ , $R_L = 820$	0.5	1.0	5.0	$\mu\text{s}$
Supply Current	$I_{CC}$	$V_{CC} = 8\text{ V}$ , All outputs OFF	5.0	9.0	18	mA

- NOTES: 1. Maximum supply voltage must be adjusted for power dissipation and ambient temperature.  
2. Typical Data is at  $V_{CC} = 12\text{ V}$  and  $T_A = +25^\circ\text{C}$  and is for design information only.



Dwg. GH-069

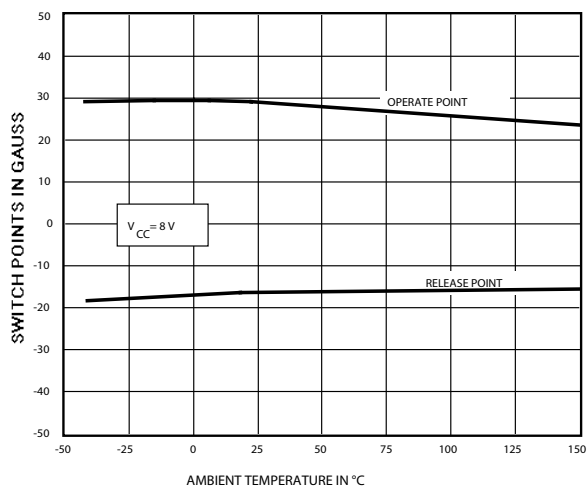
# 3422 HALL-EFFECT, DIRECTION-DETECTION SENSOR IC

## MAGNETIC CHARACTERISTICS over operating voltage range.

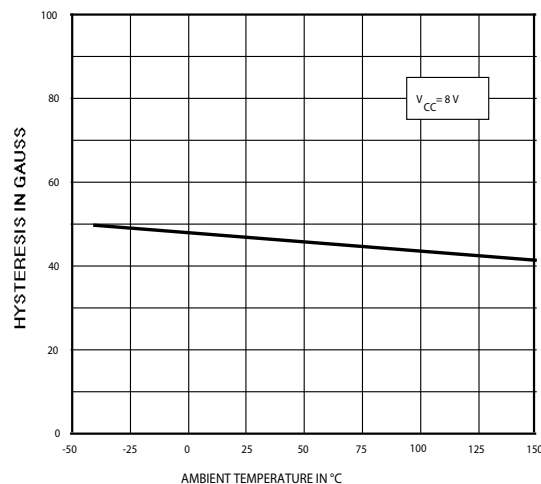
Characteristic	Symbol	Test Conditions	Limits			
			Min.	Typ.	Max.	Units
Operate Point	B <sub>OP</sub>	T <sub>A</sub> = -40°C	—	—	85	G
		T <sub>A</sub> = +25°C	—	29	75	G
		T <sub>A</sub> = Maximum	—	—	75	G
Release Point <sup>3</sup>	B <sub>RP</sub>	T <sub>A</sub> = -40°C	-85	—	—	G
		T <sub>A</sub> = +25°C	-75	-17	—	G
		T <sub>A</sub> = Maximum	-75	—	—	G
Hysteresis	B <sub>hys</sub>	T <sub>A</sub> = -40°C	10	—	—	G
		T <sub>A</sub> = +25°C	10	46	—	G
		T <sub>A</sub> = Maximum	10	—	—	G
Operate Differential	—	B <sub>OP1</sub> - B <sub>OP2</sub>	—	—	±60	G
Release Differential	—	B <sub>RP1</sub> - B <sub>RP2</sub>	—	—	±60	G

- NOTES: 1. Magnetic flux density is measured at most sensitive area of device, nominally located 0.0165" (0.42 mm) below the branded face of the package.  
 2. Typical Data is at V<sub>CC</sub> = 12 V and T<sub>A</sub> = +25°C and is for design information only.  
 3. As used here, negative flux densities are defined as less than zero (algebraic convention).

## Typical Magnetic Characteristics

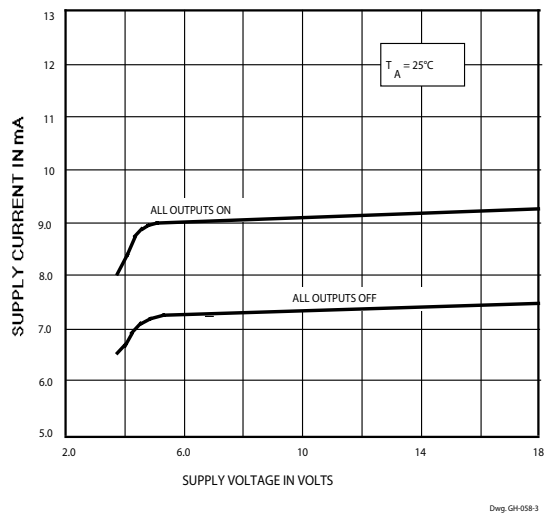
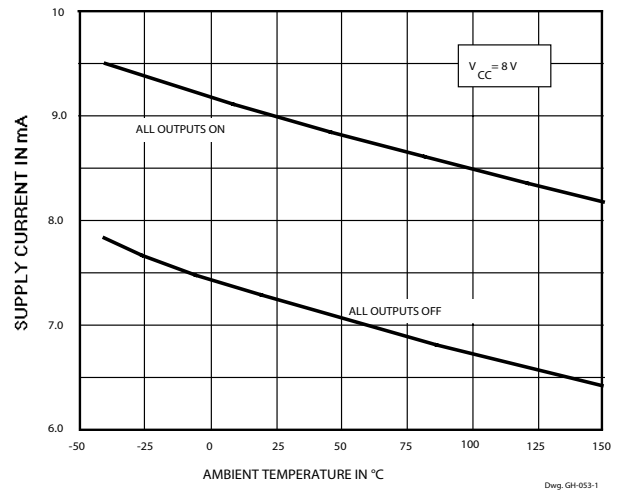
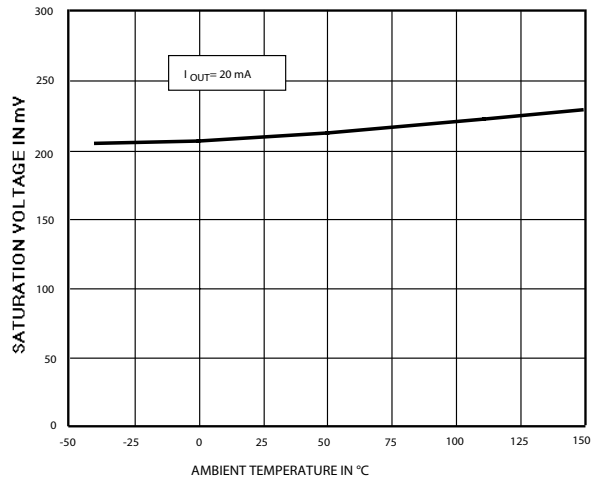


Dwg. GH-026-1



Dwg. GH-051-1

Typical Electrical Characteristics



# 3422 HALL-EFFECT, DIRECTION-DETECTION SENSOR IC

## Functional Description

The integrated circuit contains an internal voltage regulator that powers the Hall elements and both the analog and digital circuitry. This regulator allows operation over a wide supply voltage range and provides some immunity to supply noise. The device also contains CMOS logic circuitry that decodes the direction of rotation of the ring magnet.

**Quadrature/Direction Detection.** Internal logic circuitry provides outputs representing speed and direction of the magnetic field across the face of the package. For the direction signal to be appropriately updated, a quadrature relationship must be maintained between the ring magnet pole width\*, the element-to-element spacing, and, to a lesser extent, the magnetic switch points. For optimal design, the device should be actuated with a ring magnet pole width\* two times the sensor-to-sensor spacing. This will produce a sinusoidal magnetic field whose period (denoted as  $T$ ) is then four times the element-to-element spacing. A quadrature relationship can also be maintained for a ring magnet that has a period that satisfies the relationship  $nT/4 = 1.5 \text{ mm}$ , where  $n$  is any odd integer. Therefore, ring magnets with pole-pair spacings equal to 6 mm ( $n = 1$ ), 2 mm ( $n = 3$ ), 1.2 mm ( $n = 5$ ), etc. are permitted.

The response of the device to the magnetic field produced by a rotating ring magnet is shown on page 2. Note the phase shift between the two elements.

\*“Pole” refers to a single pole (North or South) unless stated as “pole pair” (North and South).

**Outputs.** The device provides three saturated outputs: DIRECTION, E1 OUTPUT, and SPEED. DIRECTION provides the direction output of the device and is defined as OFF (high) for the direction E1 to E2 and ON (low) for the direction E2 to E1. SPEED provides an XOR'd output of the two elements. Because of internal delays, DIRECTION will always be updated before SPEED and is updated at every transition of E1 OUTPUT and E2 OUTPUT (internal) allowing the use of up-down counters without the loss of pulses.

**Power-On State.** At power on, the logic circuitry is reset to provide an OFF (high) at DIRECTION and an OFF (high) for E1 and E2 (internal) for magnetic fields less than  $B_{OP}$ . This eliminates ambiguity when the device is powered up and either element detects a field between  $B_P$  and  $B_{RP}$ . If either element is subjected to a field greater than  $B_{OP}$ , the internal logic will set accordingly.

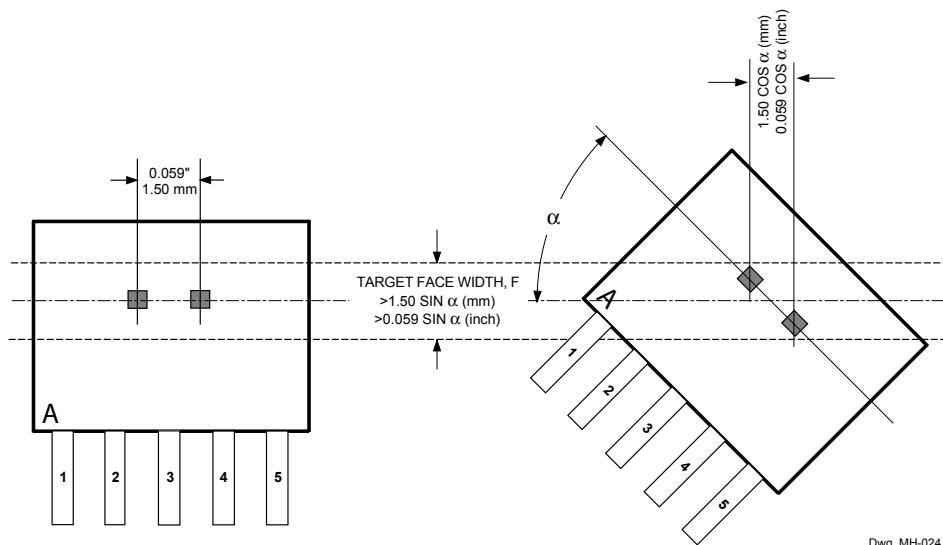
## Applications Information

**Operation with Fine-Pitch Ring Magnets.** For targets with a circular pitch of less than 4mm, a performance improvement can be observed by rotating the front face of the device (see below). This device rotation decreases the effective element-to-element spacing, provided that the Hall elements are not rotated beyond the width of the target.

**Applications.** It is strongly recommended that an external 0.01  $\mu$ F bypass capacitor be connected (in close proximity to the Hall elements) between the supply and ground of the device to reduce both external noise and noise generated by the internal logic.

The simplest form of magnet that will operate these devices is a ring magnet. Other methods of operation, such as linear magnets, are possible. Extensive applications information on magnets and Hall-effect devices is also available in the “Hall-Effect IC Applications Guide” which can be found in the latest issue of the *Allegro MicroSystems Electronic Data Book*, AMS-702 or *Application Note 27701*, or at

[www.allegromicro.com](http://www.allegromicro.com)



**Rotated device for  
fine-pitch ring  
magnets**

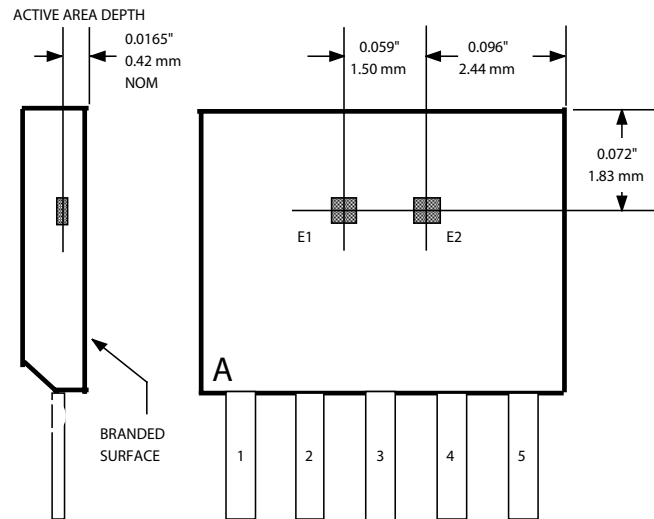


**3422**  
**HALL-EFFECT,**  
**DIRECTION-DETECTION**  
**SENSOR**

**Criteria for Device Qualification**

Contact Allegro MicroSystems for qualification information.

**Element Locations**

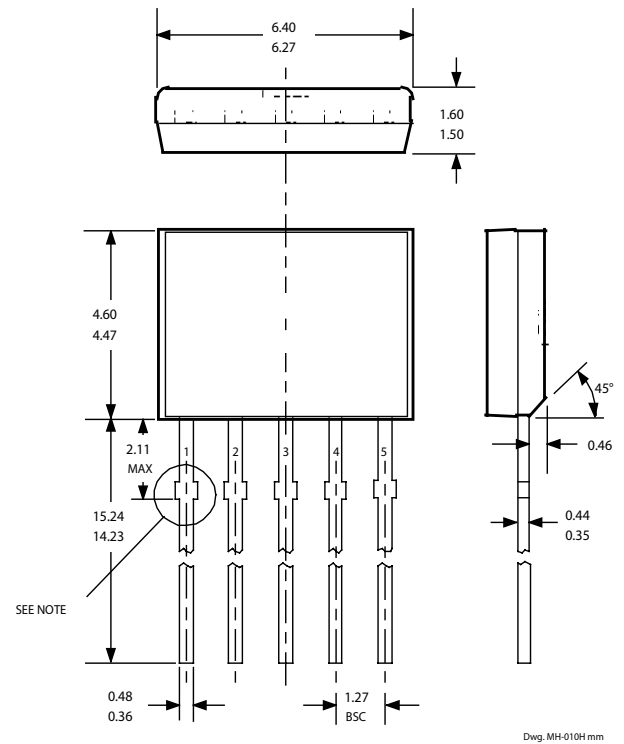
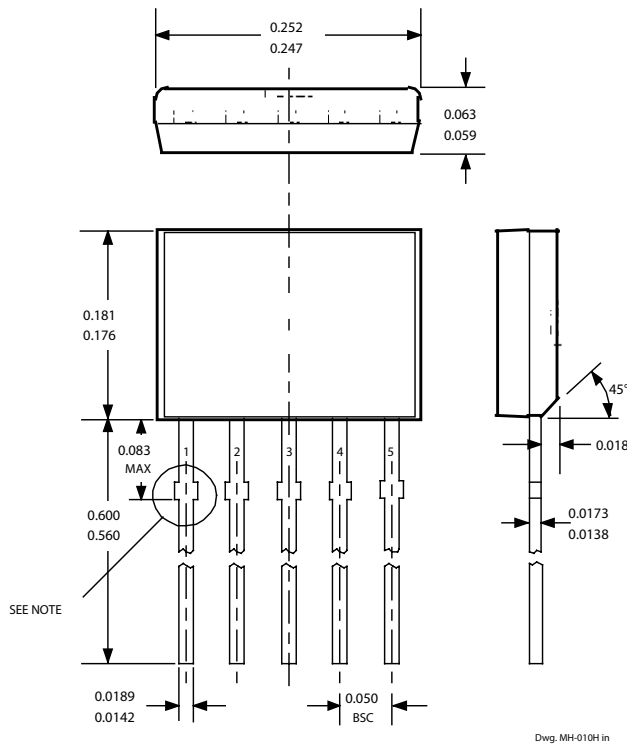


Dwg. MH-007-1A

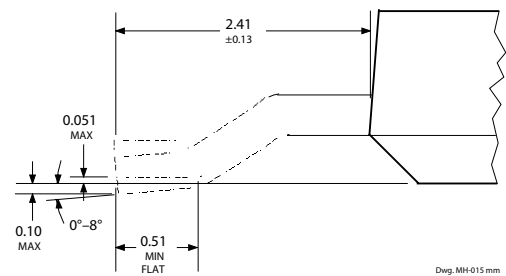
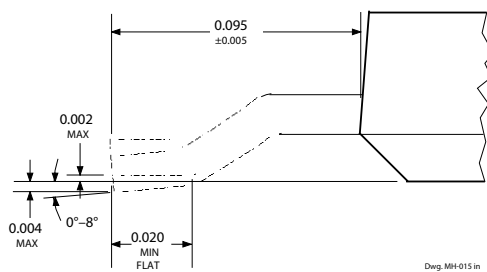
Package Designator 'KA'

Dimensions in Inches  
(controlling dimensions)

Dimensions in Millimeters  
(for reference only)



Surface-Mount Lead Form (add '-TL' to part number)



- NOTES:
1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
  2. Exact body and lead configuration at vendor's option within limits shown.
  3. Height does not include mold gate flash.
  4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
  5. Where no tolerance is specified, dimension is nominal.
  6. Supplied in bulk pack (500 pieces per bag).

**3422**  
**HALL-EFFECT,**  
**DIRECTION-DETECTION**  
**SENSOR IC**

The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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