Xenon Photoflash Capacitor Charger with IGBT Driver

Discontinued Product

This device is no longer in production. The device should not be purchased for new design applications. Samples are no longer available.

Date of status change: December 10, 2012

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

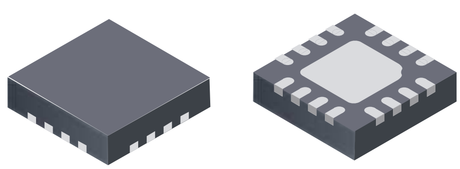
A8427

Xenon Photoflash Capacitor Charger with IGBT Driver

Features and Benefits

- Low quiescent current (0.1 µA in shutdown mode)
- Primary-side output voltage sensing; no resistor divider required
- User-adjustable current limit from 0.8 to 2.4 A
- 1.3 V logic (V_{HI}(min)) compatibility
- Integrated IGBT driver with separate sink and source
- Flash trigger with interlock for increased noise immunity
- Optimized for 1-cell Lithium-ion or 2 to 3 Alkaline/NiMH batteries
- No primary-side Schottky diode needed
- Zero-voltage switching for lower loss
- >70% efficiency
- Optional regulation feature to maintain the output voltage
- Charge complete indication
- Integrated 40 V DMOS switch in very thin profile 3 mm ×3 mm, 0.75 mm nominal height package

Package: 16-contact TQFN (suffix ES)



Approximate Scale 1:1

Description

The Allegro A8427 xenon photoflash capacitor charger IC is designed for camera phones and digital cameras. To extend battery life, it features very low supply current drain, typically 0.1 µA in shutdown mode, and 10 µA in standby mode.

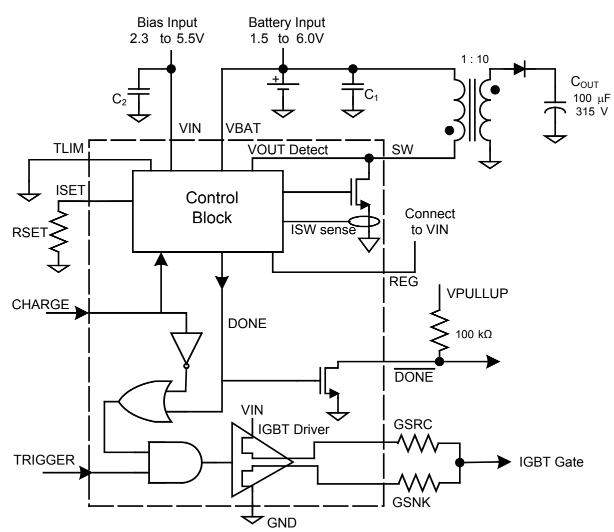
The charge time is adjustable by setting the peak current limit from 0.8 to 2.4 A. By using primary-side voltage sensing, the need for a secondary-side resistive divider is eliminated. This leads to benefits of reducing power loss, lower system cost, and smaller board space.

The A8427 has an integrated IGBT driver and flash trigger interlock to increase the system noise immunity. The IGBT driver also has separate source and sink connections, for flexibility in controlling rise and fall time. The charge and trigger input logic thresholds are set at 1.3 V_{HI} (min) to support low-voltage control logic.

The A8427 is available in 16-contact 3 mm × 3 mm TQFN package with exposed pad for enhanced thermal performance. This small, very thin profile (0.75 mm nominal overall height) package is ideal for space-constrained applications.

Applications include:
- Digital camera flash
- Film and digital SLR camera flash

Typical Application



Application 1. Typical application without output voltage regulation (REG pin connected to VIN). System needs to periodically restart the charging cycle to replenish lost charge on the output capacitor.

Selection Guide

Part Number	Packing*
A8427EESTR-T	Tape and reel, 1500 pieces/reel

*Contact Allegro for additional packing options.

Absolute Maximum Ratings*

Characteristic	Symbol	Notes	Rating	Units
SW Pin	V_{SW}	DC voltage. (V_{SW} is self-clamped by an internal active clamp and is allowed to exceed 40 V during flyback spike durations. Maximum repetitive energy during flyback spike: 0.5 µJ at frequency ≤ 400 kHz.)	–0.3 to 40	V
VBAT Pin	V_{BAT}		–0.3 to 7.0	V
VIN Pin	V_{IN}		–0.3 to 6.0	V
CHARGE, TRIGGER, $\overline{\text{DONE}}$ Pins		Care must be taken to limit the current when –0.6 V is applied to these pins	–0.6 to V_{IN} + 0.3 V	V
Remaining Pins			–0.3 to V_{IN} + 0.3 V	V
Operating Ambient Temperature	T_A	Range E	–40 to 85	ºC
Maximum Junction	T_J(max)		150	ºC
Storage Temperature	T_{stg}		–55 to 150	ºC

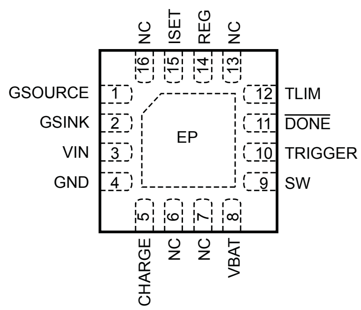
*With respect to GND.

Thermal Characteristics

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	On 4-layer PCB, based on JEDEC specification	47	ºC/W

*Additional thermal information available on Allegro website.

Pin-out Diagram

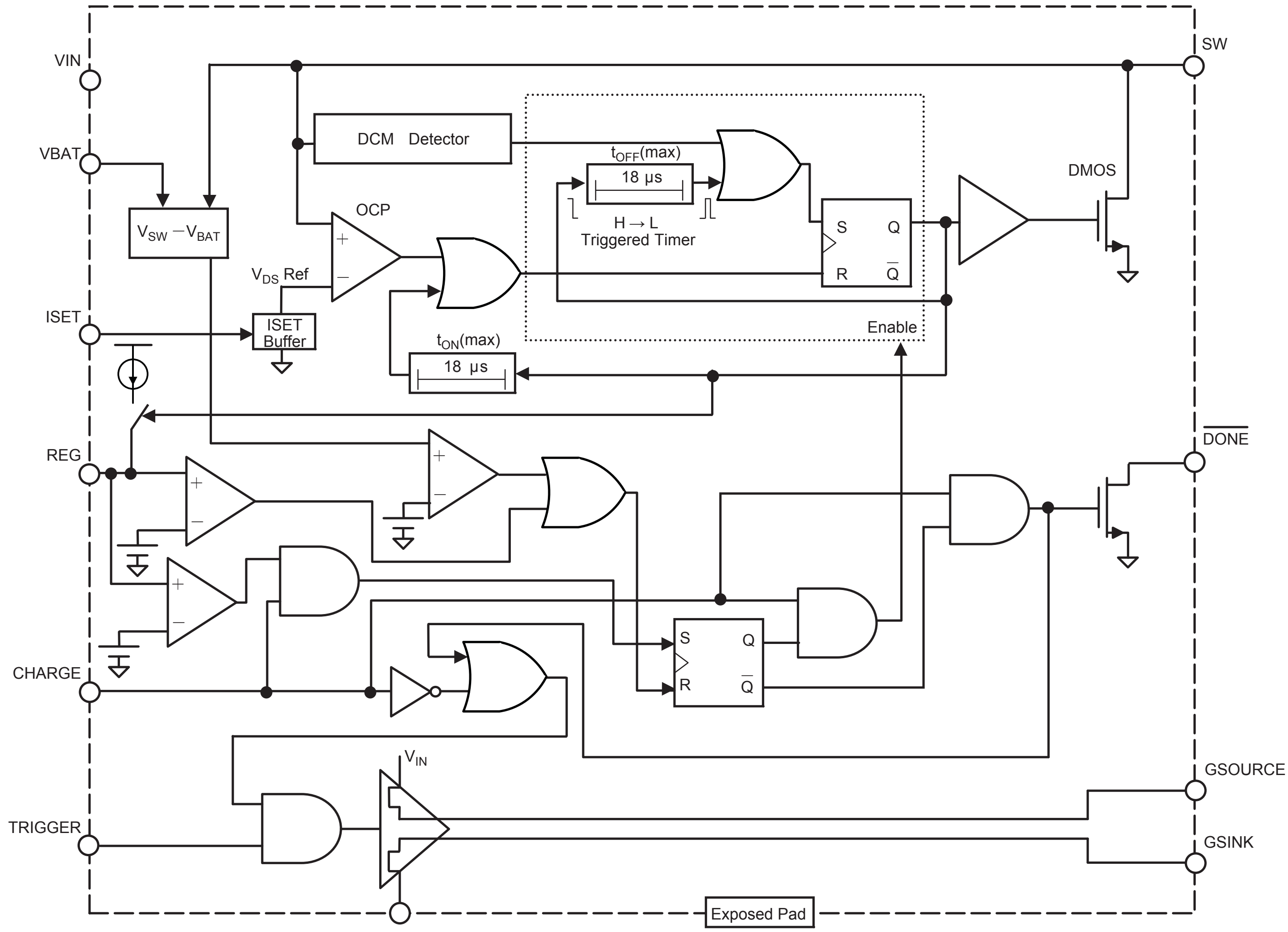


(Top View)

Terminal List Table

Number	Name	Function
1	GSOURCE	IGBT gate drive – source connection
2	GSINK	IGBT gate drive – sink connection
3	VIN	Input voltage; connect to a 2.3 to 5.5 V voltage source
4	GND	Ground connection
5	CHARGE	Pull high to initiate charging; pull low to enter low-power standby mode
6, 7, 13, 16	NC	No connection
8	VBAT	Battery voltage; connect to the main power supply for primary-side sensing
9	SW	Drain connection of internal power MOSFET switch; connect to transformer
10	TRIGGER	IGBT input trigger; triggering is enabled when CHARGE pin is low, or when CHARGE is high and $\overline{\text{DONE}}$ is low. This feature improves system noise immunity
11	$\overline{\text{DONE}}$	Pulls low when output reaches target value and CHARGE pin is high; remains low until CHARGE pin is cycled
12	TLIM	For Allegro use only; connect to GND on PCB
14	REG	Output voltage regulation pin; connect to external resistor and capacitor to regulate output voltage, or connect to VIN to disable regulation. See the Output Regulation section for details.
15	ISET	Sets the maximum switch current; connect an external resistor to GND to set the target peak current; see Circuit Description section for details
–	EP	Exposed pad for enhanced thermal dissipation (not connected electrically)

Functional Block Diagram



ELECTRICAL CHARACTERISTICS typical values valid at V_{IN}= V_{BAT}=3.6 V, R_{SET}= 36 kΩ, I_{SWlim} = 2.4 A, and T_A=25°C, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
VBAT Pin Voltage Range	V_{BAT}		1.5	–	6.0	V
VIN Pin Voltage Range[1]	V_{IN}		2.3	–	5.5	V
UVLO Enable Threshold	V_{INUV}	V_{IN} rising	–	2.05	2..2	V
UVLO Hysteresis	$V_{INUVhys}$		–	150	–	mV
Switch Current Limit[2]	$I_{SWlimMAX}$	Maximum, I_{SET} = 32.4 μA	2.16	2.4	2.64	A
	$I_{SWlimMIN}$	Minimum, I_{SET} = 10.8 μA	–	0.8	–	A
SW Current Limit to ISET Current Ratio	I_{SWlim}/I_{SET}	I_{SET} = 32.4 μA, CHARGE = high	–	74	–	kA/A
ISET Pin Voltage While Charging	V_{SET}	I_{SET} = 32.4 μA, CHARGE = high, I_{SW} = 0 A (VBAT disconnected)	–	1.167	–	V
		I_{SET} = 32.4 μA, CHARGE = high, I_{SW} = 2.4 A	–	1.232	–	V
ISET Pin Internal Resistance	$R_{SET(INT)}$		–	1000	–	Ω
GND Pin Internal Resistance	$R_{GND(INT)}$		–	27	–	mΩ
Switch On-Resistance	$R_{SWDS(on)}$	V_{IN} = 3.6 V, I_D = 800 mA, T_A = 25°C	–	0.25	–	Ω
Switch Leakage Current[1]	I_{SWlk}	V_{SW} = V_{BAT}(MAX)	–	–	2	μA
VIN Pin Supply Current	I_{IN}	Shutdown (CHARGE = 0 V, TRIGGER = 0 V)	–	0.01	1	μA
		Charging done, regulation disabled (REG = VIN)	–	10	50	μA
		Charging done, regulation enabled	–	0.5	–	mA
		Charging (CHARGE = VIN, TRIGGER = 0 V)	–	2	–	mA
VBAT Pin Supply Current	I_{BAT}	Shutdown (CHARGE = 0 V, TRIGGER = 0 V)	–	0.01	1	μA
		Charging done, regulation disabled (REG = VIN)	–	–	1	μA
		Charging done, regulation enabled	–	–	50	uA
		Charging (CHARGE = VIN, TRIGGER = 0 V)	–	–	125	uA
CHARGE Pin Input Current	I_{CHARGE}	V_{CHARGE} = V_{IN}	–	36	–	μA
CHARGE Pin Input Voltage High[1]	$I_{CHARGE(H)}$	Over input supply range, V_{IN}	1.3	–	–	V
CHARGE Pin Input Voltage Low[1]	$I_{CHARGE(L)}$	Over input supply range, V_{IN}	–	–	0.4	V
CHARGE Pin Pull-down Resistor	R_{CHARGE}		–	100	–	kΩ
Maximum Switch-off Timeout	t_{offMAX}		–	18	–	μs
Maximum Switch-on Timeout	t_{onMAX}		–	18	–	μs
$\overline{\text{DONE}}$ Pin Output Leakage Current[1]	I_{DONElk}		–	–	1	μA
$\overline{\text{DONE}}$ Pin Output Low Voltage[1]	V_{DONEL}	32 μA into $\overline{\text{DONE}}$ pin	–	–	100	mV
Output Comparator Trip Voltage[1]	$V_{OUTTRIP}$	Measured as $V_{SW} - V_{BAT}$	31	31.5	32	V
Output Comparator Overdrive	V_{OUTOV}	200 ns pulse width (90% to 90%)	–	200	400	mV
Minimum dV/dt for ZVS Comparator	dV/dt	Measured at SW pin	–	20	–	V/μs

Continued on the next page …

ELECTRICAL CHARACTERISTICS (continued) typical values valid at $V_{IN} = V_{BAT} = 3.6$ V, $R_{SET} = 36$ kΩ, $I_{SWlim} = 2.4$ A, and $T_A = 25°C$, unless otherwise noted

Characteristics	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Regulation						
REG Voltage When Charging Completes	$V_{REG(H)}$	CHARGE = high, at $\overline{DONE}$ → low transition	1.15	1.2	1.25	V
REG Voltage Threshold for Regulation	$V_{REG(L)}$	CHARGE = high, $\overline{DONE}$ = low	–	0.96	–	V
REG Output Current Drive Capability	I_{REG}	CHARGE = high, $\overline{DONE}$ = high, $V_{SW} - V_{IN} = 30$ V, $V_{REG} = 1.0$ V	–	50	–	μA
REG Leakage Current While Not Charging	I_{REGlk}	CHARGE = high, $\overline{DONE}$ = low, $V_{REG} = 1.2$ V	–	0.2	–	μA
IGBT Driver						
TRIGGER Pin High Input Voltage[1]	$V_{TRIG(H)}$	Over input supply range, V_{IN}	1.3	–	–	V
TRIGGER Pin Low Input Voltage[1]	$V_{TRIG(L)}$	Over input supply range, V_{IN}	–	–	0.4	V
TRIGGER Pin Pull-down Resistor	R_{TRIGPD}		–	100	–	kΩ
GSOURCE On-Resistance to VIN	$R_{SrcDS(on)}$	$V_{IN} = 3.6$ V, $V_{GSOURCE} = 1.8$ V	–	5	–	Ω
GSINK On-Resistance to GND	$R_{SnkDS(on)}$	$V_{IN} = 3.6$ V, $V_{GSINK} = 1.8$ V	–	6	–	Ω
Propagation Delay (Rising)	t_{dr}	Connect GSOURCE to GSINK (measure at pin), $R_{GATE} = 12$ Ω, $C_{LOAD} = 6500$ pF, $V_{DRV} = 3.6$ V	–	30	–	ns
Propagation Delay (Falling)	t_{df}		–	30	–	ns
Output Rise Time	t_r		–	70	–	ns
Output Fall Time	t_f		–	70	–	ns

[1]Specifications over the range $T_A = -40°C$ to 85°C; guaranteed by design and characterization.

[2]Current limit guaranteed by design and correlation to static test. Refer to application section for peak current in actual circuits.

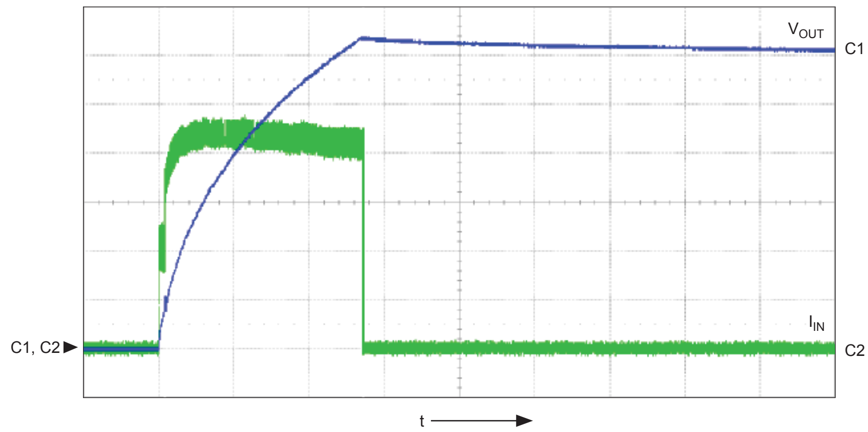
Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000
www.allegromicro.com

Performance Characteristics

Charging time at various peak switch current levels, with
V_{IN} = 3.6 V (bias voltage), V_{BAT} = 3.6 V (battery voltage), C_{OUT} = 100 µF / 330 V UCC (output capacitor), transformer type DCT5EPL-UxxS002 (TDK), T_A = 25°C

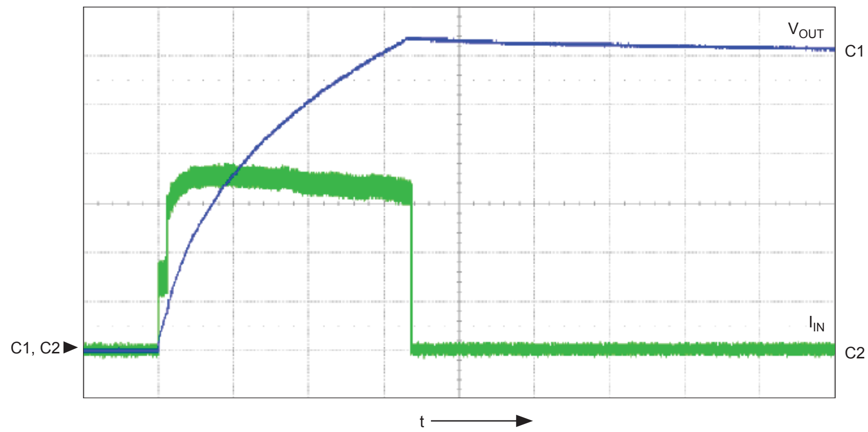
I_{SWpk} ≈ 2.3 A
(R_{SET} = 40 kΩ)

Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	I_{IN}	200 mA
t	time	1 s



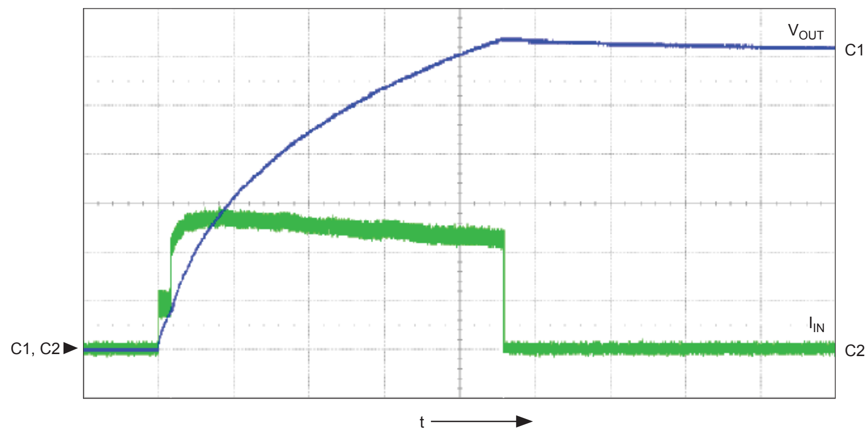
I_{SWpk} ≈ 1.9 A
(R_{SET} = 48 kΩ)

Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	I_{IN}	200 mA
t	time	1 s



I_{SWpk} ≈ 1.55 A
(R_{SET} = 60 kΩ)

Symbol	Parameter	Units/Division
C1	V_{OUT}	50 V
C2	I_{IN}	200 mA
t	time	1 s



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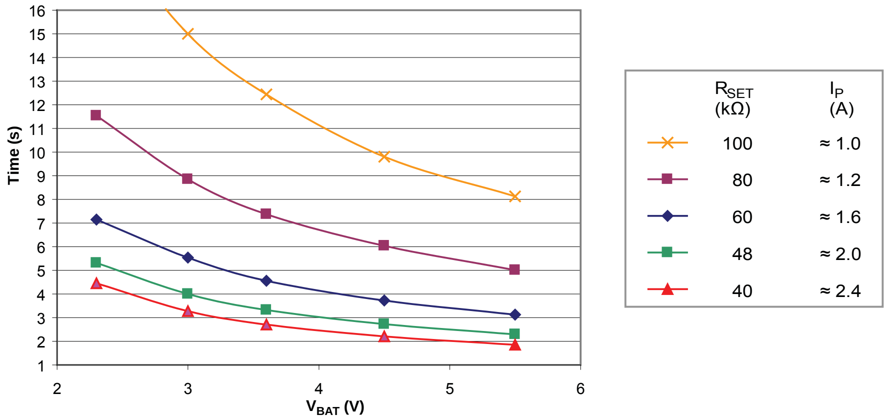
Performance Characteristics

V_{IN} = 3.6 V (bias voltage), C_{OUT} = 100 μF / 330 V UCC (output capacitor), transformer L_P = 7.5 μH, N = 10, T_A = 25°C

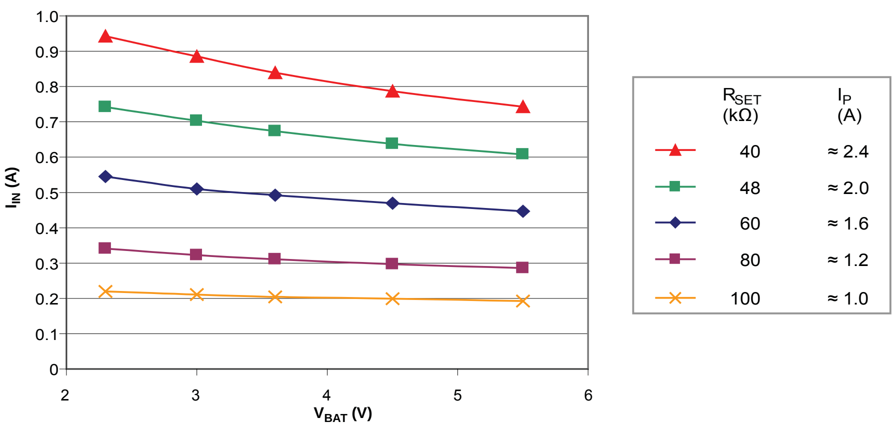
Charge Time versus Battery Voltage

V_{TLIM} = low



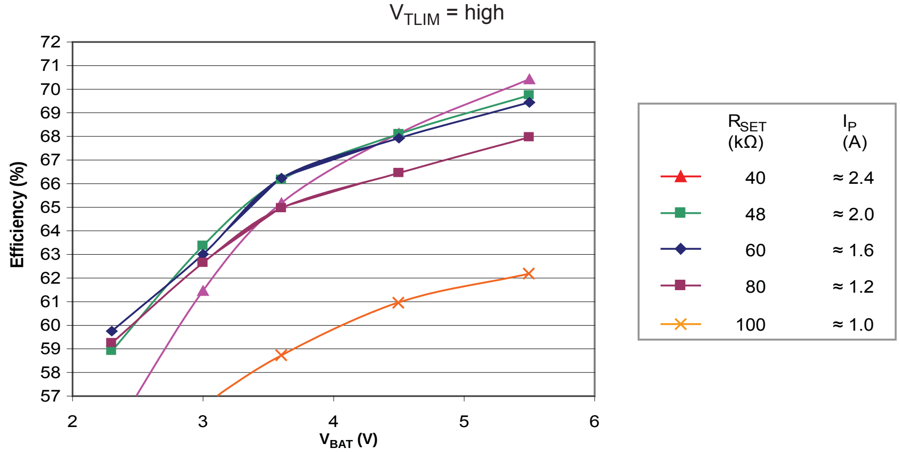
Average Input Current versus Battery Voltage

V_{TLIM} = low

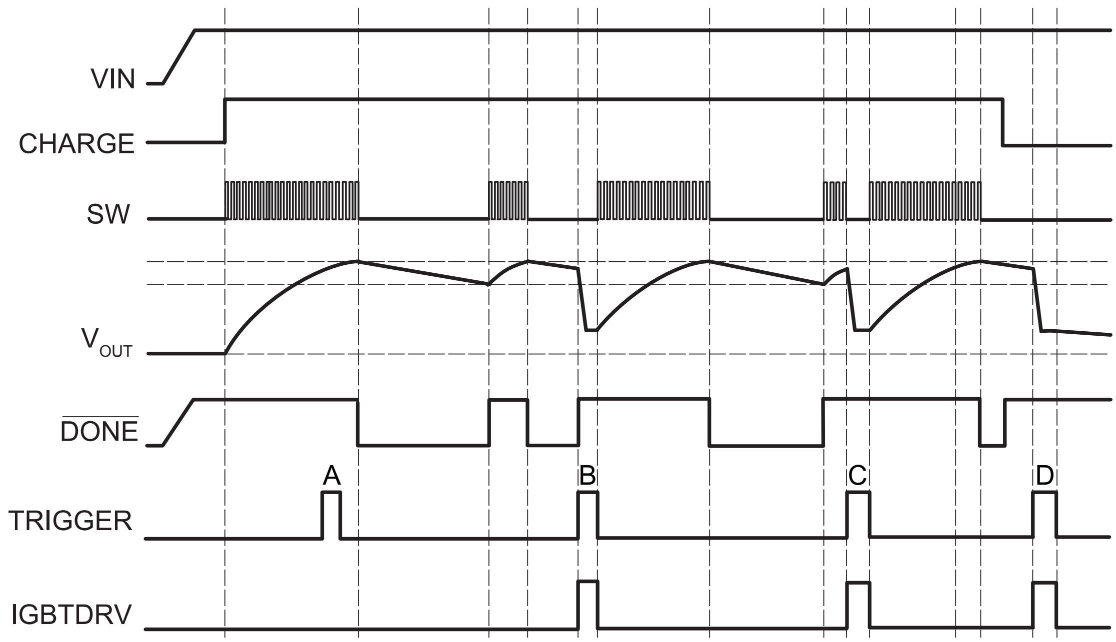


Efficiency versus Battery Voltage

V_{TLIM} = high



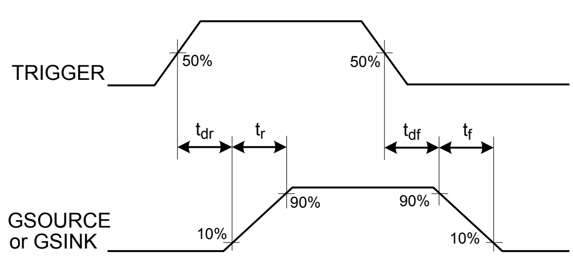
Timing and IGBT Interlock Function



Explanation of Events

Trigger A arrives before the first charging cycle is finished. IGBTDRV is disabled in this case (CHARGE = high and $\overline{\text{DONE}}$ = high).
Trigger B arrives during regulation mode while not refreshing. IGBTDRV is enabled. Charging resumes when TRIGGER goes low again.
Trigger C arrives during regulation mode while refreshing. Charging is stopped after present cycle. IGBTDRV is enabled. Charging resumes when TRIGGER goes low again.
Trigger D arrives while the A8427 is in low-power standby mode. IGBTDRV is always enabled in this case (CHARGE = low).

IGBT Drive Timing Definition



Application Information

General Operation Overview

The CHARGE pin enables the part and starts charging. The $\overline{\text{DONE}}$ open-drain indicator is pulled low when CHARGE is high and the target output voltage is reached. Charging is reinitiated when the REG pin voltage falls below the regulation threshold. Pulling the CHARGE pin low stops charging and forces the chip into low-power standby mode.

Timer Mode and Fast Charging Mode

The A8427 achieves fast charging times and high efficiency by operating in discontinuous conduction mode (DCM) through most of the charging process. The relationship of Timer Mode and Fast Charging Mode is shown in figure 1.

The IC operates in Timer Mode when beginning to charge a completely discharged photoflash capacitor, usually when the output voltage, V_{OUT}, is less than approximately 40 V (actual value depends on input voltage and transformer inductance). Timer Mode is a fixed period, 18 μs, off-time control. One advantage of having Timer Mode is that it limits the initial battery current surge and thus acts as a "soft-start." A time expanded view of a Timer Mode interval is shown in figure 2.

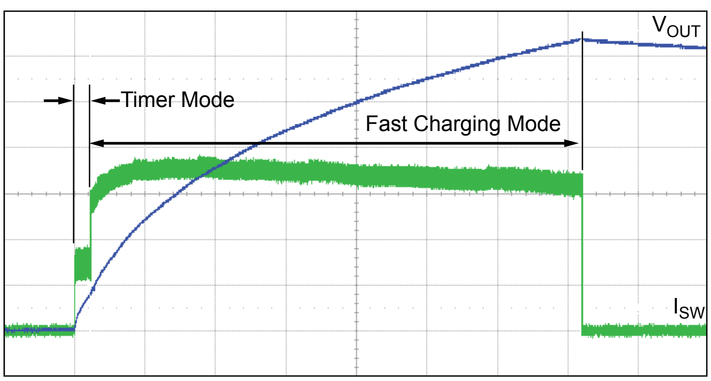
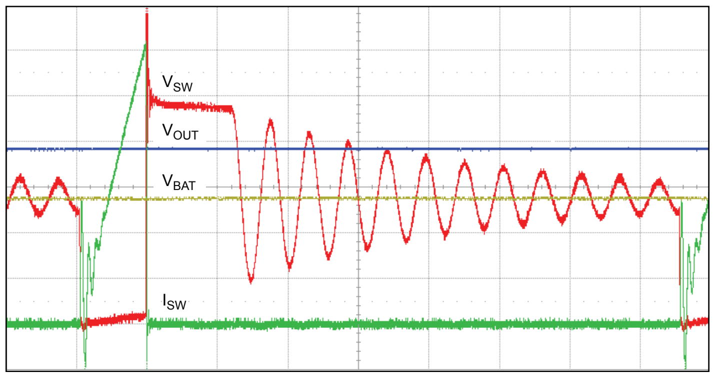


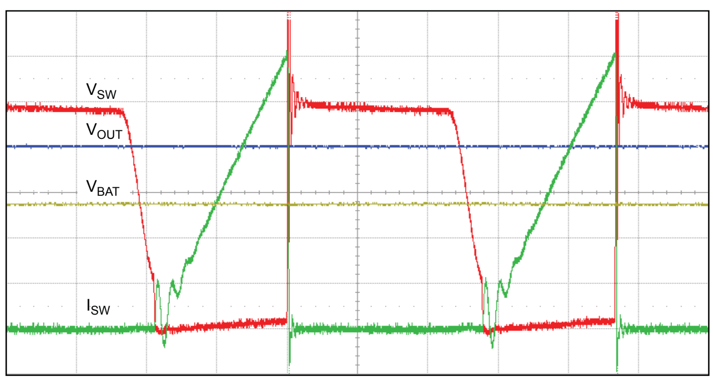
Figure 1. Relationship of Timer mode and Fast Charging mode

As soon as a sufficient voltage has built up at the output capacitor, the IC enters Fast-Charging Mode. In this mode, the next switching cycle starts after the secondary side current has stopped flowing, and the switch voltage has dropped to a minimum value. A proprietary circuit is used to allow minimum-voltage switching, even if the SW pin voltage does not drop to 0 V. This enables Fast-Charging Mode to start earlier than previously possible, thereby reducing the overall charging time. Minimum-voltage switching is shown in figure 3.



t = 2 μs/div; V_{OUT} =10 V/div; V_{BAT} =2 V/div.; V_{SW} =2 V/div; I_{SW} =200 mA/div. V_{IN} = 3.6 V; V_{BAT} =5.5 V; R_{SET}=80 kΩ; Transformer L_P= 7.5 μH, N = 10

Figure 2. Timer Mode



t = 1 μs/div; V_{OUT} =10 V/div; V_{BAT} =2 V/div.; V_{SW} =2 V/div; I_{SW} =200 mA/div. V_{IN} = 3.6 V; V_{BAT} =5.5 V; R_{SET}=80 kΩ; Transformer L_P= 7.5 μH, N = 10

Figure 3. Fast Charging Mode, minimum voltage

During Fast-Charging Mode, when V_{OUT} is high enough such that the reflected voltage (V_{OUT} / N) is greater than V_{BAT}, true zero-voltage switching (ZVS) is achieved. This further improves efficiency as well as reduces switching noise. A ZVS interval is shown in figure 4.

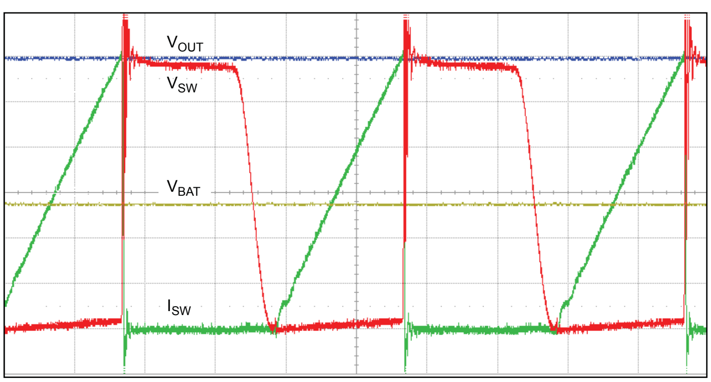
Output Voltage Regulation

When the REG pin is connected to VIN, the A8427 stops charging the output voltage after the reflected voltage ($V_{SW} – V_{IN}$) reaches 31.5 V. In this mode, charging can be reinitiated by cycling the CHARGE signal through a low-to-high transition.

The A8427 can also be used to regulate output voltage within a predetermined window. In this mode, connect a capacitor, CREG, and resistor, RREG, from the REG pin to GND (refer to the figure Application 3). When CHARGE is held high, the voltage monitoring circuit of the A8427 is always active, irrespective of the REG pin voltage level.

Voltage Regulation Using Predicitive Droop

The A8427 uses a technique called *Predictive Droop* for regulating the output capacitor voltage after the completion of a charging cycle. When the target output voltage is reached, the converter stops charging and output capacitor voltage will droop due to leakage current. An external resistor connected from REG pin to ground provides a RC discharge time constant. This time constant can be selected to mirror the droop rate of the output capacitor. When voltage at the REG pin drops to 80% of its reference value, the converter will start charging again and bring the output capacitor back to target voltage again.



t = 1 µs/div; V_{OUT} =10 V/div; V_{BAT} =2 V/div.; V_{SW} =2 V/div; I_{SW} =200 mA/div. V_{IN} = 3.6 V; V_{BAT} =5.5 V; R_{SET}=80 kΩ; Transformer L_P= 7.5 µH, N = 10

Figure 4. Zero-voltage switching

The time required for a RC network to discharge from V_0 to V_T is given by:

$$T = R \times C \times \ln(V_0 / V_T) . \qquad (1)$$

For example, if C = 10 µF, R = 10 M Ω and V_0 / V_T = 1.25, then T = 22 s. Assuming that the RC-discharge characteristic of the output capacitor matches that at the REG pin, we can predict that the output voltage has drooped 20%, and therefore it is time to recharge the output capacitor.

By implementing a Predictive Droop technique, no additional leakage paths are introduced on the secondary side, which helps to keep power losses to a minimum. By intentionally making the RC discharge time constant at the REG pin shorter than that of the output capacitor, we can also regulate the output voltage to a window tighter than the default 20% hysteresis.

Voltage Regulation Using Direct Sensing

If direct sensing from the secondary side is required, connect the REG pin to a resistor divider network across the output capacitor to enable output regulation. In this case, the charging cut-off is still controlled by primary side sensing (charging stops when reflected voltage reaches 31.5 V), but the regulation threshold is controlled by secondary-side sensing. When the CHARGE pin is high and the sensed output voltage falls below the lower V_{REG} threshold, the flyback charges the output capacitor again until the primary-side sensing stops further charging. This cycle repeats until the CHARGE pin is pulled low.

The benefit of this method is that this lower output voltage can be selected independently, simply by changing the resistor divider ratio. For example, if:

R1= 10 MΩ,

R2= 33.2 kΩ, and

$V_{REG(L)}$ = 0.96 V,

then:

$$V_{OUT}(\text{Low}) = V_{REG(L)} \times (R1 / R2 + 1) = 290 \text{ V} . \quad (2)$$

Selection of Switching Current Limit

The A8427 features continuously adjustable peak switching current between 0.8 and 2.4 A. This is done by selecting the value of an external resistor RSET, connected from the ISET pin to GND, which determines the ISET bias current, and therefore the switching current limit.

To the first order approximation, I_{SWlim} is related to I_{SET} and R_{SET} according to the following equation :

$$I_{SWlim} = I_{SET} \times K = V_{SET} / R_{SET} \times K , \quad (3)$$

where V_{SET} is 1.2 V and K is approximately 74000 when bias voltage, V_{IN}, is 3.6 V.

In applications, the actual switching current limit is affected by bias voltage, battery voltage, and also the transformer primary inductance, L_P. If necessary, the following expressions can be used to determine I_{SWlim} more accurately:

$$I_{SET} = V_{SET} / (R_{SET} + R_{SET(INT)} - K \times R_{GND(INT)}), (4)$$

where:

$R_{SET(INT)}$ is the internal resistance of the I_{SET} pin (1 kΩ typical),

$R_{GND(INT)}$ is the internal resistance of the bonding wire for the GND pin (27 mΩ typical), and

$K = (K' + V_{IN} \times K'')$, with K' = 67500 and $K'' \approx$ 2200 at T_A = 25°C.

Then,

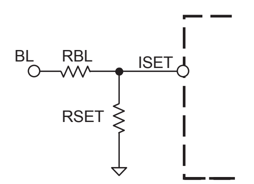
$$I_{SWlim} = I_{SET} \times K + V_{BAT} / L_P \times t_D , \quad (5)$$

where t_D is the delay in SW turn-off (0.1 μs typical).

Figure 5 can be used to determine the relationship between R_{SET} and I_{SWlim} at various bias voltages.

Smart Current Limit (Optional)

With the help of some simple external logic, the user can change the charging current according to the battery voltage. As an example (refer to the circuit diagram below), assume that the ISET current level is normally 30 μA (for I_{SWlim} = 2.2 A). Further, when the battery voltage drops below 2.5 V, an external BL (battery-low) signal comes high. A resistor, RBL, connected from the BL node to the ISET pin, then injects 10 μA into RSET. This effectively reduces ISET current to 20 μA (for I_{SWlim} = 1.5 A). The disadvantage of this method is that the 10 μA current is always flowing whenever the BL signal goes high.



IGBT Gate Driver Interlock

The TRIGGER pin controls the IGBT gate driver. However, triggering is disabled (locked) during charging. This is to prevent switching noises from interfering with the IGBT driver. After the CHARGE pin goes high (at the start of a charging cycle), the IC must wait for completion of the charging cycle ($\overline{\text{DONE}}$ goes low) before triggering can be enabled, according to the following chart:

Conditions		Resulting State
CHARGE	$\overline{\text{DONE}}$	IGBT Gate Driver
Low	Don't Care	Enabled
High	High	Disabled
High	Low	Enabled

After completion of the charging cycle, if the charge pin is kept high and REG is enabled, the IC will periodically recharge the output. If a trigger signal comes in during a recharge cycle, charging will be halted immediately and the IGBT gate driver will be allowed to fire after a delay of less than 1 µs. Charging resumes after the trigger signal is removed.

Red Eye Reduction

The IGBT gate driver is always enabled when the CHARGE pin is low. If the CHARGE pin is disabled before sufficient voltage has built up on the output capacitor, the flash may not fire. In the case of red-eye reduction flashes, it is recommended to keep the CHARGE pin low until completion of triggering pulses. This ensures that the IGBT gate driver will remain enabled regardless of the $\overline{\text{DONE}}$ pin state.

Selection of Transformer

1. The transformer turns ratio ($N = N_S/N_P$) determines the output voltage:

$$V_{OUT} = 31.5 \times N - V_d \,, \qquad (6)$$

where V_d is the forward drop of the output diode.

2. The primary inductance L_P determines the on-time of the switch:

$$t_{on} = -L_P / R \times \ln\left(1 - I_{SWlim} \times R / V_{BAT}\right) \,, \qquad (7)$$

where R is the total resistance in the primary current path (including the $R_{DS(on)}$ of SW and the DC resistance of the transformer).

If V_{BAT} is much larger than $I_{SWlim} \times R$, then t_{on} can be approximated by:

$$t_{on} = I_{SWlim} \times L_P / V_{BAT} \,. \qquad (8)$$

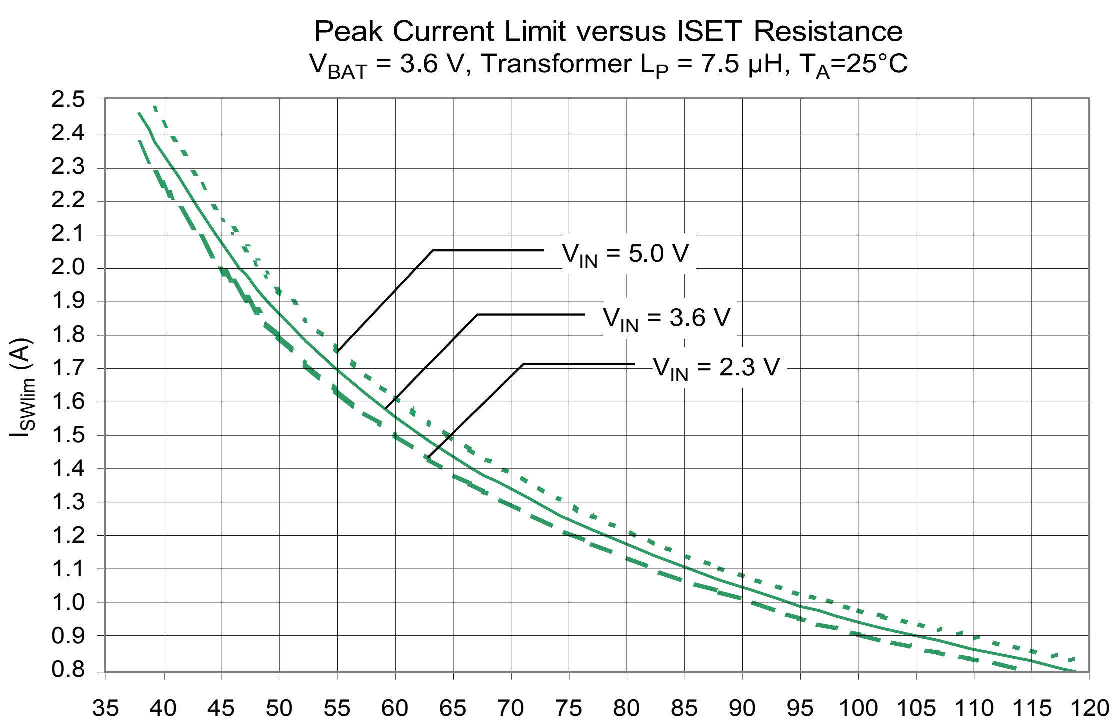


Figure 5. Chart of current versus limit settings

Allegro MicroSystems, Inc.
115 Northeast Cutoff, Box 15036
Worcester, Massachusetts 01615-0036 (508) 853-5000
www.allegromicro.com

3. The secondary inductance, L_S , determines the off-time of the switch:

$$t_{off} = (I_{SWlim} / N) \times L_S / V_{OUT} \ . \qquad (9)$$

Because $L_S / L_P = N \times N$:

$$t_{off} = (I_{SWlim} \times L_P \times N) / V_{OUT} \ . \qquad (10)$$

The minimum pulse width for t_{off} determines what is the minimum primary inductance required for the transformer. For example, if I_{SWlim} = 1.0 A, N = 10, and V_{OUT} = 315 V, then L_P must be at least 6.3 µH in order to keep t_{off} at 200 ns or longer.

In general, choosing a transformer with a larger L_P results in higher efficiency (because a larger L_P means lower switch frequency and hence lower switching loss). But a transformer with a larger L_P also requires more windings and a larger magnetic core. Therefore a trade-off must be made between transformer size and efficiency.

Component Selection

Selection of the flyback transformer should be based on the peak current, according to the following table. Note: The maximum peak current must be derated at higher temperatures.

I_{Peak} Range (A)	Supplier	Part Number	L_P (µH)	N
1.0 to 2.0	TDK	LDT565630T-001	6	10.4
1.4 to 2.4	TDK	LDT565630T-041	4.7	10.4
0.8 to 2.0	TDK	DCT5EPL-UxxS002	8	10
0.8 to 2.4	TDK	DCT9.5/5ER-UxxS003	7.6	10

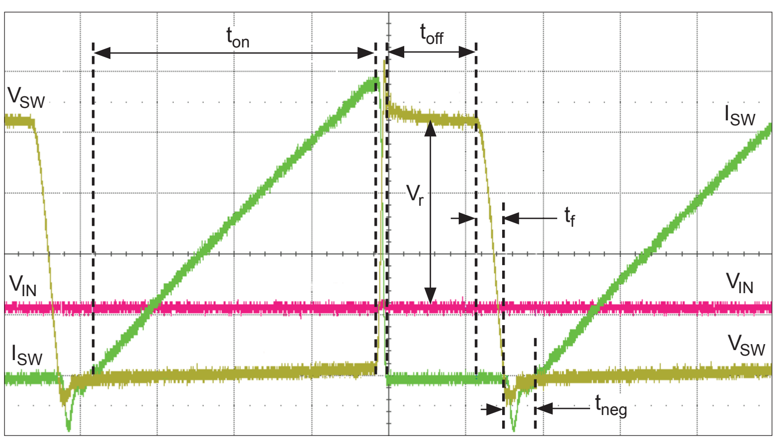
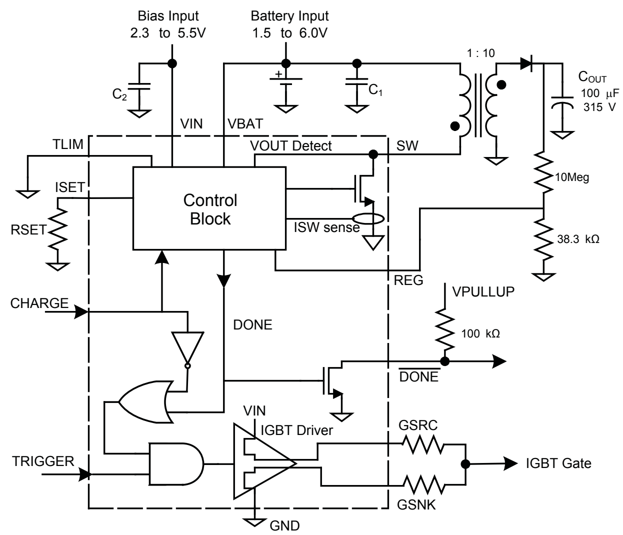
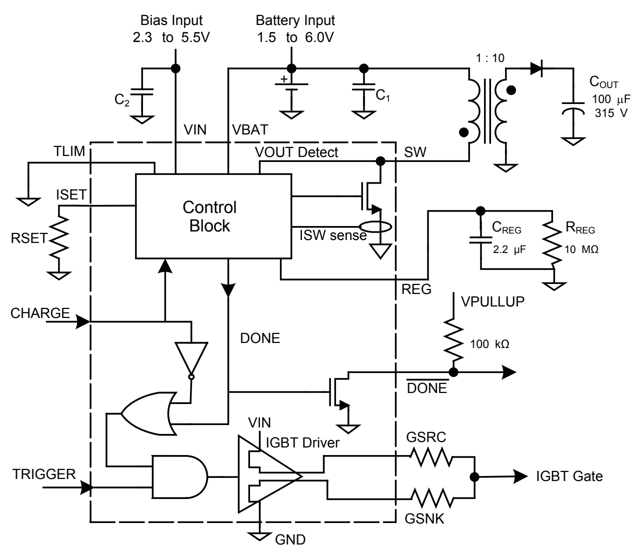


Figure 6. Relationship of t_{off} and switch output.

Typical Applications

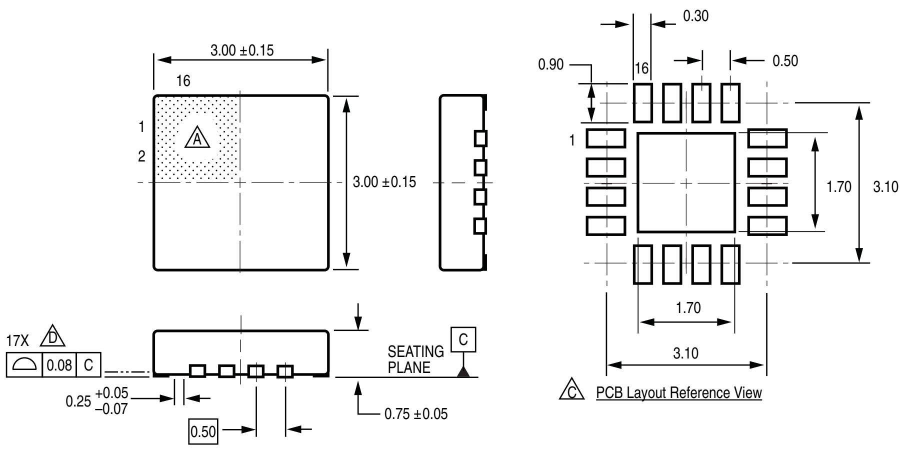


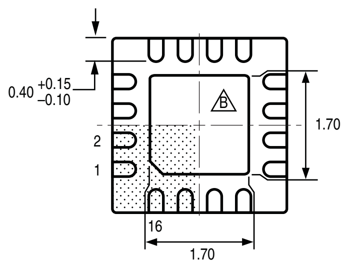
Application 2: Maintaining output target voltage by directly monitoring the output voltage droop (REG pin connected to a secondary-side resistor divider).



Application 3: Maintaining output target voltage by *predicting* the output voltage droop (REG pin connected to a primary-side RC network).

Package ES, 3 mm x 3 mm 16-Contact TQFN
with Exposed Thermal Pad





For reference only
(reference JEDEC MO-220WEED)
Dimensions in millimeters
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (reference only, terminal #1 identifier appearance at supplier discretion)

C Reference land pattern layout (reference IPC7351 QFN50P300X300X80-17W4M);
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

D Coplanarity includes exposed thermal pad and terminals

Revision History

Revision	Revision Date	Description of Revision
Rev. 1	April 19, 2012	Update Selection Guide, miscellaneous format changes