

# TQP3M9008

## High Linearity LNA Gain Block

### Applications

- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / EDGE / CDMA
- General Purpose Wireless

### Product Features

- 50-4000 MHz
- 20.6 dB Gain @ 1.9 GHz
- +36 dBm Output IP3
- 1.3 dB Noise Figure @ 1.9 GHz
- 50 Ohm Cascadable Gain Block
- Unconditionally stable
- High input power capability
- +5V Single Supply, 85 mA Current
- SOT-89 Package

### General Description

The TQP3M9008 is a cascadable, high linearity gain block amplifier in a low-cost surface-mount package. At 1.9 GHz, the amplifier typically provides 20.6 dB gain, +36 dBm OIP3, and 1.3 dB Noise Figure while only drawing 85 mA current. The device is housed in a leadfree/green/RoHS-compliant industry-standard SOT-89 package using a NiPdAu plating to eliminate the possibility of tin whiskering.

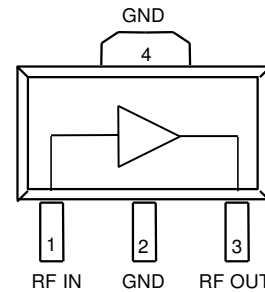
The TQP3M9008 has the benefit of having high gain across a broad range of frequencies while also providing very low noise. This allows the device to be used in both receiver and transmitter chains for high performance systems. The amplifier is internally matched using a high performance E-pHEMT process and only requires an external RF choke and blocking/bypass capacitors for operation from a single +5V supply. The internal active bias circuit also enables stable operation over bias and temperature variations.

The TQP3M9008 covers the 0.05-4 GHz frequency band and is targeted for wireless infrastructure or other applications requiring high linearity and/or low noise figure.



3-pin SOT-89 Package

### Functional Block Diagram



### Pin Configuration

Pin #	Symbol
1	RF Input
3	RF Output / Vcc
2, 4	Ground

### Ordering Information

Part No.	Description
TQP3M9008	High Linearity LNA Gain Block
TQP3M9008-PCB_IF	TQP3M9008 EVB 0.05-0.5 GHz
TQP3M9008-PCB_RF	TQP3M9008 EVB 0.5-4 GHz

Standard T/R size = 1000 pieces on a 7" reel.

### Specifications

#### Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to +150 °C
RF Input Power, CW, 50 Ω, T = 25 °C	+23 dBm
Device Voltage, V <sub>dd</sub>	+7 V
Reverse Device Voltage	-0.3V

Operation of this device outside the parameter ranges given above may cause permanent damage.

#### Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V <sub>dd</sub>	+3	+5	+5.25	V
T(case)	-40		85	°C
T <sub>j</sub> (for >10 <sup>6</sup> hours MTTF)			190	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

#### Electrical Specifications

Test conditions unless otherwise noted: +25 °C, +5V V<sub>supply</sub>, 50 Ω system.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		4000	MHz
Test Frequency			1900		MHz
Gain		19	20.6	22	dB
Input Return Loss			16		dB
Output Return Loss			17		dB
Output P1dB			+20		dBm
Output IP3	P <sub>out</sub> = 3 dbm/tone, Δf= 1 MHz	+32.5	+36		dBm
Noise Figure			1.3		dB
V <sub>dd</sub>			+5		V
Current, I <sub>dd</sub>			85	100	mA
Thermal Resistance (junction to base) θ <sub>jb</sub>				38.7	°C/W

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## High Linearity LNA Gain Block



### Device Characterization

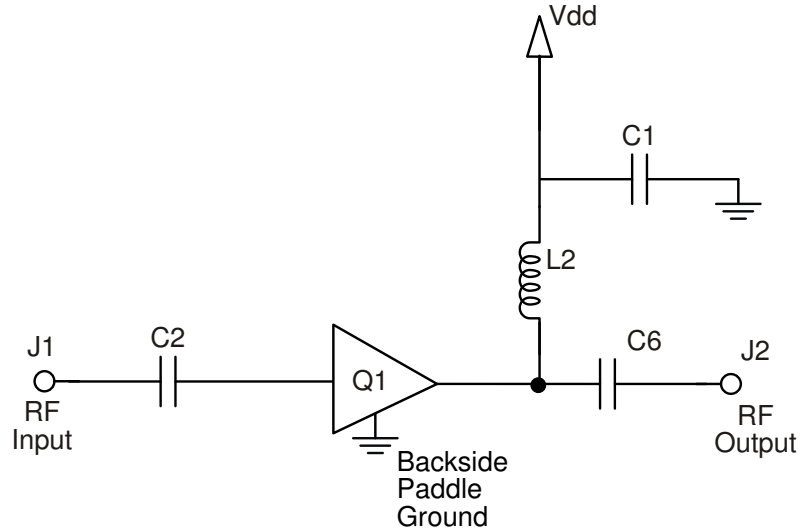
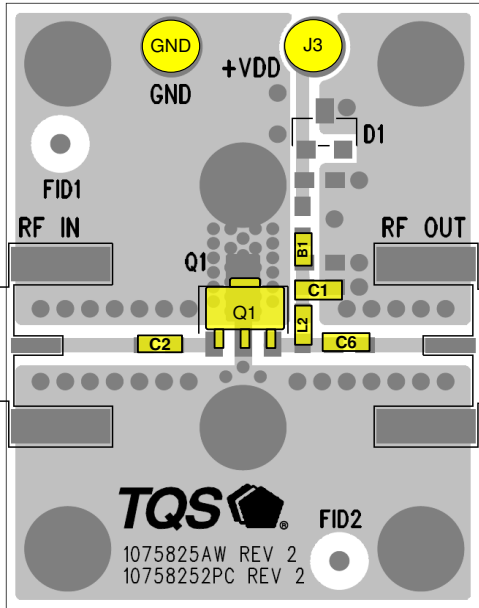
$V_{dd} = +5\text{ V}$ ,  $I_{dd} = 85\text{ mA}$ ,  $T = +25\text{ }^{\circ}\text{C}$ , calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-12.52	-170.01	23.61	172.94	-26.71	0.57	-9.82	177.18
100	-11.90	-175.09	23.48	167.73	-26.65	-1.85	-9.88	171.87
200	-11.41	177.96	23.07	159.45	-26.63	-5.51	-10.01	162.15
400	-11.36	166.96	22.66	144.06	-26.65	-12.85	-10.48	145.49
600	-11.58	154.05	22.31	129.39	-26.65	-19.62	-10.67	129.34
800	-11.76	147.21	21.98	114.61	-26.71	-26.09	-11.30	111.77
1000	-12.33	139.09	21.71	99.52	-26.78	-33.35	-12.37	94.27
1200	-12.65	132.05	21.41	85.59	-26.92	-39.92	-13.06	77.75
1400	-13.27	126.25	21.02	70.96	-27.11	-47.72	-14.33	58.69
1600	-13.58	116.91	20.78	56.21	-27.39	-56.48	-15.41	36.83
1800	-13.92	110.23	20.45	41.84	-27.60	-63.31	-16.28	15.29
2000	-14.30	103.50	20.30	27.87	-28.05	-71.56	-17.53	-11.21
2200	-15.07	94.63	19.92	13.81	-28.50	-80.24	-18.03	-39.05
2400	-15.75	85.16	19.71	-1.08	-28.73	-88.86	-17.43	-65.92
2600	-16.78	72.66	19.45	-15.98	-29.42	-96.81	-16.62	-94.17
2800	-18.00	55.24	19.22	-31.32	-29.90	-105.73	-14.89	-115.00
3000	-19.76	25.52	18.95	-46.86	-30.63	-117.08	-14.06	-131.67
3200	-19.90	-16.80	18.64	-63.51	-31.00	-128.03	-13.12	-148.29
3400	-17.79	-58.97	18.31	-80.47	-31.77	-139.44	-12.40	-160.20
3600	-14.26	-90.75	17.71	-98.47	-32.84	-154.36	-11.92	-173.86
3800	-11.29	-114.34	16.98	-117.12	-33.98	-168.14	-11.23	174.45
4000	-8.73	-132.65	16.09	-135.80	-34.80	173.11	-10.66	167.57

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## Application Circuit Configuration



**Notes:**

1. See PC Board Layout, page 8 for more information.
2. Components shown on the silkscreen but not on the schematic are not used.
3. B1 (0 Ω jumper) may be replaced with copper trace in the target application layout.
4. The recommended component values are dependent upon the frequency of operation.
5. All components are of 0603 size unless stated on the schematic.

## Bill of Material

Reference Designation	Frequency (MHz)	
	TQP3M9008-PCB_IF	TQP3M9008-PCB_RF
	50 - 500	500 - 4000
Q1	TQP3M9008	
C2, C6	1000 pF	100 pF
C1	0.01 uF	0.01 uF
L2	330 nH	68 nH
D1	Do Not Place	
B1	0 Ω	

Performance can be optimized at frequency of interest by using recommended component values shown in the table below.

Reference Designation	Frequency (MHz)			
	500	2000	2500	3500
C2, C6	100 pF	22 pF	22 pF	22 pF
L2	82 nH	22 nH	18 nH	15 nH

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## High Linearity LNA Gain Block



### Typical Performance TQP3M9008-PCB\_RF

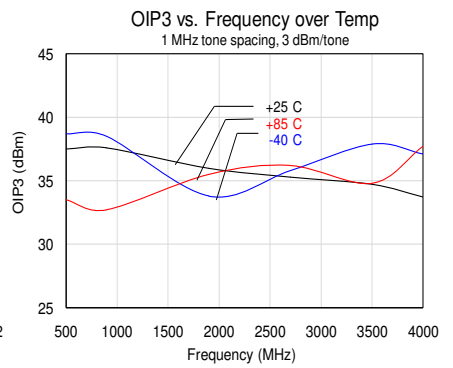
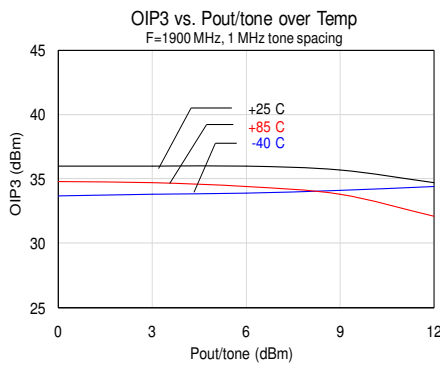
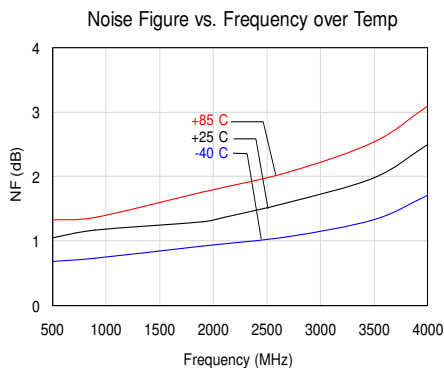
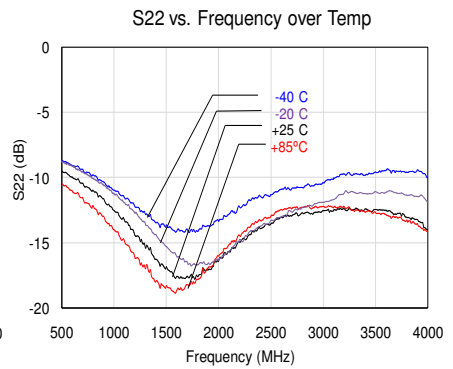
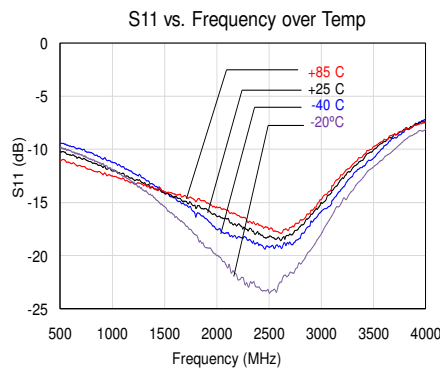
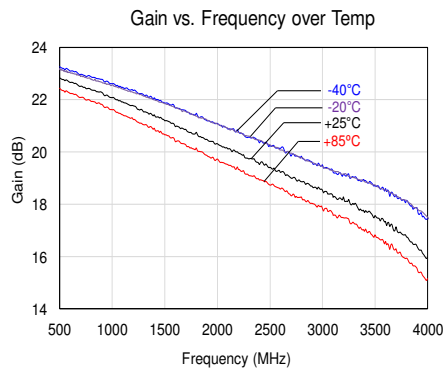
Test conditions unless otherwise noted: +25 °C, +5V, 85 mA, 50 Ω system.

Frequency	MHz	500	900	1900	2700	3500	4000
Gain	dB	22.8	22.3	20.6	19.0	17.6	16.0
Input Return Loss	dB	10	12	16	18	10	7.3
Output Return Loss	dB	9.5	12	17	13	12.4	14
Output P1dB	dBm	+20.9	+19.7	+19.9	+19.4	+19.7	+18.5
OIP3 [1]	dBm	+37.5	+37.6	+36	+35.3	+34.7	+33.7
Noise Figure [2]	dB	1.1	1.1	1.3	1.6	2	2.5

Notes:

- OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz.
- Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1dB @ 2 GHz.

### RF Performance Plots

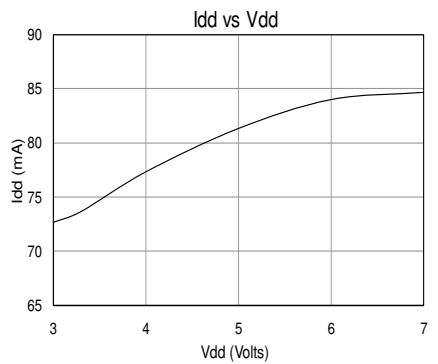
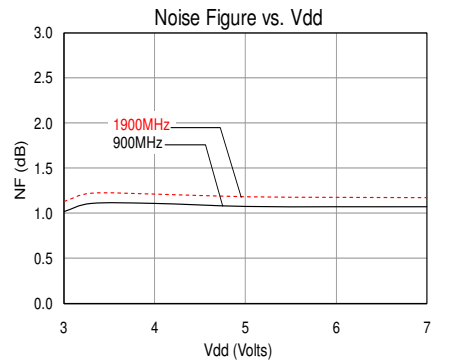
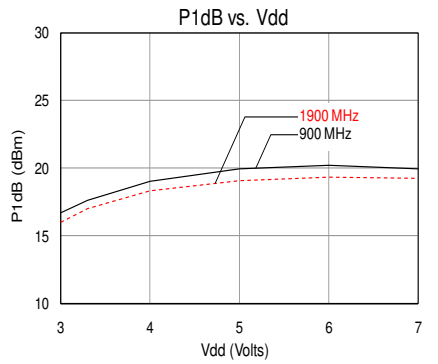
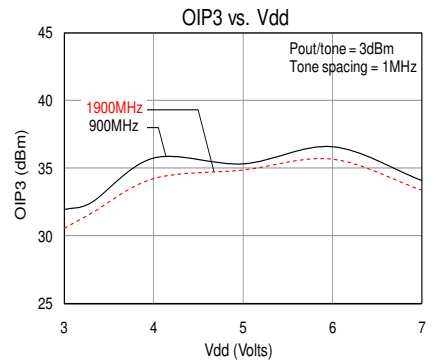
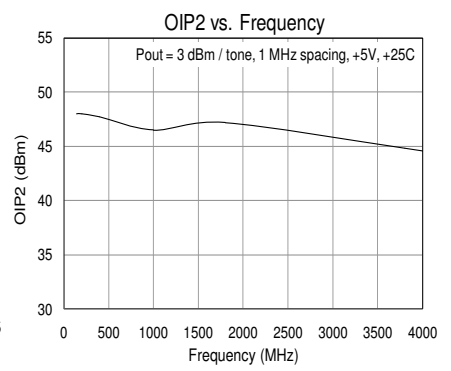
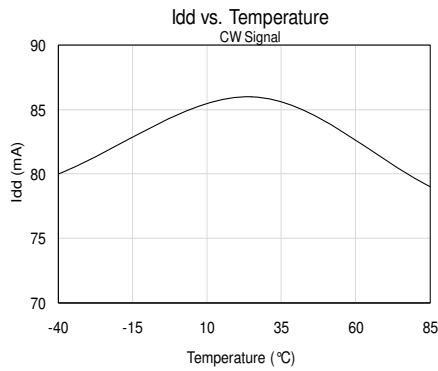
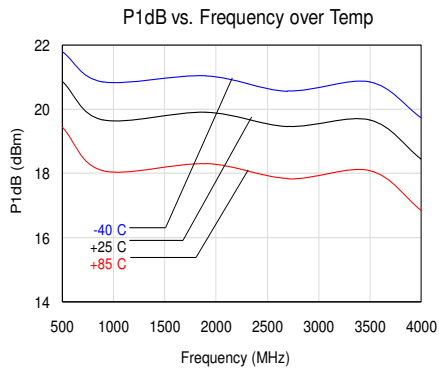


# TQP3M9008

## High Linearity LNA Gain Block



### RF Performance Plots



# TQP3M9008

## High Linearity LNA Gain Block



### Typical Performance TQP3M9008-PCB\_IF

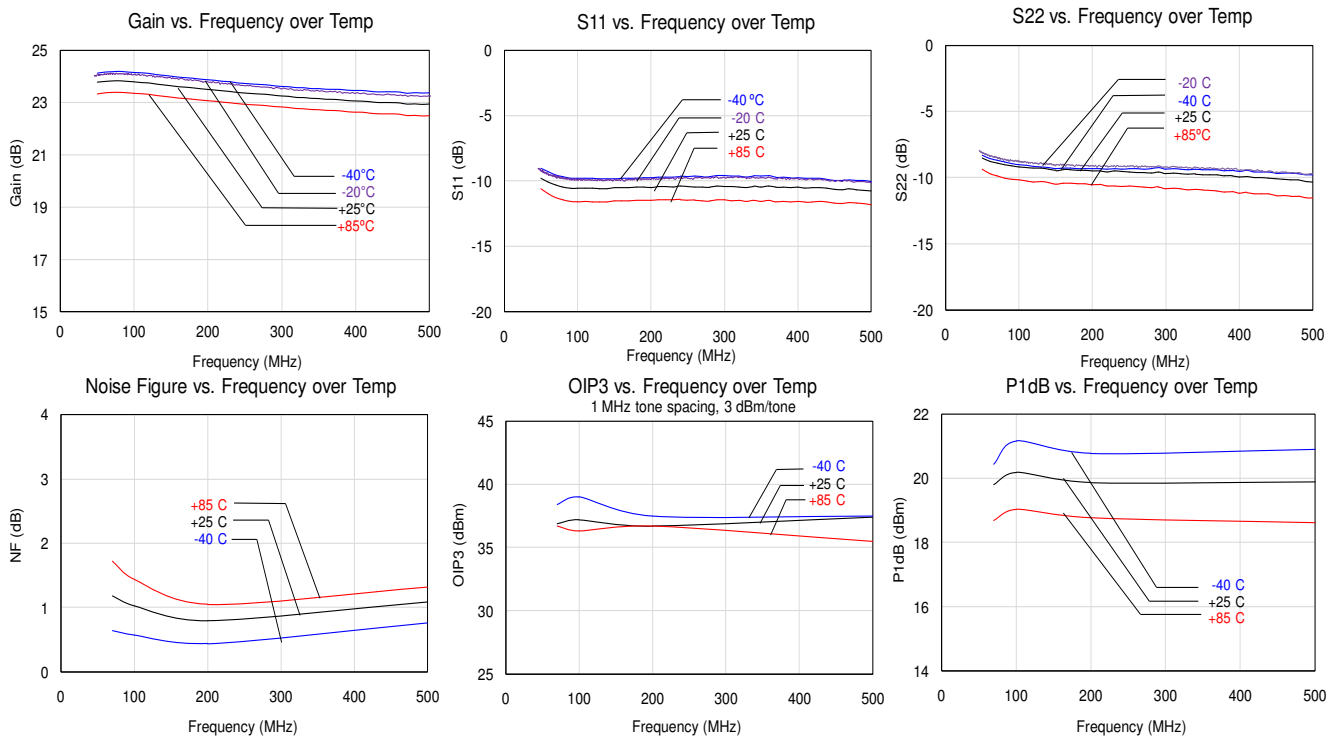
Test conditions unless otherwise noted: +25°C, +5V, 85 mA, 50 Ω system.

Frequency	MHz	70	100	200	500
Gain	dB	23.2	23.2	22.9	22.3
Input Return Loss	dB	10	11	11	11
Output Return Loss	dB	9	9	10	10
Output P1dB	dBm	+19.8	+20.2	+19.9	+19.9
OIP3 [1]	dBm	+37	+37	+37	+37
Noise Figure [2]	dB	1.2	1.1	0.8	1.1

Notes:

- OIP3 measured with two tones at an output power of +3 dBm / tone separated by 1 MHz.
- Noise figure data shown in the table above is measured on evaluation board which includes board losses of around 0.1 dB @ 2 GHz.

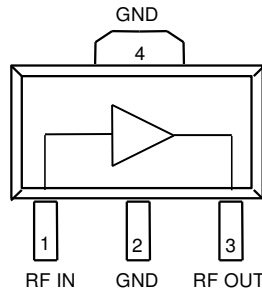
### IF Performance Plots



# TQP3M9008

High Linearity LNA Gain Block

## Pin Description

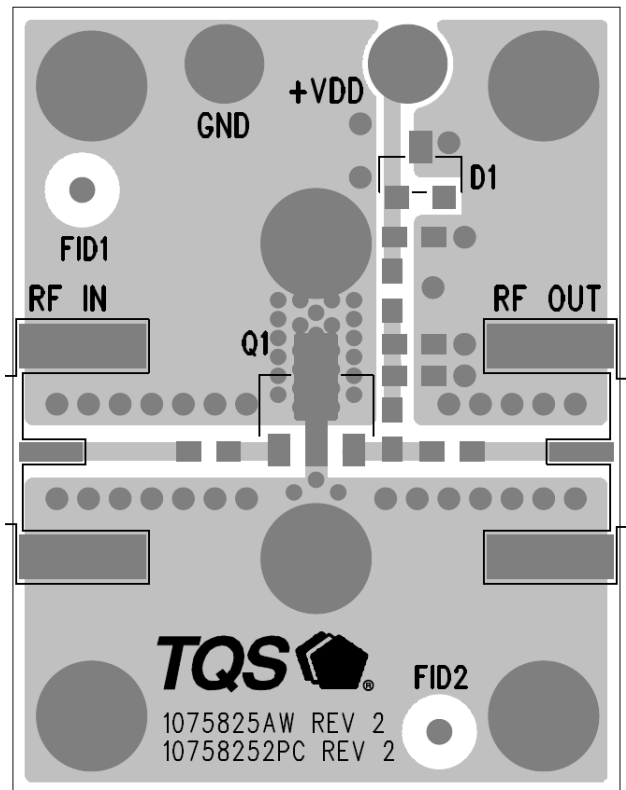
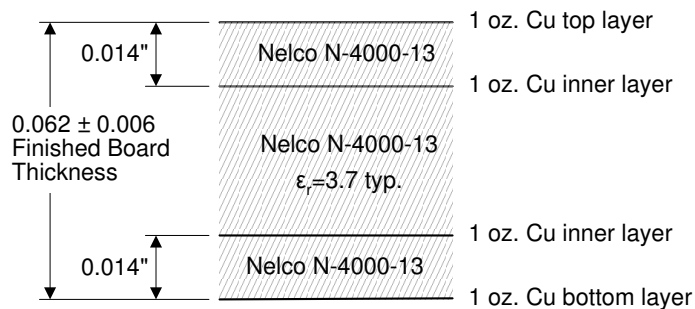


Pin	Symbol	Description
1	RF IN	Input, matched to 50 ohms. External DC Block is required.
2, 4	GND	RF/DC Ground Connection
3	RFout / Vdd	Output, matched to 50 ohms, External DC Block is required and supply voltage

## Evaluation Board PCB

### PC Board Layout

TriQuint PCB 1075825 Material and Stack Up





# TQP3M9008

## High Linearity LNA Gain Block

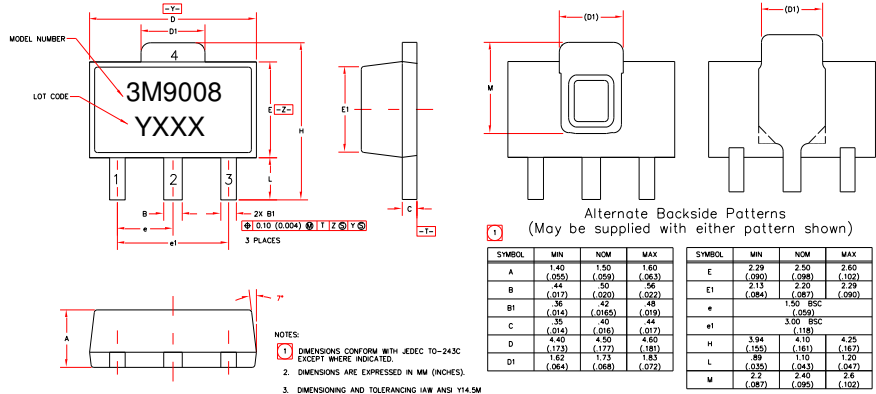


### Mechanical Information

### Package Information and Dimensions

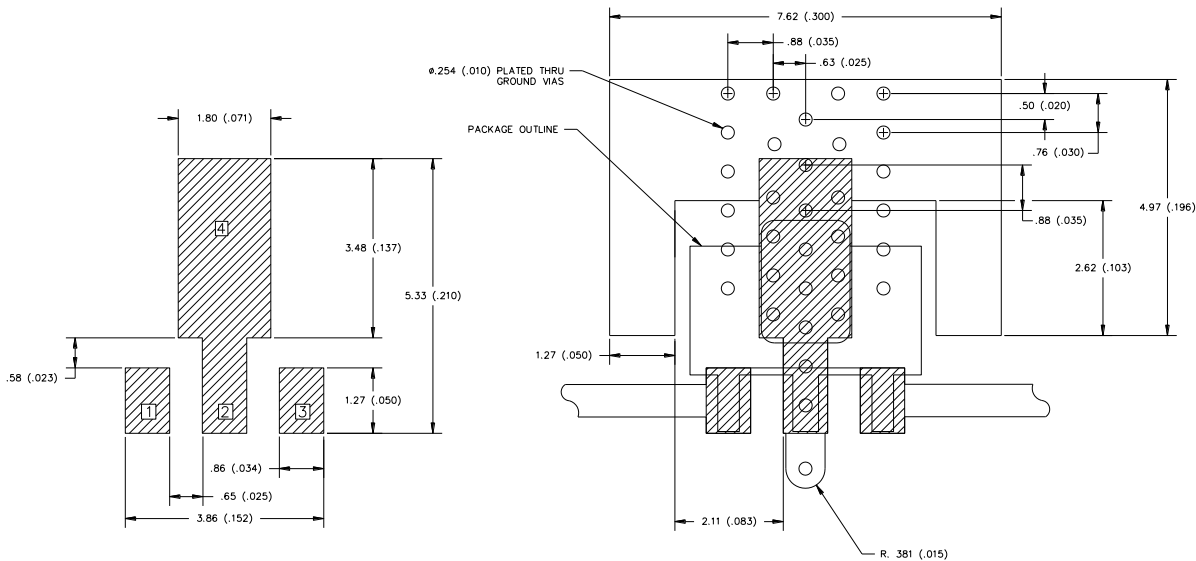
Markings:

Part number: 3M9008  
 Assembly code: 'Y' is last digit of part  
 manufacture year. 'XXX' is lot code.



### PCB Mounting Pattern

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:

1. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
2. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
3. RF trace width depends upon the PC board material and construction.
4. Use 1 oz. Copper minimum.

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**High Linearity LNA Gain Block**

## Product Compliance Information

### ESD Sensitivity Ratings



**Caution! ESD-Sensitive Device**

ESD Rating: 1A  
Value: Passes  $\geq 250V$  to  $< 500 V$   
Test: Human Body Model (HBM)  
Standard: JEDEC Standard JESD22-A114

ESD Rating: IV  
Value: Passes  $\geq 1000 V$   
Test: Charged Device Model (CDM)  
Standard: JEDEC Standard JESD22-C101

### MSL Classification

MSL Rating: 3  
Floor Life: 168 hours max. at  $\leq 30^{\circ}C$  / 60% RH  
Test:  $+260^{\circ}C$  convection reflow  
Standard: JEDEC standard IPC/JEDEC J-STD-020

### Solderability

Compatible with both lead-free ( $260^{\circ}C$  max. reflow temp.) and lead ( $245^{\circ}C$  max. reflow temp.) soldering processes.

Package lead plating: NiPdAu

### RoHS Compliance

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ( $C_{15}H_{12}Br_4O_2$ ) Free
- PFOS Free
- SVHC Free

## Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: [info-sales@tqs.com](mailto:info-sales@tqs.com)

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Fax: +1.503.615.8902

For technical questions and application information: Email: [sjcapplcations.engineering@tqs.com](mailto:sjcapplcations.engineering@tqs.com)

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