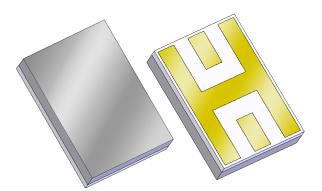
# Applications

- S-Band
- For high-selectivity applications





## Functional Block Diagram

• Usable bandwidth 30 MHz

**Product Features** 

- Low loss
- High selectivity
- Single-ended operation
- Ceramic chip-scale Package (CSP)
- Small Size
- Hermetic **RoHS** compliant, **Pb**-free

## Pin Configuration

Pin # SE-Balanced	Description
I/O	Input/Output
GND	Ground

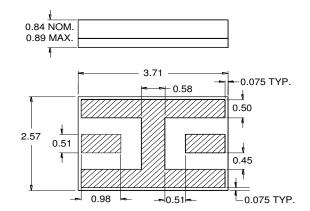
# I/O

Overall width, length, and thickness are the only critical dimensions. All other dimensions are for reference only.

Dimensions shown are nominal in millimeters All tolerances are  $\pm 0.13$ mm except overall length and width  $\pm 0.25$ mm

#### Body: *Sapphire* Package: *Alumina*

Terminations: Au plating 0.5 - 2.5µm, over a 2.0 – 6.0 µm Ni plating



# **Ordering Information**

Part No.	Description
880157	packaged part
880157 Eval Board	evaluation board



## **Specifications**

# Electrical Specifications (1)

Specified Temperature Range: <sup>(2)</sup> -40 to +85 °C

Parameter <sup>(3)</sup>	Conditions	Min	Typical <sup>(4)</sup>	Max	Units
Center Frequency		-	2560	-	MHz
Maximum Insertion Loss	@ 2560 MHz	-	3.8	4.5	dB
3dB Bandwidth	Reference loss at 2560 MHz	30	38	-	MHz
40dB Lower Frequency Edge		2505	2525	-	MHz
40dB Upper Frequency Edge		-	2595	2610	MHz
VSWR	@ 2560 MHz	-	1.5	2.0	-
Source Impedance (single-ended) <sup>(5)</sup>		-	50	-	Ω
Load Impedance (single-ended) <sup>(5)</sup>		-	50	-	Ω

Notes:

1. All specifications are based on the TriQuint schematic for the main reference design shown on page 3

2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature

3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances

4. Typical values are based on average measurements at room temperature

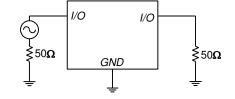
5. This is the optimum impedance in order to achieve the performance shown

## **Reference Design**



## Schematic

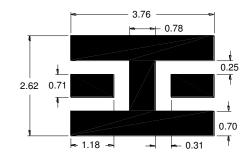




```
50 Ω
Single-ended
Input
```

# PC Board

# **Mounting Configuration**



Refer to **<u>PCB Layout</u>** for more information.

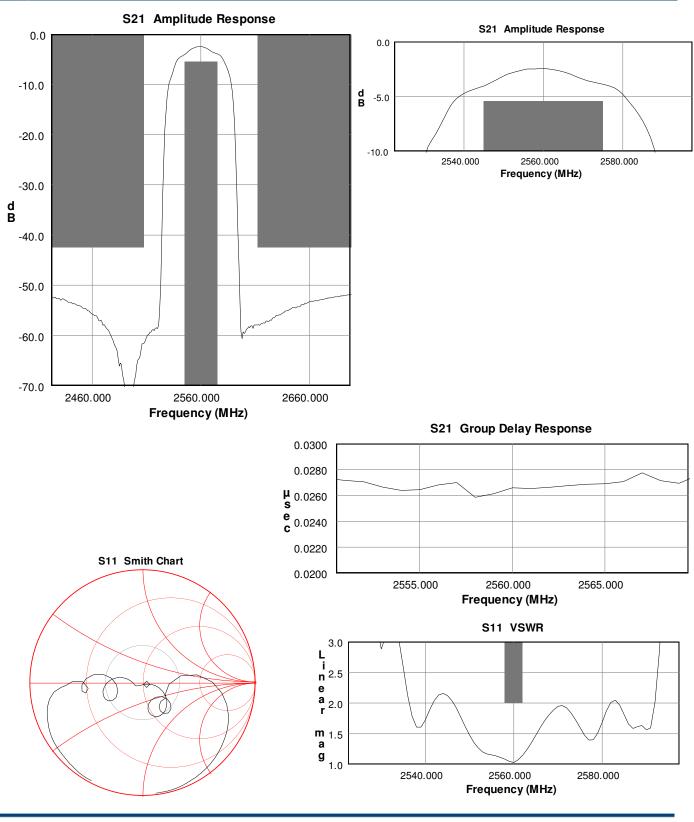
#### Notes:

1. All dimensions are in millimeters.

2. This footprint represents a recommendation only.



## Typical Performance (at room temperature)

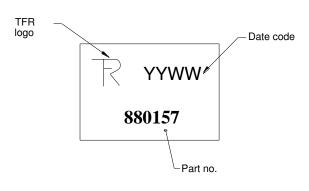


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## **Mechanical Information**

# Marking



The date code consists of: YY = Iast digit of year, WW = 2 digit week

## **Tape and Reel Information**

Tape and Reel available upon request EIA-481

Tinning available per J-STD-001

## **Absolute Maximum Ratings**

Parameter	Rating
Operating Temperature	-40 to +85 °C
Storage Temperature	-55 to +100 °C
Maximum Input Power	+23 dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.



## **Product Compliance Information**

## **ESD** Information



JEDEC Standard JESD22-A115

Value:	Passes $\geq 4000$ V min.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114
Value:	Passes $\geq 200$ V min.
Test:	Machine Model (MM)

Refer to ESD Sensitivity for data

Standard:

## Solderability

Compatible with the latest version of J-STD-020, lead free solder,  $260^{\circ}C$ 

Refer to Soldering Profile for recommended guidelines.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ( $C_{15}H_{12}Br_40_2$ ) Free
- PFOS Free
- SVHC Free

## **Contact Information**

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web:	www.triquint.com	Tel:	+1.407.886.8860
Email:	info-sales@tqs.com	Fax:	+1.407.886.7061

For technical questions and application information:

Email: info-defense@tqs.com

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