

TAT8857

CATV Doubler – Hybrid RFIC



Applications

- CATV Line Amplifiers
- CATV System Amplifiers
- Distribution Nodes
- Green Applications

Product Features

- 75 Ω , 40 – 1000 MHz Bandwidth
- GaAs pHEMT & MESFET Technology
- 21 – 27 dB configurable gain
- Integrated linearization
- Flexible bias voltage and current for optimum efficiency
- SOIC-16 Wide Package

General Description

The TAT8857 is a cost effective 75 Ω RFIC Amplifier designed for use in Doubler CATV applications up to 1000 MHz. It works with readily available SMT baluns and transformers to provide a highly flexible low cost replacement for traditional hybrids.

Gain of the TAT8857 may be easily adjusted by varying external components, allowing for a family of Doubler solutions to be developed from a single RFIC.

The TAT8857 provides integrated linearization to improve the 3rd order distortion performance.

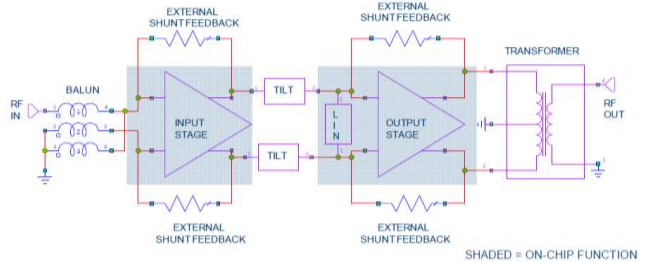
The TAT8857 may be protected against transient surges with the TQP200002 and an output high pass filter network. Consult TriQuint for discussion.

The TAT8857 supports traditional 24 V and 12 V supply voltages. Bias current may be adjusted to suit particular requirements with standard or active biasing approaches. Consult TriQuint for further discussion.



SOIC-16 Wide Package

Functional Block Diagram



Pin Configuration

Pin #	Symbol	Pin #	Symbol
1	OUT 1A	10	IN 2B
2	LIN ADJ A	11	OUT 2B
3	IN 1A	12	GATE B
4	BIAS 1A	13	GATE A
5	BIAS 1B	14	OUT 2A
6	IN 1B	15	IN 2A
7	LIN ADJ B	16	BIAS 2A
8	OUT 1B	17	GND
9	BIAS 2B		

Ordering Information

Part No.	Description
TAT8857	RFIC
TAT8857-EB	evaluation board

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{cc}		24		V
I _{cc}		350		mA

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: 25°C case temp, +24V V_{supply}

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		40		1000	MHz
Test Frequency					MHz
Gain			25		dB
Input Return Loss			18		dB
Output Return Loss			17		dB
Output P1dB at 500 MHz			31		dBm
Output IP3	See Note 1		52		dBm
CTB	See Note 2		-73		dBc
CSO	See Note 2		-74		dBc
CIN	See Note 2		60		dB
XMOD	See Note 2		-68		dBc
Noise Figure			4.0		dB
V _{bias}			24		V
I _{dd}	See Note 3		350		mA
Thermal Resistance (jnc. to case) θ_{jc}			3.4		°C/W

Notes:

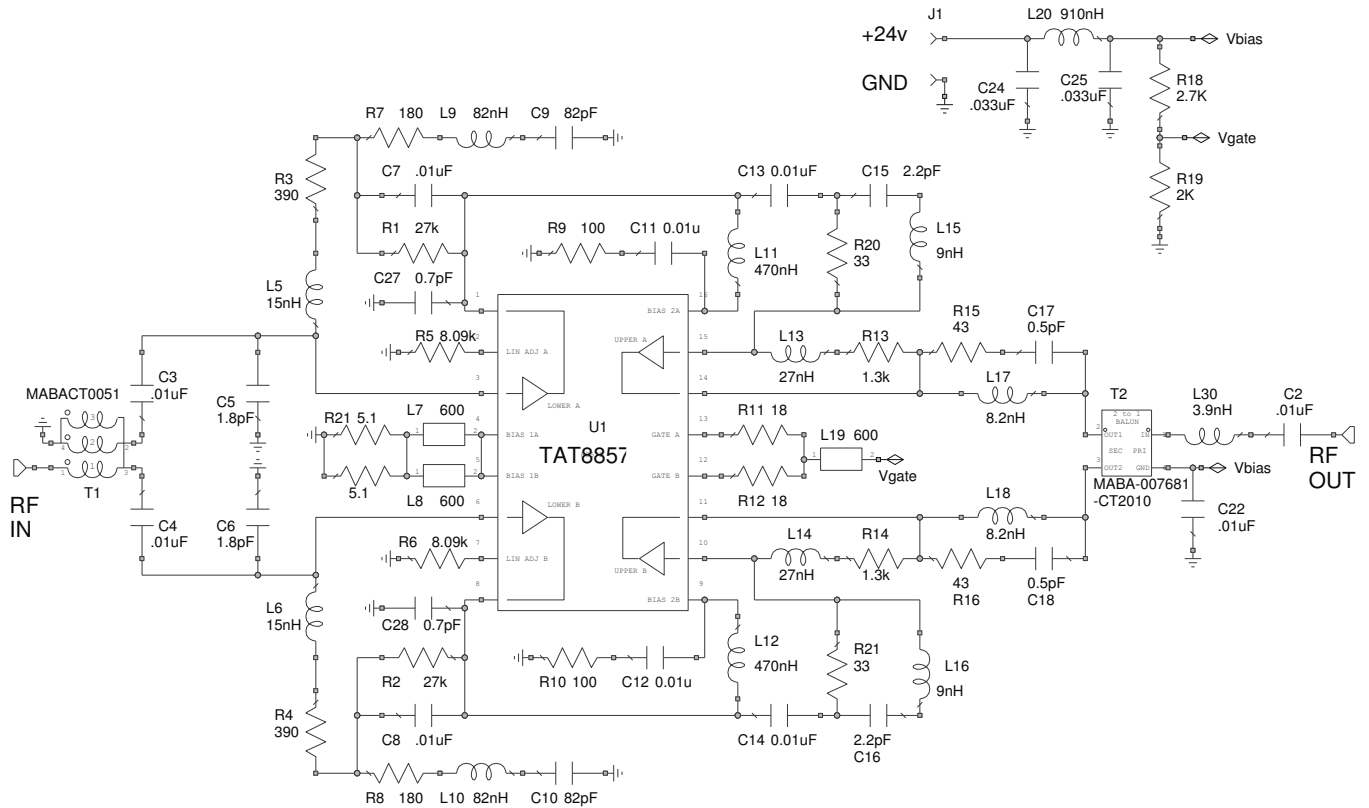
- 100 MHz tone spacing, tone 1 at 225 MHz, tone 2 at 325 MHz, low and high side intermod products.
- 79ch. NTSC + QAM (6dB offset) to 1003.25MHz, 13dB uptilt from 55.25MHz to 1003.25MHz, 40dBmV/ch at 55.25 MHz and the equivalent of 53 dBmV/ch at 1003.25 MHz.
- Active biasing is easily implemented with traditional dual-pnp approaches. Biasing at 12 V is also possible.

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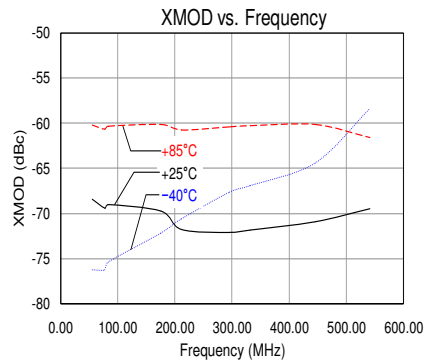
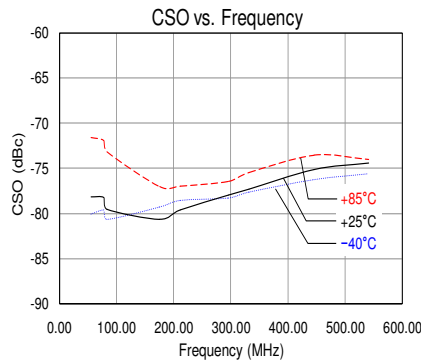
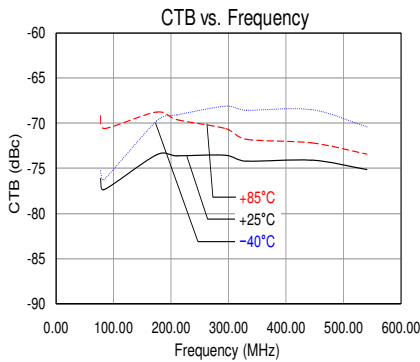
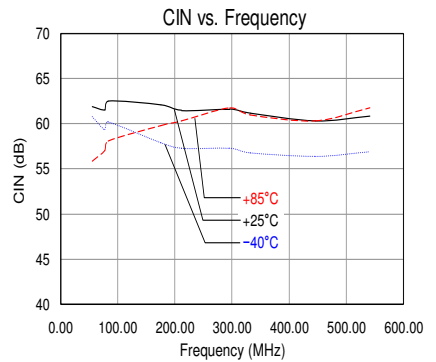
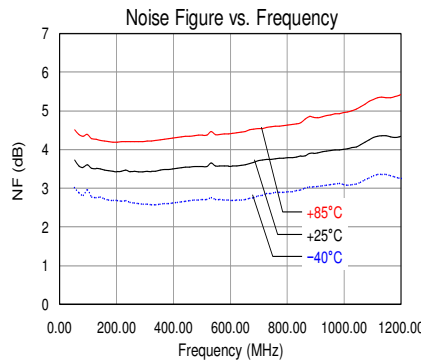
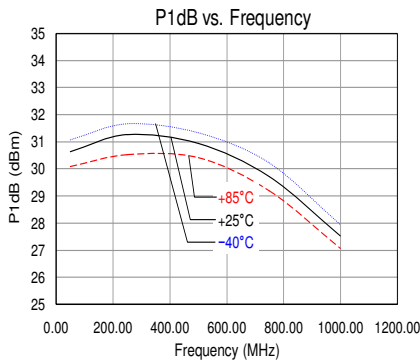
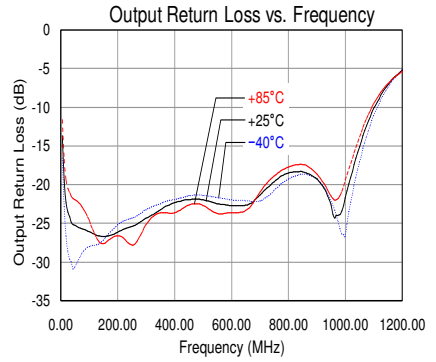
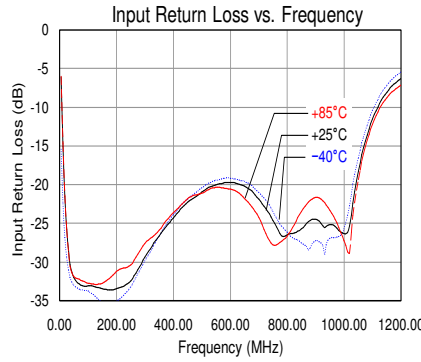
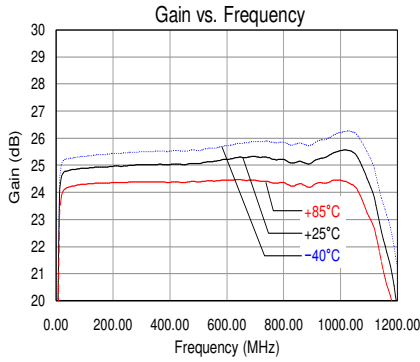
Application Circuit 40-1000 MHz



Typical Performance 40-1000 MHz

Notes:

1. 25°C case temp, 24V supply,.
2. 79ch. NTSC + QAM (6dB offset) to 1003.25MHz, 13dB uptil from 55.25MHz to 1003.25MHz, 40dBmV/ch at 55.25 MHz and the equivalent of 53 dBmV/ch at 1003.25 MHz



Detailed Device Description

The TAT8857 is similar to other parts offered on the market; it contains two separate amplifiers. A major difference is the TAT8857 allows much flexibility to set gain and bias to cover multiple applications without an additional stage. This makes it ideal for green designs. It uses a cost effective high voltage MESFET technology (designed for CATV) and a pHEMT process (developed for high-volume applications). On-chip linearization is also utilized.

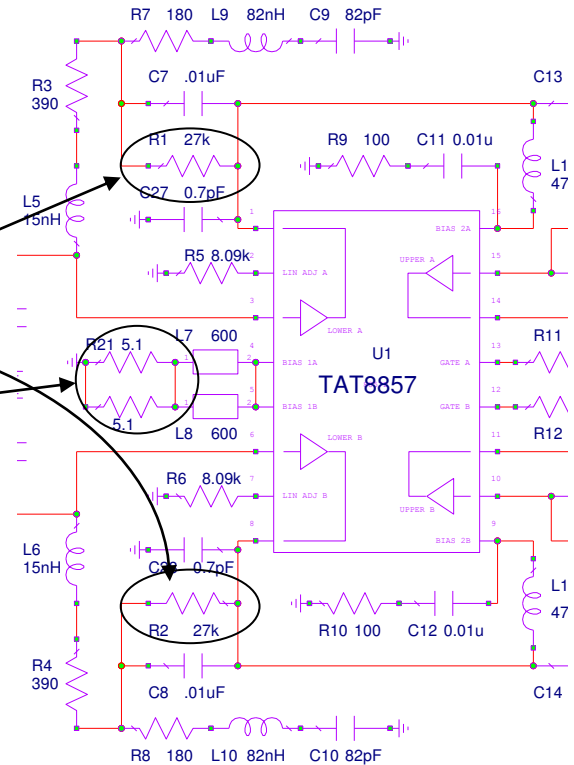
Bias Current Adjustment

Bias current is determined by 2 settings:

1. Size of DC feedback resistors - decreasing R1 & R2 will increase IDD
2. Tail resistors - decreasing R21 will increase IDD, but lead to wider variations

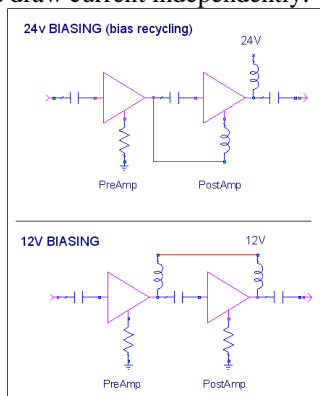
Active biasing schemes are possible but not necessary for most applications.

Best performance is with $I_{DD} = 350\text{mA}$



Voltage Biasing: 24V and 12V

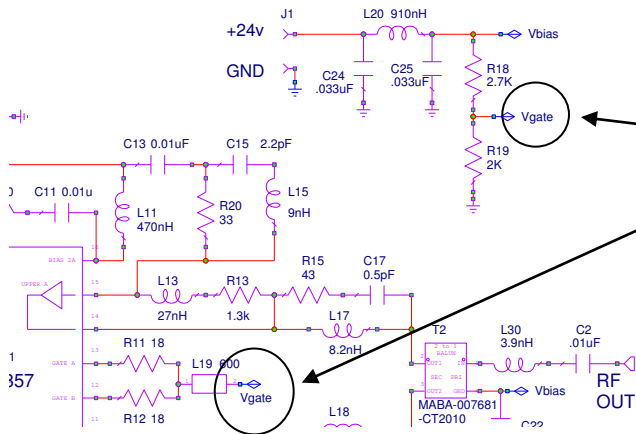
The TAT8857 has two amplifiers which can be configured to split a 24 V supply (and share the same current) or both amplifiers can be biased from a 12V supply and draw current independently.



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In the 24V case the voltage split ratio is left to the customer and is set by V_{gate} . In 24v applications, no capacitance should be put on V_{gate} ; this prevents a turn-on over-voltage condition from damaging the output FET.



Voltage divider should be done with same or lower resistor values to prevent gate leakage currents in the output FET from affecting V_{gate} .

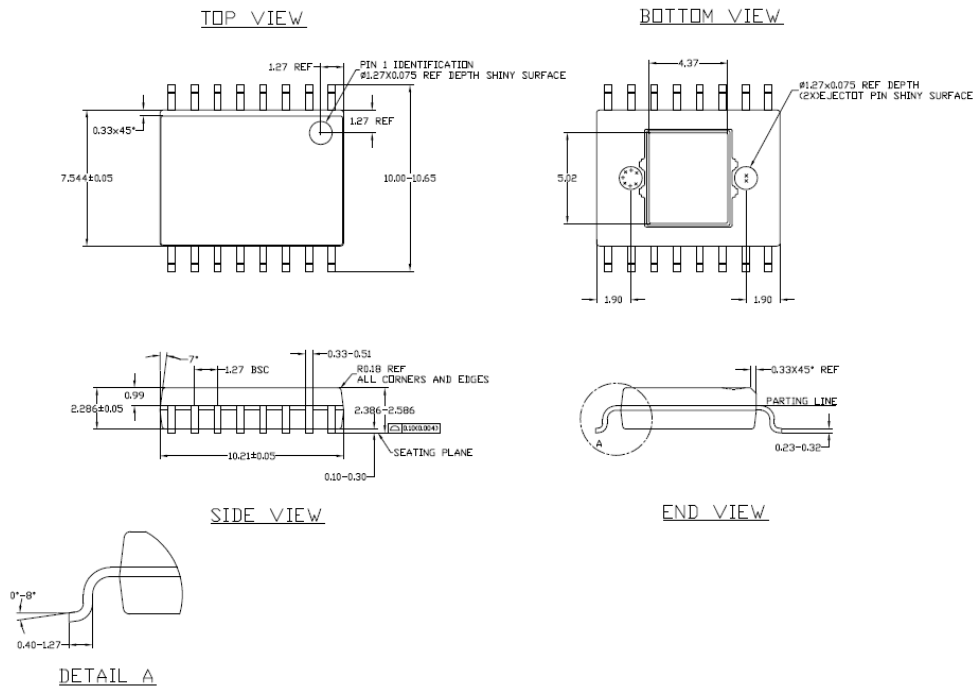
Additional information can be requested from TriQuint Applications Engineering, sjcappliations.engineering@tqs.com.

Mechanical Information

Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is 100% Matte Tin. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

The TAT8857 will be marked with an “TAT8857” designator with a lot code marked below the part designator. The “Y” represents the last digit of the year the part was manufactured, the “XXXX” is an auto-generated number and “Z” refers to a wafer number in a lot batch.



Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.

Notes:

1. A heatsink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .xxmm (#xx / .0xxx”) diameter drill and have a final plated thru diameter of .xx mm (.0xx”).
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Information



Caution! ESD-Sensitive Device

ESD Rating: Class III
Value: Passes ≥ 500 V min.
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

MSL Rating

Level 3 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level <xy> at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: sjapplications.engineering@tqs.com

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