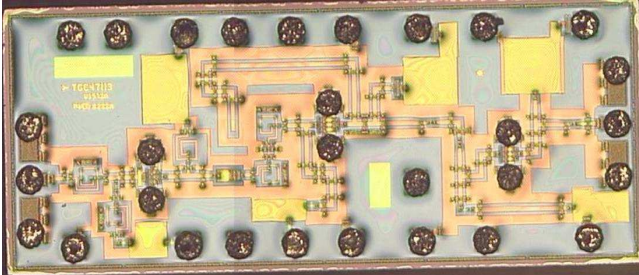
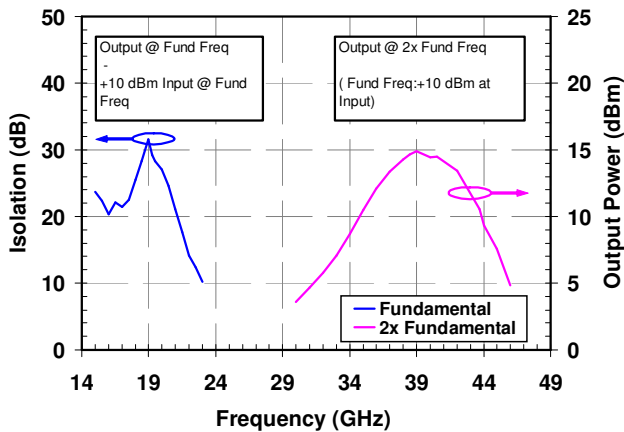
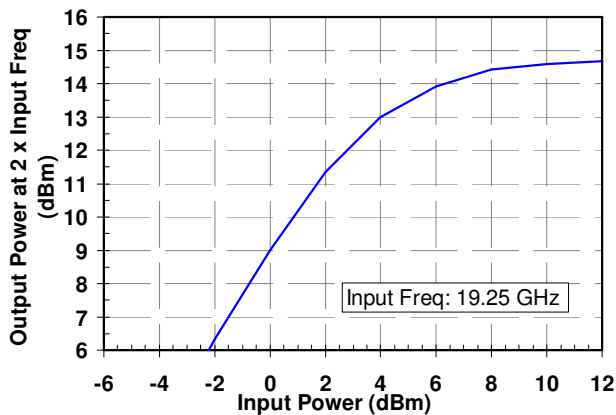


**19 to 38 GHz Doubler**



**Measured Performance**

Bias conditions:  $V_d = 3.5\text{ V}$ ,  $V_{g1} = -0.4\text{ V}$ ,  $V_{g2} = +0.2\text{ V}$ ,  
 $I_{dq} = 65\text{ mA}$  Typical



**Key Features**

- RF Output Frequency Range: 38 – 38.5 GHz
- Input Frequency Range: 19 – 19.25 GHz
- 14 dBm saturated Output Power
- 8 dB nominal Conversion Gain
- 30 dB input Frequency Isolation at output
- Input Return Loss > 15 dB
- Output Return Loss > 8 dB
- Bias:  $V_d = 3.5\text{ V}$ ,  $I_{dq} = 65\text{ mA}$ ,  $V_{g1} = -0.4\text{ V}$ ,  $V_{g2} = +0.2\text{ V}$  Typical
- Technology: 0.13  $\mu\text{m}$  pHEMT with front-side Cu/Sn pillars
- Chip Dimensions: 1.16 x 2.85 x 0.38 mm

**Primary Applications**

- Automotive Radar
- E-Band Communication

**Product Description**

The TriQuint TGC4703-FC is a flip-chip frequency doubler. It combines an input and output buffer amplifier and a frequency doubler for use in automotive radar. The TGC4703-FC is designed using TriQuint’s proven 0.13  $\mu\text{m}$  pHEMT process and front-side Cu / Sn pillar technology for simplified assembly and low interconnect inductance. Die reliability is enhanced by using TriQuint’s BCB polymeric passivation process.

The TGC4703-FC typically provides 14 dBm saturated output power with 8 dB conversion gain.

Lead-free and RoHS compliant.

**Table I**  
**Absolute Maximum Ratings <sup>1/</sup>**

Symbol	Parameter	Value	Notes
Vd-Vg	Drain to Gate Voltage	5.5 V	
Vd	Drain Voltage	4.0 V	
Vg	Gate Voltage Range	-1 to +0.45 V	
Id	Drain Current	170 mA	
Ig	Gate Current Range	-0.5 to +3.0 mA	
Pin	Input Continuous Wave Power	13 dBm	

<sup>1/</sup> These ratings represent the maximum operable values for this device. Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device and / or affect device lifetime. These are stress ratings only, and functional operation of the device at these conditions is not implied.

**Table II**  
**Recommended Operating Conditions**

Symbol	Parameter <sup>1/</sup>	Value
Vd	Drain Voltage	3.5 V
Idq	Drain Current, No RF signal at Input	65 mA
Id	Drain Current, RF signal at Input	135 mA
Vg1	Multiplier Stage Gate Voltage	-0.4 V
Vg2a, Vg2b	Amplifier Stages Gate Voltage	+0.2 V

<sup>1/</sup> See electrical schematic diagram for bias instructions.

**Table III**  
**RF Characterization Table**

**Bias: Vd = 3.5 V, Idq = 65 mA, Vg1 = -0.4 V, Vg2 = +0.2 V Typical**

<b>SYMBOL</b>	<b>PARAMETER</b>	<b>TEST CONDITIONS</b>	<b>MINIMUM</b>	<b>NOMINAL</b>	<b>UNITS</b>
IRL	Input Return Loss	Fin = 19.00 –19.25 GHz		15	dB
ORL	Output Return Loss	Fin = 38.00 – 38.50 GHz		8	dB
Pout	Output Power (RFin = 0 dBm)	Fin = 19.25 GHz Fout = 38.5 GHz	8	10.5	dBm
Pout	Output Power (RFin = 6 dBm)	Fin = 19.25 GHz Fout = 38.5 GHz	12.5	13.5	dBm
Isol	Isolation	Fin = 19.00 –19.25 GHz Fout = 19.00 –19.25 GHz		30	dB

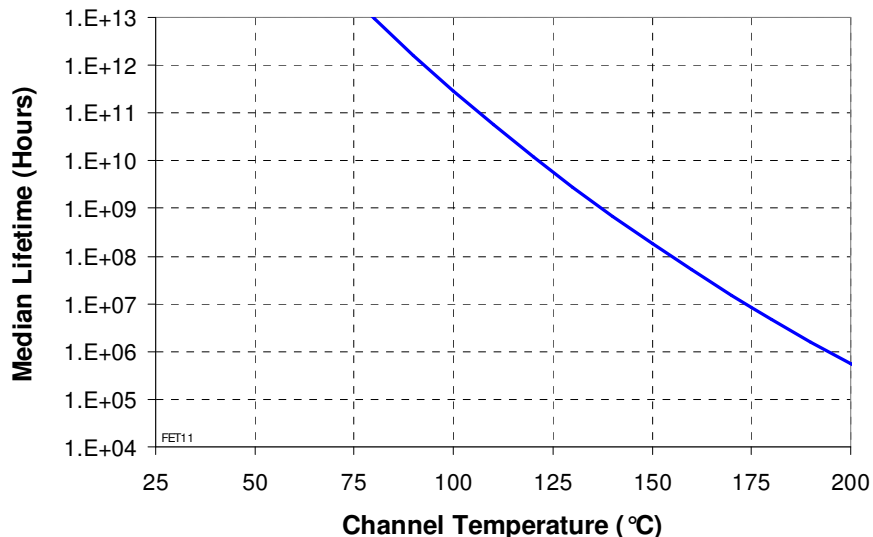
**Table IV**  
**Power Dissipation and Thermal Properties**

Parameter	Test Conditions	Value	Notes
Maximum Power Dissipation	Tbaseplate = 126.5 °C	Pd = 0.560 W Tchannel = 150 °C Tm = 2.4E+7 Hrs	<u>1/</u> <u>2/</u> <u>3/</u>
Thermal Resistance, $\theta_{jc}$	Vd = 3.5 V Vg1 = -0.4 V Vg2 = +0.2 V Id = 0.135 A Pd = 0.473 W Tbaseplate = 85 °C	$\theta_{jc}$ = 42 (°C/W) Tchannel = 104 °C Tm = 6.6E+9 Hrs	<u>3/</u>
Mounting Temperature		Refer to Solder Reflow Profiles (pp 11)	
Storage Temperature		-65 to 150 °C	

- 1/ For a median life of 2.4E+7 hours, Power Dissipation is limited to  

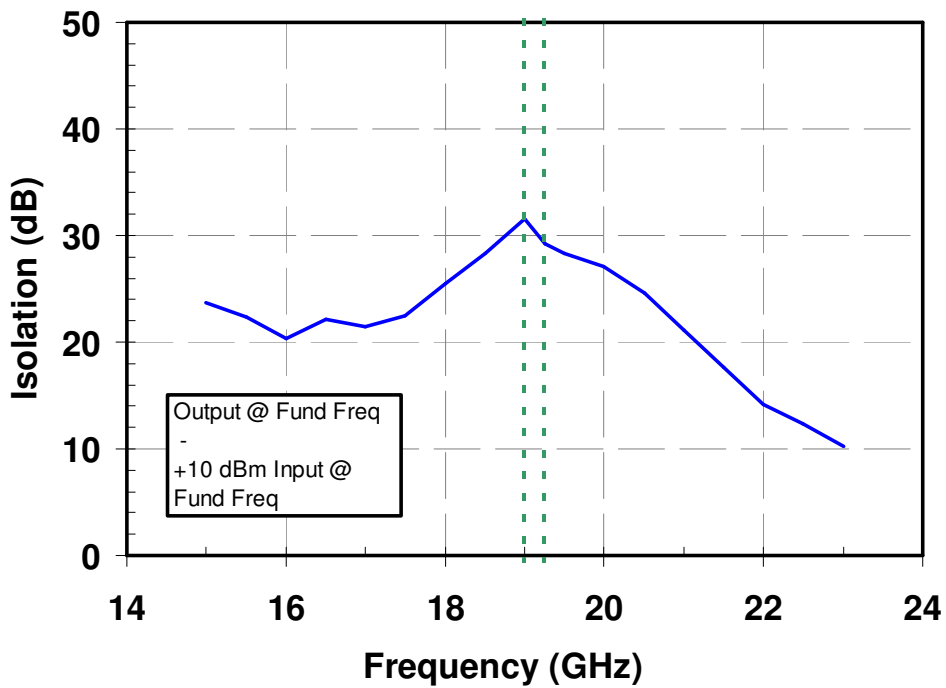
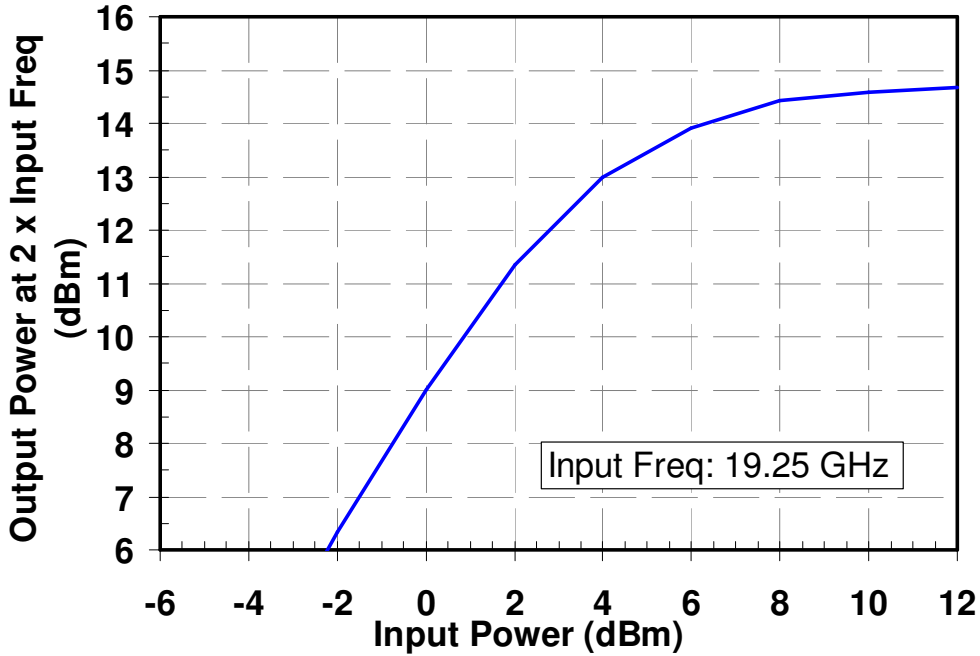
$$Pd(max) = (150\text{ °C} - Tbase\text{ °C})/\theta_{jc}.$$
- 2/ Channel operating temperature will directly affect the device median time to failure (MTTF). For maximum life, it is recommended that channel temperatures be maintained at the lowest possible levels.
- 3/ For this flip-chip die, the baseplate is a plane between the Cu/Sn pillars and the test board. For the TGC4703-FC, the critical pillars for thermal power dissipation are 24 thru 28 and 30. (See Mechanical Drawing.)

**Median Lifetime (TM) vs Channel Temperature**



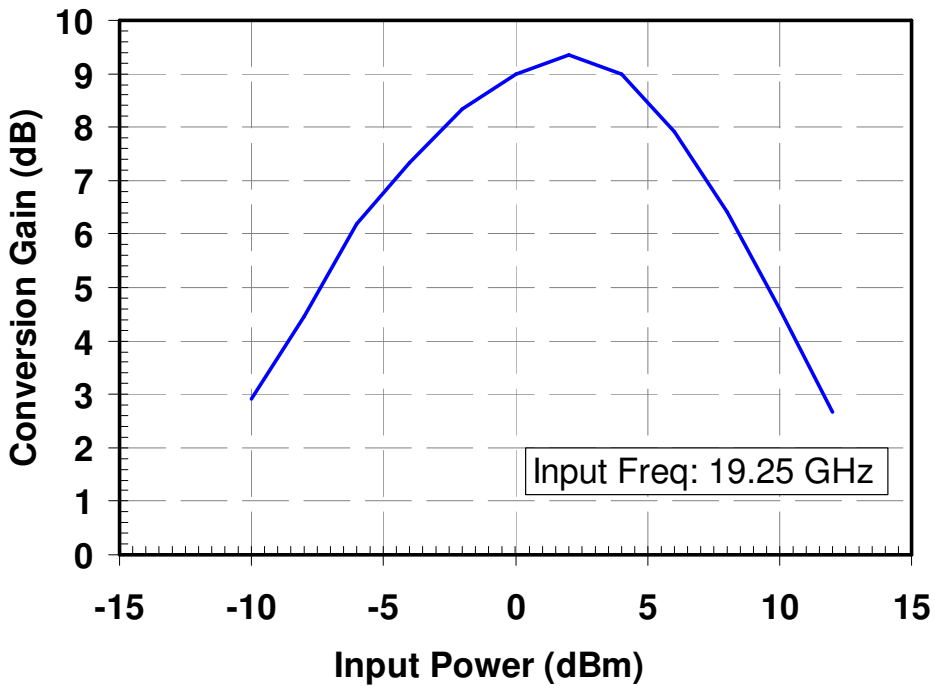
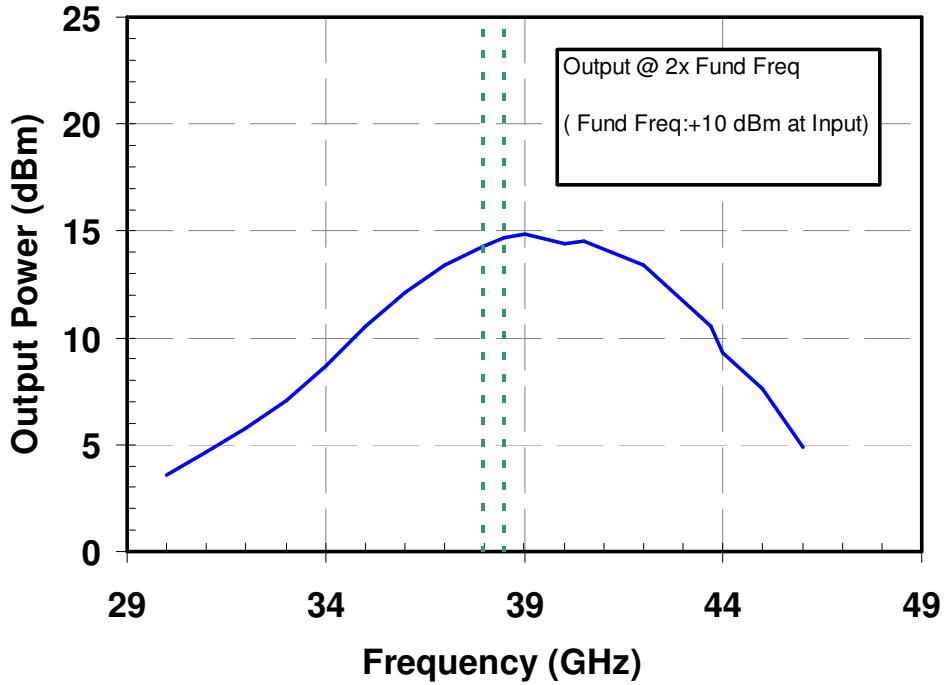
**Measured Data on Flipped Die on Carrier Board**

Bias conditions:  $V_d = 3.5\text{ V}$ ,  $I_{dq} = 65\text{ mA}$ ,  $V_{g1} = -0.4\text{ V}$ ,  $V_{g2} = +0.2\text{ V}$  Typical



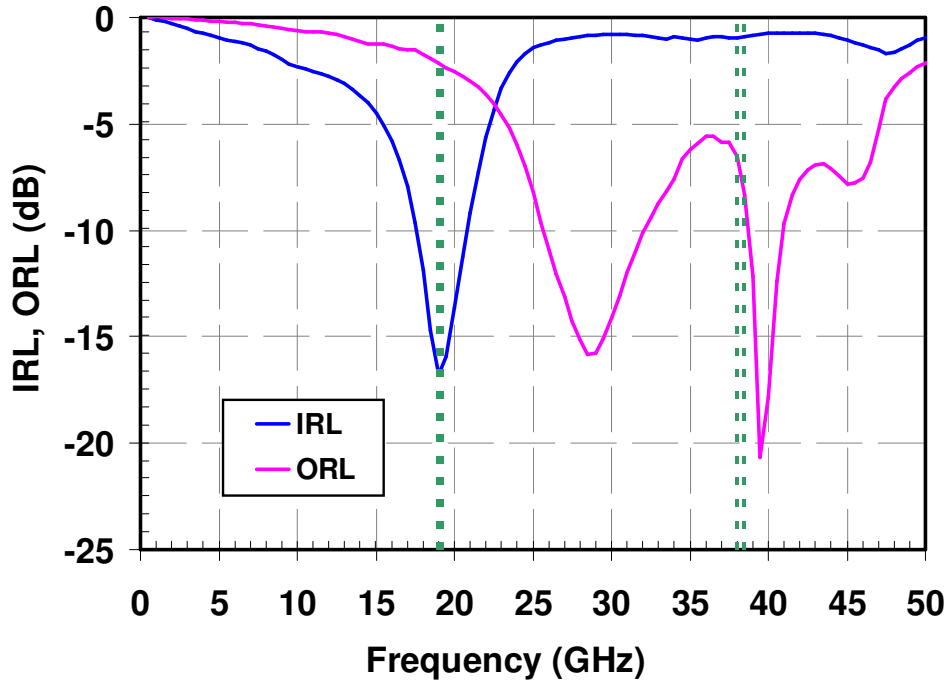
**Measured Data on Flipped Die on Carrier Board**

Bias conditions:  $V_d = 3.5\text{ V}$ ,  $I_{dq} = 65\text{ mA}$ ,  $V_{g1} = -0.4\text{ V}$ ,  $V_{g2} = +0.2\text{ V}$  Typical

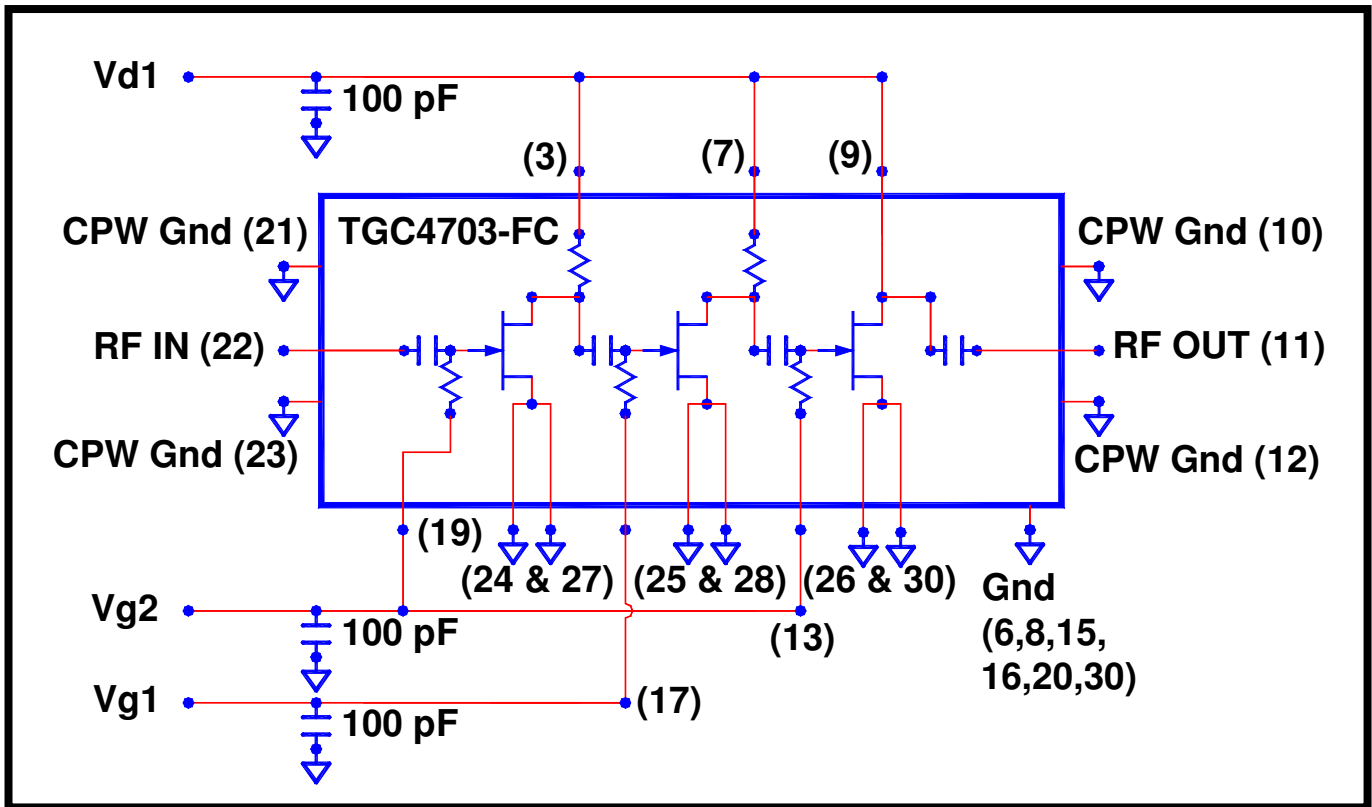


**Measured Data on Flipped Die on Carrier Board**

Bias conditions:  $V_d = 3.5$  V,  $I_{dq} = 65$  mA,  $V_{g1} = -0.4$  V  $V_{g2} = +0.2$  V Typical



**Electrical Schematic**



**Bias Procedures**

**Bias-up Procedure**

Vg1, Vg2 set to -0.4 V

Vd set to +3.5 V

Adjust Vg2 ONLY more positive until Id is 65 mA  
(Vg ~ +0.2 V)

Apply RF signal to input  
Id will be ~135 mA

**Bias-down Procedure**

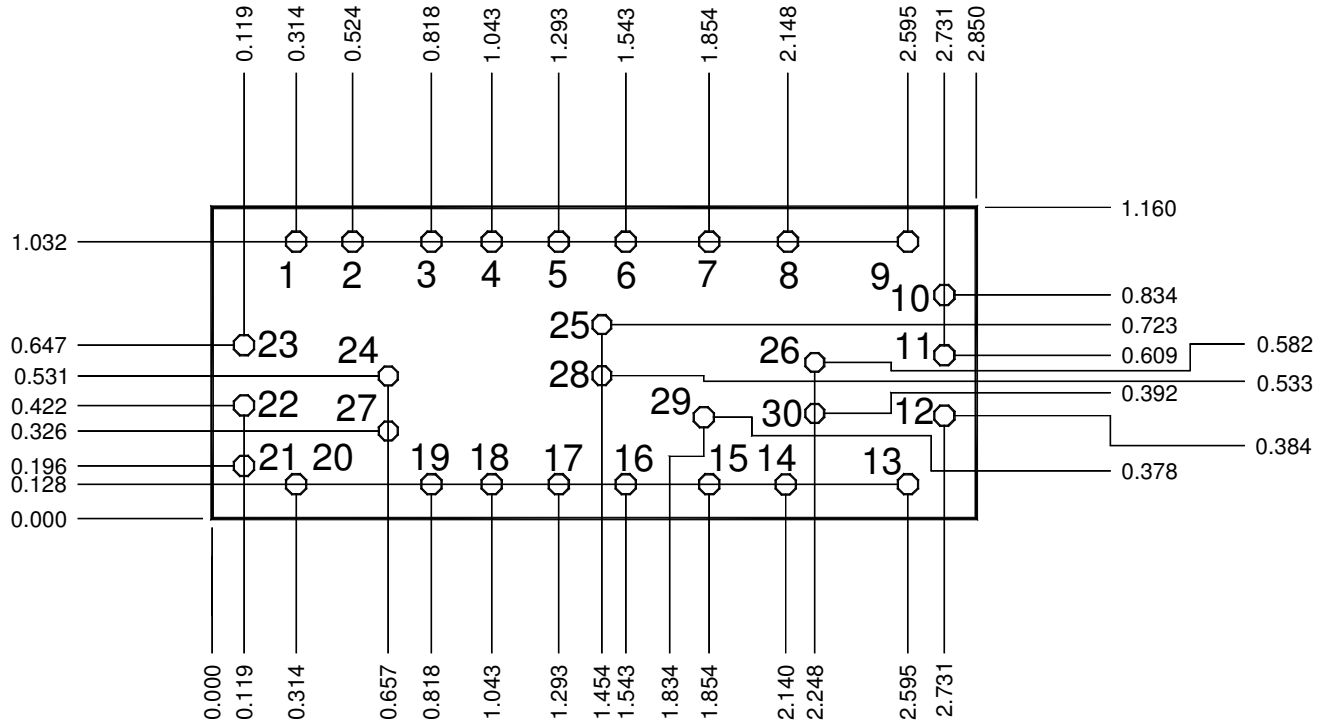
Turn off RF signal to input

Reduce Vg1, Vg2 to -0.4 V. Ensure Id ~ 0 mA

Turn Vd to 0 V



**Mechanical Drawing**  
Drawing is for chip face-up



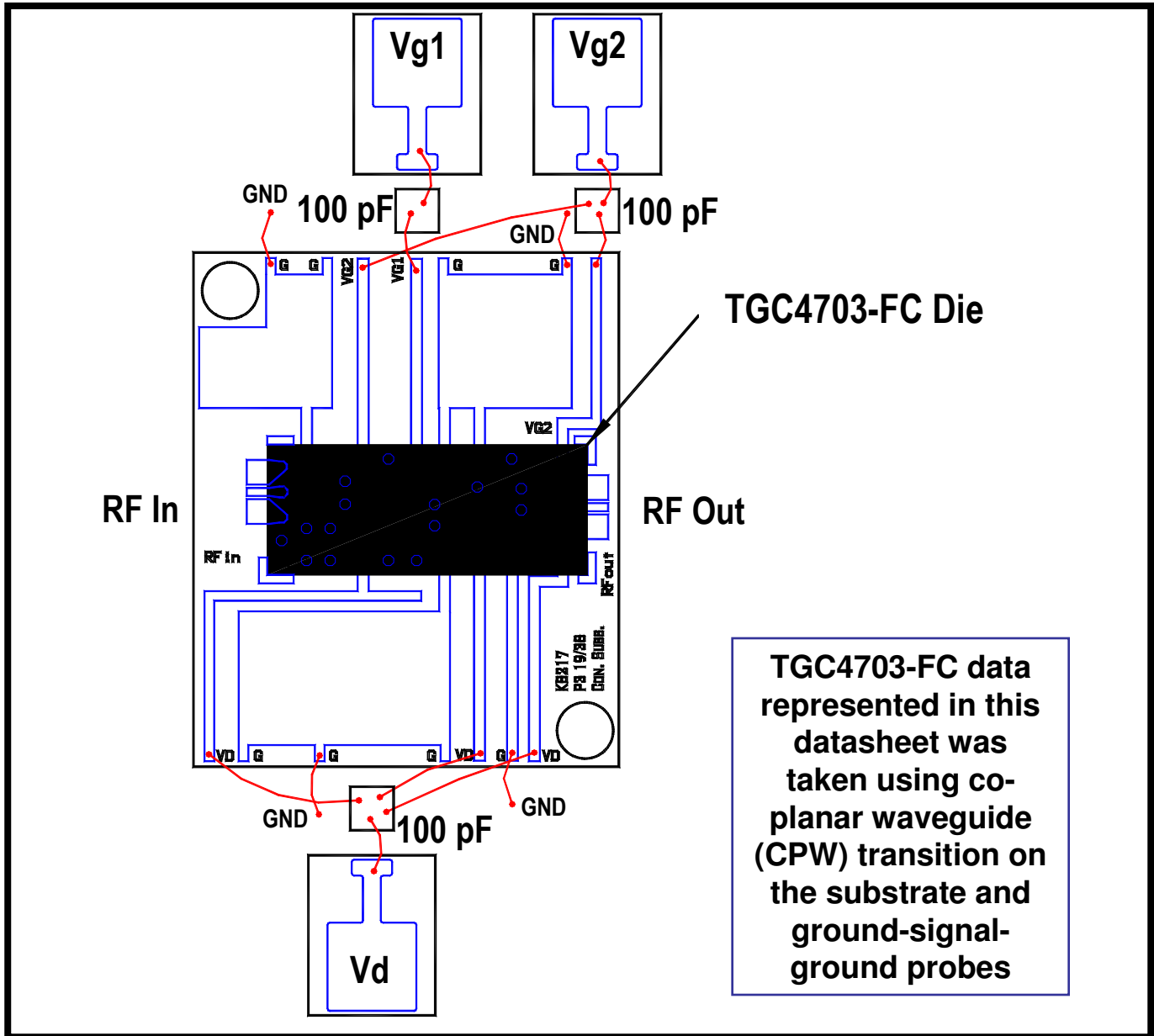
Units: millimeters Thickness: 0.380  
 Die x,y size tolerance: +/- 0.050  
 Chip edge to pillar dimensions are shown to center of pillar

Pillar #22	RF In	0.075 Ø
Pillar #11	RF Out	0.075 Ø
Pillar #10, 12, 21, 23	RF CPW Ground	0.075 Ø
Pillar #17	Vg1	0.075 Ø
Pillar #19	Vg2a	0.075 Ø
Pillar #13	Vg2b	0.075 Ø

Pillar #7	Vd1	0.075 Ø
Pillar #3	Vd2a	0.075 Ø
Pillar #9	Vd2b	0.075 Ø
Pillar #6, 8, 15, 16, 20, 24-28, 30	DC Ground	0.075 Ø
Pillar #1, 2, 4, 5, 14, 18, 29	Mech. Support Only	0.075 Ø

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

**Recommended Assembly Diagram**



Die is flip-chip soldered to a 15 mil thick alumina test substrate

**GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.**

## Assembly Notes

Component placement and die attach assembly notes:

- Vacuum pencils and/or vacuum collets are the preferred method of pick up.
- Air bridges must be avoided during placement.
- Cu pillars on die are 65 um tall with a 22 um tall Sn solder cap.
- Recommended board metallization is evaporated TiW followed by nickel/gold at pillar attach interface. Ni is the adhesion layer for the solder and the gold keeps the Ni from oxidizing. The Au should be kept to a minimum to avoid embrittlement; suggested Au / Sn mass ratio must not exceed 8%.
- Au metallization is not recommended on traces due to solder wicking and consumption concerns. If Au traces are used, a physical solder barrier must be applied or designed into the pad area of the board. The barrier must be sufficient to keep the solder from undercutting the barrier.

Reflow process assembly notes:

- Minimum alloying temperatures 245 °C.
- Repeating reflow cycles is not recommended due to Sn consumption on the first reflow cycle.
- An alloy station or conveyor furnace with an inert atmosphere such as N2 should be used.
- Dip copper pillars in “no-clean flip chip” flux prior to solder attach. Suggest using a high temperature flux. Avoid exposing entire die to flux.
- If screen printing flux, use small apertures and minimize volume of flux applied.
- Coefficient of thermal expansion matching between the MMIC and the substrate/board is critical for long-term reliability.
- Devices must be stored in a dry nitrogen atmosphere.
- Suggested reflow will depend on board material and density.

## Typical Reflow Profiles for TriQuint Cu / Sn Pillars

Process	Sn Reflow
Ramp-up Rate	3 °C/sec
Flux Activation Time and Temperature	60 – 120 sec @ 140 – 160 °C
Time above Melting Point (245 °C)	60 – 150 sec
Max Peak Temperature	300 °C
Time within 5 °C of Peak Temperature	10 – 20 sec
Ramp-down Rate	4 – 6 °C/sec

## Ordering Information

Part	Package Style
TGC4703-FC	GaAs MMIC Die

***GaAs MMIC devices are susceptible to damage from Electrostatic Discharge. Proper precautions should be observed during handling, assembly and test.***