AH322

2W High Linearity InGaP HBT Amplifier

Applications

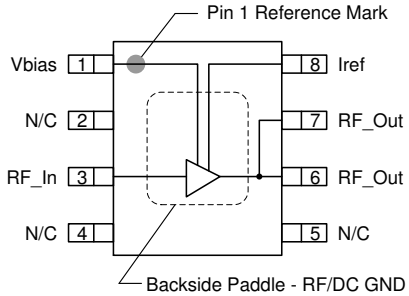
- Repeaters
- Base Station Transceivers
- High Power Amplifiers
- Mobile Infrastructure
- LTE / WCDMA / CDMA / WiMAX

SOIC-8 Package

Product Features

- 400-2700 MHz
- 13.7 dB Gain at 2140 MHz
- +33 dBm P1dB
- +50 dBm Output IP3
- 500 mA Quiescent Current
- +5 V Single Supply
- MTTF > 100 Years
- Lead-free/RoHS-compliant SOIC-8 Package

Functional Block Diagram



General Description

The AH322 is a high dynamic range driver amplifier in a low-cost surface-mount package. The InGaP/GaAs HBT is able to achieve high performance for various narrowband-tuned application circuits with up to +50 dBm OIP3 and +33 dBm of compressed 1dB power. The integrated active bias circuitry in the devices enables excellent stable linearity performance over temperature. It is housed in a lead-free/RoHS-compliant SOIC-8 package. All devices are 100% RF and DC tested.

The AH322 is targeted for use as a driver amplifier in wireless infrastructure where high linearity and medium power is required. The AH322 is ideal for the final stage of small repeaters or as driver stages for high power amplifiers. In addition, the amplifier can be used for a wide variety of other applications within the 400 to 2700 MHz frequency band.

Pin Configuration

Pin #	Symbol
1	Vbias
2, 4, 5	N/C
3	RF_in
6, 7	RF_Out
8	Iref
Backside Paddle	RF/DC GND

Not Recommended for New Designs

Recommended Replacement Part: TQP7M9104

Ordering Information

Part No.	Description
AH322-S8G	2W High Linearity Amplifier

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power, CW, 50Ω, T=25°C	+10 dBm
Device Voltage, V_{cc}, V_{bias}	+8 V
Device Current	1400 mA
Device Power	+8 W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{cc}	+4.5	+5	+5.25	V
T_{case}	-40		+85	°C
T_J (for >10^6 hours MTTF)			+200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: V_{cc} = +5 V, I_{cq} = 500 mA, T = +25°C, in a tuned application circuit.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		400		2700	MHz
Test Frequency			2140		MHz
Gain			13.7		dB
Input Return Loss			10.2		dB
Output Return Loss			14		dB
Output P1dB		+31.4	+32.6		dBm
Output IP3	See Note 1	+45	+50.0		dBm
WCDMA Channel Power at -50 dBc ACLR	See Note 2		+23.4		dBm
Noise Figure			4.7		dB
V_{cc}, V_{bias}			+5		V
Quiescent Current, I_{cq}	See Note 3	435	500	600	mA
Iref			30		mA
Thermal Resistance (jnc. to case) θ_{jc}				18.6	°C/W

Notes:
1. OIP3 measured with two tones at an output power of +24 dBm / tone separated by 1 MHz, 2140 MHz. The suppression on the largest IM3 product is used to calculate the OIP3 using a 2:1 rule.
2. 3GPP WCDMA, 1±64DPCH, ±5 MHz, no clipping, PAR = 10.2 dB at 0.01% Probability.
3. This corresponds to the quiescent collector current or operating current under small-signal conditions into pins 6 and 7.

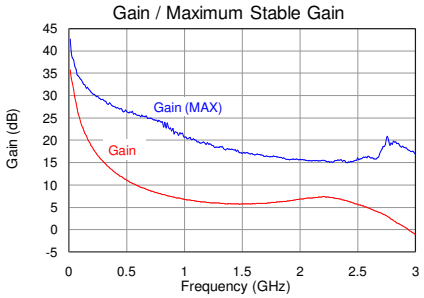
Performance Summary Table

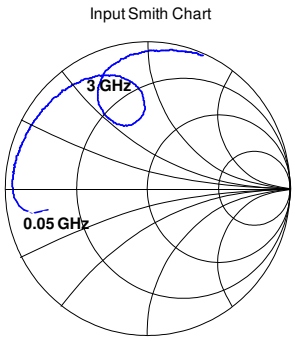
Test conditions unless otherwise noted: V_{cc} = +5 V, I_{cq} = 500 mA, T = +25°C, in an application circuit tuned for each frequency.

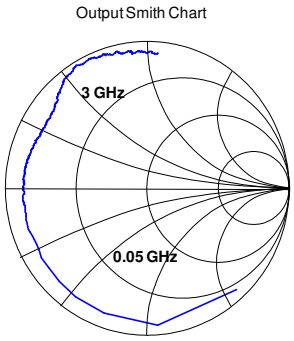
Frequency	750	940	1840	1960	2140	2655	MHz
Gain	19.2	19.3	14.6	14.1	13.7	12.6	dB
Input Return Loss	17	13	19	12.6	10.2	20	dB
Output Return Loss	10.3	7.5	11.3	10.9	14	9.3	dB
Output P1dB	+32.5	+32.8	+33.1	+33.2	+32.6	+31.9	dBm
Output IP3 [See note 1]	+46	+47.3	+49.5	+48.5	+50.0	+45.1	dBm
WCDMA Channel Power at -50 dBc ACLR	+23.1	+23.5	+24.1	+23.7	+23.4	+22.6	dBm

Notes:
1. OIP3 is measured at 21 dBm / tone separated by 1 MHz, 750 MHz, 940 MHz, 1840 MHz, 1960 MHz, and 2655 MHz. OIP3 is measured at 24 dBm / tone separated by 1 MHz, 2140 MHz.

Device Characterization Data







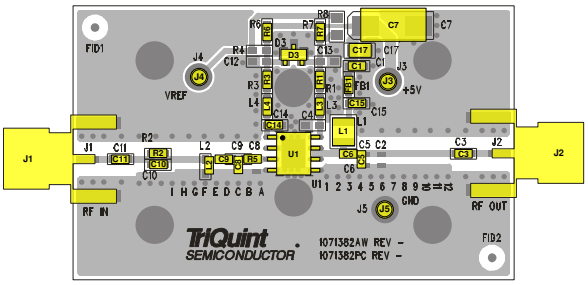
Note: The gain for the unmatched device in 50 ohm system is shown as the trace in pink color, [DB (S (2, 1)]. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the blue line [DB (GMAX)]. The impedance plots are shown from 0.05 – 3 GHz.

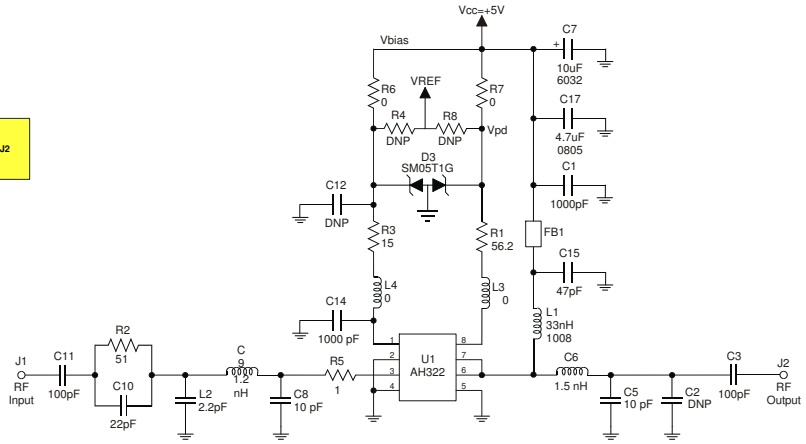
S-Parameter Data

V_{cc} = +5 V, I_{cq} = 500 mA, T = +25°C, unmatched 50 ohm system, calibrated to device leads

Freq (MHz)	S11 (dB)	S11 (ang)	S21 (dB)	S21 (ang)	S12 (dB)	S12 (ang)	S22 (dB)	S22 (ang)
50	-0.74	-174.58	29.75	109.51	-43.47	25.51	-1.15	-135.3
100	-0.53	-179.31	24.21	98.59	-43.22	17.83	-1.22	-157.31
200	-0.45	176.71	18.46	89.55	-42.49	8.135	-1.19	-170.3
400	-0.44	170.07	12.77	80.82	-42.04	5.31	-1.22	-178.39
600	-0.56	163.11	9.78	73.71	-41.41	10.52	-1.18	176.07
700	-0.61	159.9	8.73	69.49	-41.21	11.31	-1.12	173.93
800	-0.64	156.03	7.94	65.68	-40.26	12.50	-1.17	171.69
1000	-0.78	147.66	6.80	56.95	-39.65	7.88	-1.22	166.82
1200	-0.87	138.49	6.11	46.99	-38.34	2.45	-1.26	162.15
1400	-1.08	128.32	5.80	36.79	-37.99	-3.10	-1.33	157.29
1600	-1.40	117.39	5.83	25.05	-37.52	-14.57	-1.49	152.31
1800	-1.94	106.19	6.17	10.83	-37.39	-27.07	-1.46	147.31
2000	-3.20	95.90	6.80	-7.89	-37.45	-42.22	-1.41	143.05
2200	-5.84	94.01	7.36	-33.75	-38.56	-69.38	-1.21	138.40
2400	-6.52	112.96	6.50	-64.88	-41.93	-115.31	-0.9	133.24
2600	-4.45	121.06	4.77	-92.83	-41.83	167.17	-0.4	126.56
2800	-2.44	117.78	2.24	-121.06	-38.13	103.07	-0.27	119.41
3000	-1.26	108.49	-1.12	-142.85	-34.99	62.15	-0.35	112.36

700 - 800 MHz Application Circuit





Notes:

1. Vref can be used as device power down voltage (low = RF off) by swapping R7 with R8.
2. The edge of R5 is placed at 10 mils from the edge of AH322 RFin pin pad (1.5 ° @ 750 MHz)
3. The edge of C8 is placed at 10 mils from the edge of component R5 (1.5 ° @ 750 MHz).
4. The edge of C5 is placed at 170 mils from the edge of AH322 RFout pin pad (7 ° @ 750 MHz).
5. L2 is placed against the edge of C9.
6. L3 is critical for linearity performance.
7. Do not exceed +5.5V supply or TVS diode D3 will be damaged.
8. 0 Ω jumpers may be replaced with copper traces in the target application layout.
9. DNP implies Do Not Place.
10. FB1 (Ferrite Bead) prevents bias line resonances by isolating C15 and C17. Steward MI0603K300R-10.

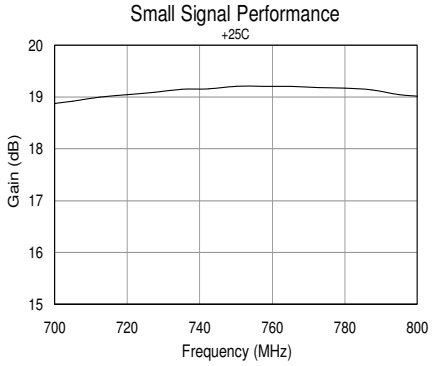
Typical Performance 700 - 800 MHz

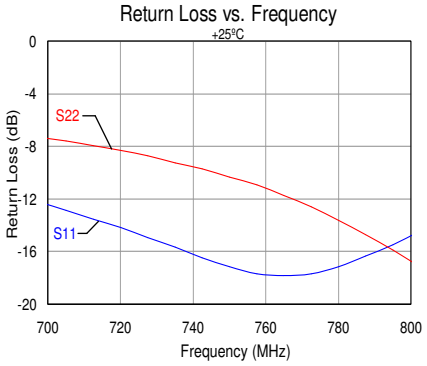
Frequency	MHz	700	750	800
Gain	dB	18.9	19.2	19
Input Return Loss	dB	12.4	17	15
Output Return Loss	dB	7.4	10.3	16.7
Output P1dB	dBm	+32	+32.5	+32
Channel Power @ 2.5% EVM [1]	dBm	+24.6	+25.2	+24.6
WCDMA Channel Power at -50 dBc ACLR [2]	dBm	+22.5	+23.1	+22.5
Output IP3(21 dBm/tone, 1 MHz spacing) [3]	dBm	+45.5	+46	+44.2
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		600	

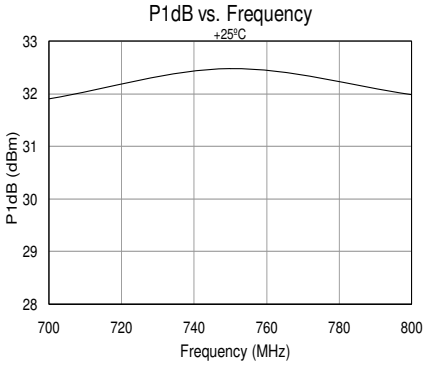
Notes:

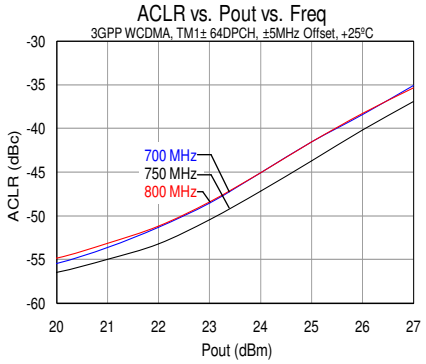
1. EVM Test set-up: 802.16 – 2004 OFDMA, 64QAM – ½, 1024 FFT, 20 symbols, 30 subchannels.
2. ACLR test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset, PAR = 10.2 dB @ 0.01% Prob.
3. OIP3 is measured at 21 dBm / tone output power with 1 MHz spacing.

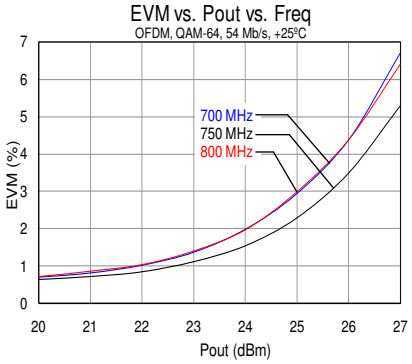
Typical Performance Plots 700 - 800 MHz

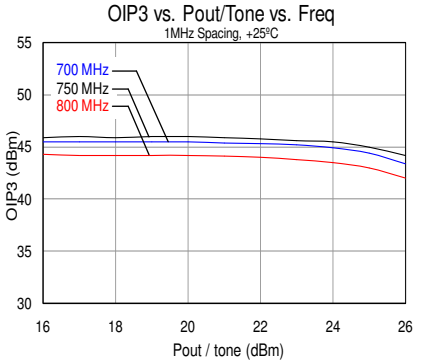




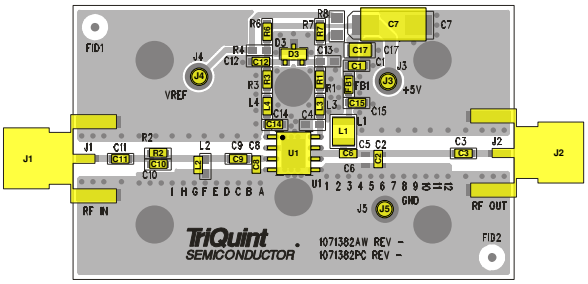


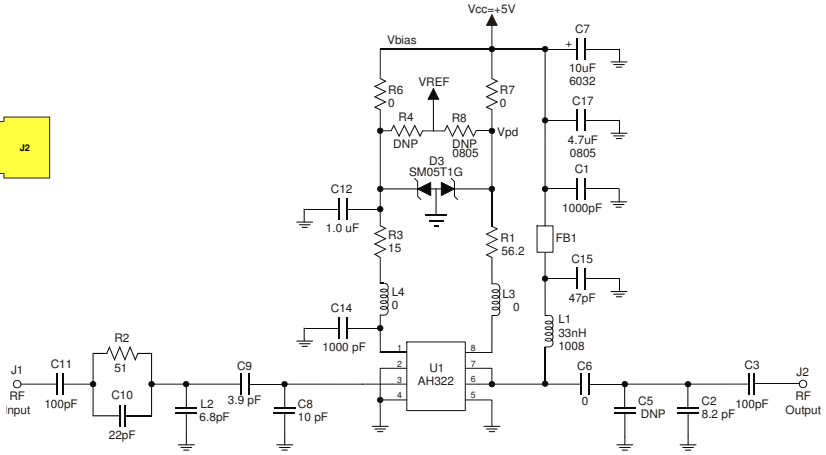






824 - 894 MHz Application Circuit





Notes:

1. Vref can be used as device power down voltage (low = RF off) by swapping R7 with R8.
2. The edge of L2 is placed at 265 mils from edge of AH322 RFout pin pad (12º @ 850 MHz).
3. The edge of C2 is placed at 250 mils from edge of AH322 RFout pin pad (11º @ 850 MHz).
4. The edge of C8 is placed at 25 mils from edge of AH322 RFout pin pad (1º @ 850 MHz).
5. L1 is critical for linearity performance.
6. Do not exceed +5.5V supply or TVS diode D3 will be damaged.
7. Zero ohm jumpers may be replaced with copper traces in the target application layout.
8. DNP implies Do Not Place.
9. FB1 (Ferrite Bead) prevents bias line resonances by isolating C15 and C1.Steward MI0603K300R-10.

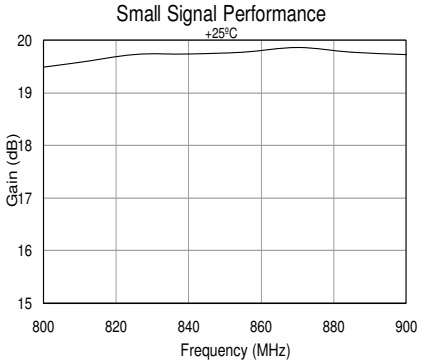
Typical Performance 824 - 894 MHz

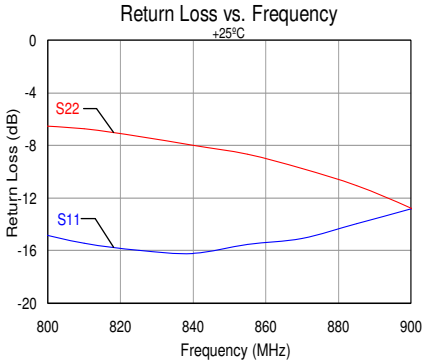
Frequency	MHz	824	848	894
Gain	dB	19.7	19.7	19.7
Input Return Loss	dB	16	16	13
Output Return Loss	dB	7	8	12
Output P1dB	dBm	+33.0	+33	+32.6
Channel Power @ 2.5% EVM [1]	dBm	+24.4	+24.4	+23.8
WCDMA Channel Power at -50 dBc ACLR [2]	dBm	+23.7	+23.7	+23
Output IP3(21 dBm/tone, 1 MHz spacing) [3]	dBm	+46.2	+46.3	+45.1
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		600	

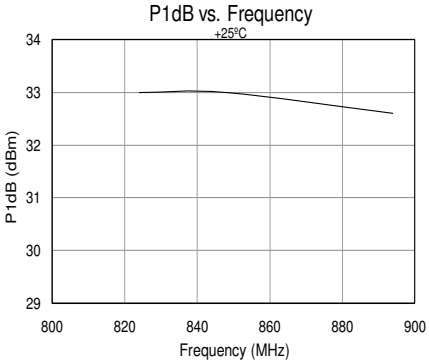
Notes:

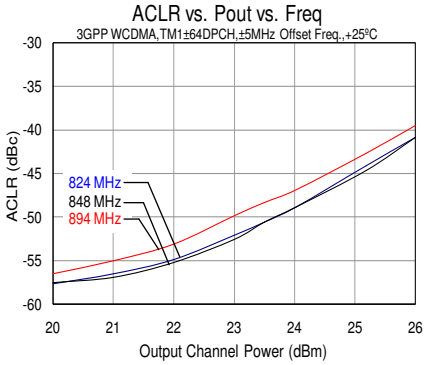
1. EVM test set-up: IS-95CDMA, 9 channels fwd, ±750KHz offset, 30KHz Meas BW, PAR=9.7 dB@ 0.01% Prob.
2. ACLR test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset, PAR = 10.34 dB @ 0.01% Prob.
3. OIP3 is measured at 21 dBm / tone output power with 1 MHz spacing.

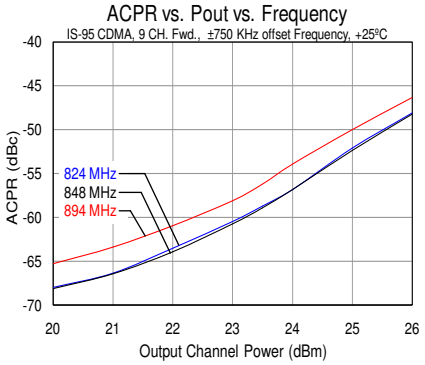
Typical Performance Plots 824 - 894 MHz

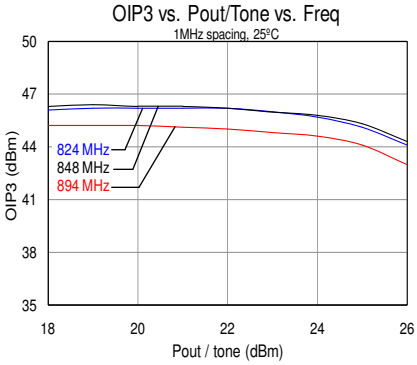




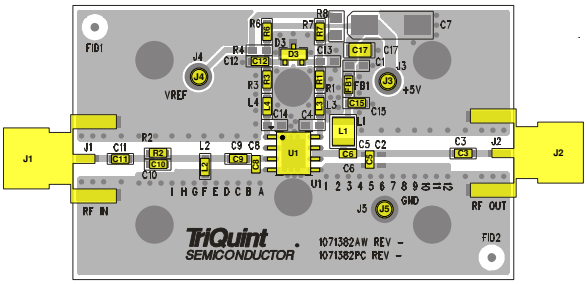


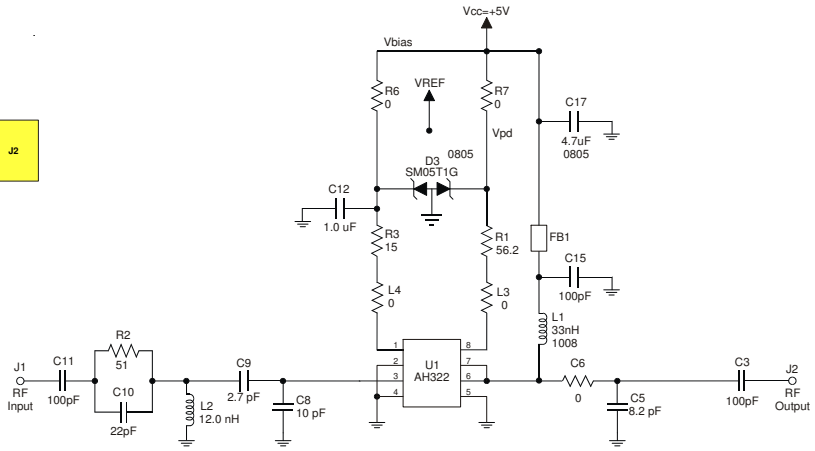






920 - 960 MHz Application Circuit (AH322-S8PCB900)





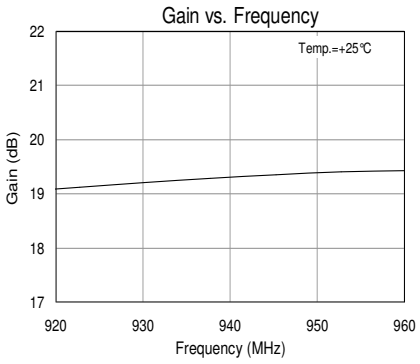
Notes:
1. Vref can be used as device power down voltage (low = RF off) by swapping R7 with R8.
2. The edge of L2 is placed at 240 mils from the edge of AH322 RFin pin pad (12 ° @ 940 MHz)
3. The edge of C9 is placed at 75 mils from the edge of AH322 RFin pin pad (3.8 ° @ 940 MHz).
4. The edge of C8 is placed at 7 mils from the edge of AH322 RFin pin pad (0.3 ° @ 940 MHz)
5. The edge of C5 is placed at 192 mils from the edge of AH322 RFout pin pad (9.6 ° @ 940 MHz).
6. L1 is critical for linearity performance.
7. Do not exceed +5.5V supply or TVS diode D3 will be damaged.
8. 0 Ω jumpers may be replaced with copper traces in the target application layout.
9. DNP implies Do Not Place.
10. FB1 (Ferrite Bead) prevents bias line resonances by isolating C15 and C17. Steward MI0603K300R-10.

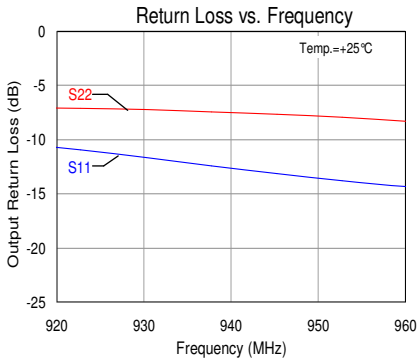
Typical Performance 920 - 960 MHz

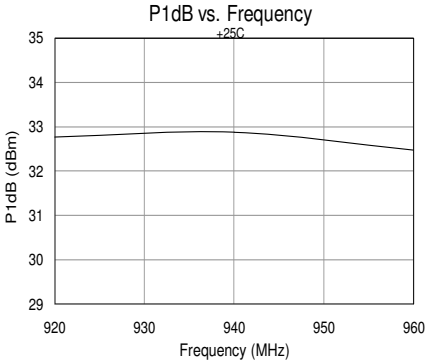
Frequency	MHz	920	940	960
Gain	dB	19.1	19.3	19.4
Input Return Loss	dB	10.6	13	14.3
Output Return Loss	dB	7.1	7.5	8.3
Output P1dB	dBm	+32.8	+32.8	+32.5
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+23.6	+23.6	+23.6
Output IP3 (21 dBm/tone, 1 MHz spacing) [2]	dBm	+47.6	+47.3	+46.9
Noise Figure	dB	7.5	7.9	8.3
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		600	

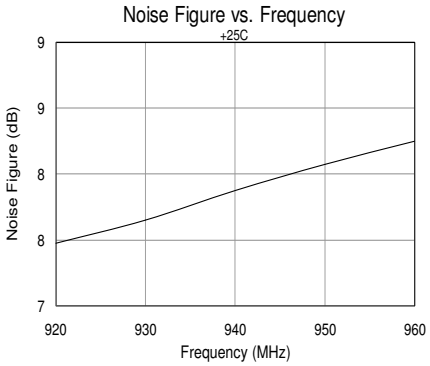
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset, PAR=10.2dB@0.01% Prob.
2. OIP3 is measured at 21 dBm / tone output power with 1 MHz spacing.

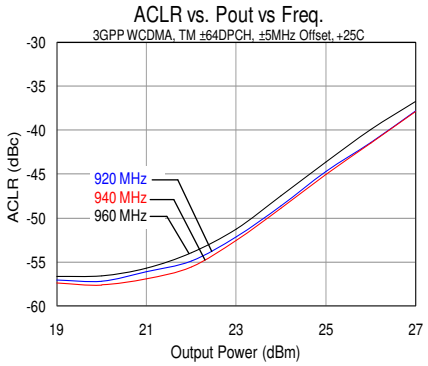
Typical Performance Plots 920 - 960 MHz

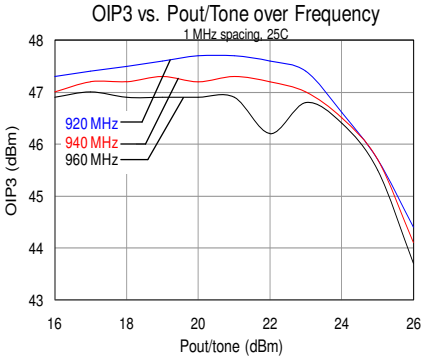




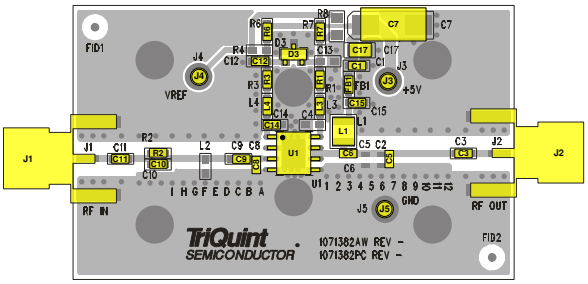


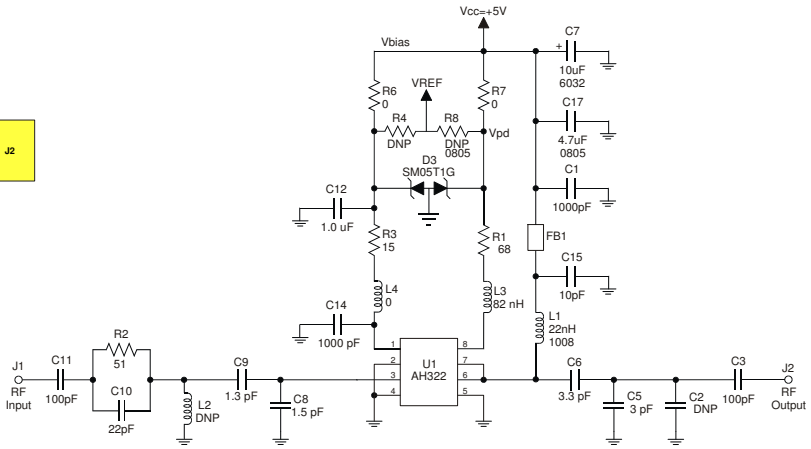






1805 - 1880 MHz Application Circuit





Notes:

1. Vref can be used as device power down voltage (low = RF off) by swapping R7 with R8.
2. The edge of C5 is placed at 315 mils from the edge of AH322 RFout pin pad (31 ° @ 1840 MHz).
3. C8 is placed against the edge of C9.
4. The multilayer inductor L3 (82nH) is critical for linearity performance.
5. Do not exceed +5.5V supply or TVS diode D3 will be damaged.
6. 0 Ω jumpers may be replaced with copper traces in the target application layout.
7. DNP implies Do Not Place.
8. FB1 (Ferrite Bead) prevents bias line resonances by isolating C15 and C1.Steward MI0603K300R-10.

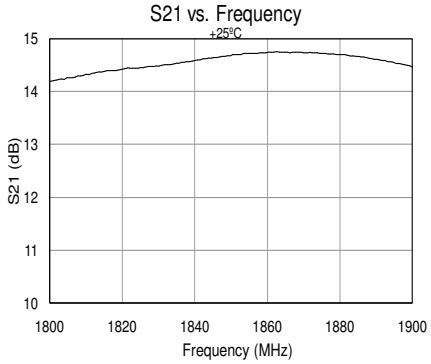
Typical Performance 1805 - 1880 MHz

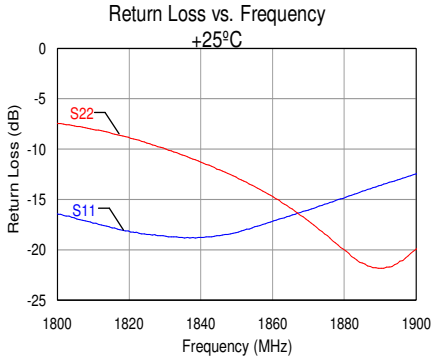
Frequency	MHz	1805	1840	1880
Gain	dB	14.3	14.6	14.7
Input Return Loss	dB	17	19	15
Output Return Loss	dB	7.7	11.3	20
Output P1dB	dBm	+33	+33.1	+32.3
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+23.2	+24.1	+22.5
Output IP3(21 dBm/tone, 1 MHz spacing) [2]	dBm	+47.9	+49.5	+44.6
Noise Figure	dB	4.9	4.9	4.9
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		500	

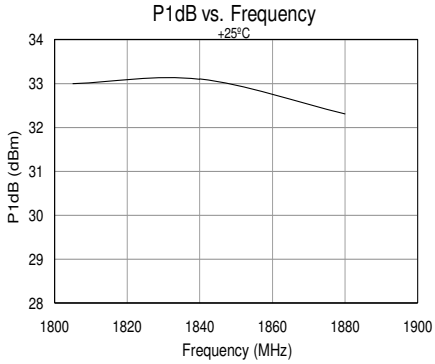
Notes:

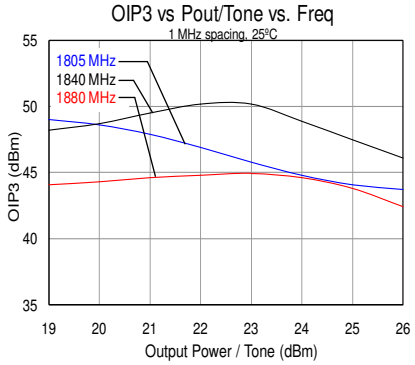
1. ACLR test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset, PAR=10.2dB @ 0.01% Prob.
2. OIP3 is measured at 21 dBm / tone output power with 1 MHz spacing.

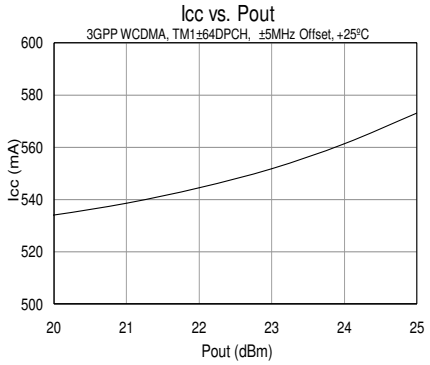
Typical Performance Plots 1805 - 1880 MHz

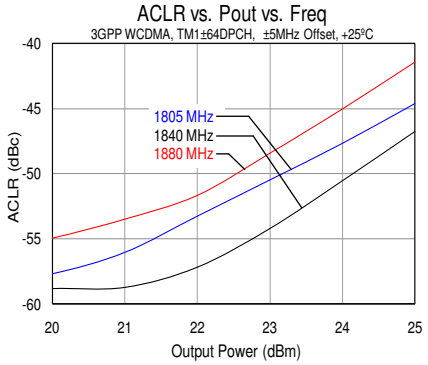




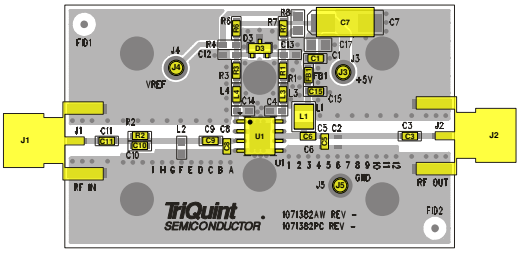


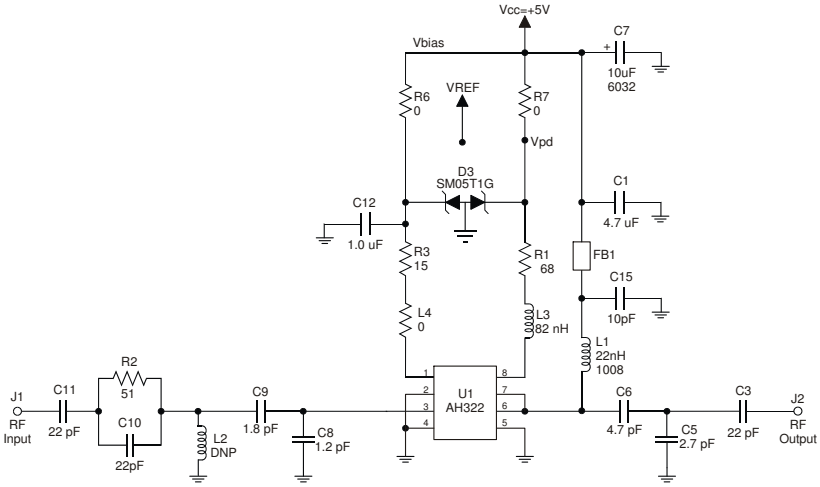






1930 - 1990 MHz Application Circuit (AH322-S8PCB1960)





Notes:

1. Vref can be used as device power down voltage (low = RF off) by swapping R7 with R8.
2. The edge of C9 is placed at 100 mils from the edge of AH322 RFin pin pad (10.5 ° @ 1960 MHz).
3. The edge of C8 is placed at 40 mils from the edge of AH322 RFin pin pad (4.2 ° @ 1960 MHz).
4. The edge of C6 is placed at 110 mils from the edge of AH322 RFout pin pad (11.5 ° @ 1960 MHz).
5. The edge of C5 is placed at 210 mils from the edge of AH322 RFout pin pad (11 ° @ 1960 MHz).
6. The multilayer inductor L3 (82nH) is critical for linearity performance.
7. Do not exceed +5.5V supply or TVS diode D3 will be damaged.
8. 0 Ω jumpers may be replaced with copper traces in the target application layout.
9. DNP implies Do Not Place.
10. FB1 (Ferrite Bead) prevents bias line resonances by isolating C15 and C1.Steward MI0603K300R-10.

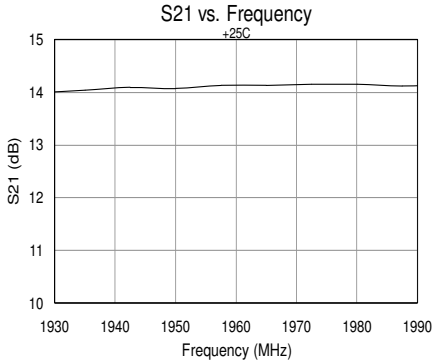
Typical Performance 1930 - 1990 MHz

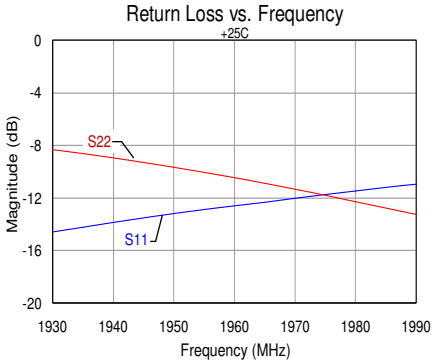
Frequency	MHz	1930	1960	1990
Gain	dB	14.0	14.1	14.1
Input Return Loss	dB	14.5	12.6	11.0
Output Return Loss	dB	8.5	10.9	13.6
Output P1dB	dBm	+33.2	+33.2	+32.9
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+23	+23.7	+23.3
Output IP3(21 dBm/tone, 1 MHz spacing) [2]	dBm	+49.0	+48.5	+46.4
Noise Figure	dB	4.6	4.6	4.6
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		500	

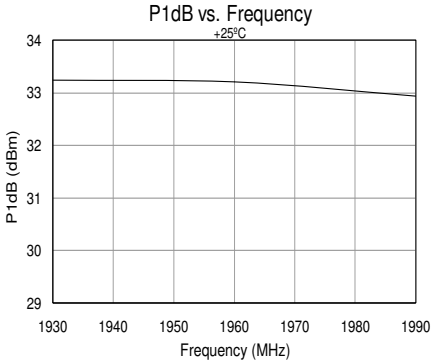
Notes:

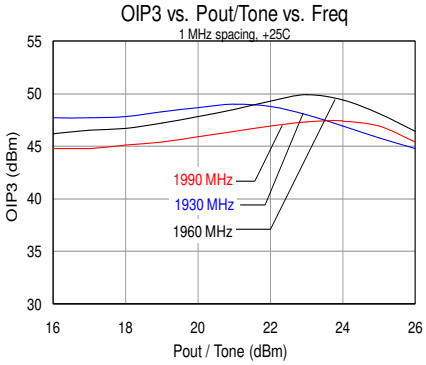
1. ACLR test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset, PAR=10.2dB @ 0.01% Prob.
2. OIP3 is measured at 21 dBm / tone output power with 1 MHz spacing.

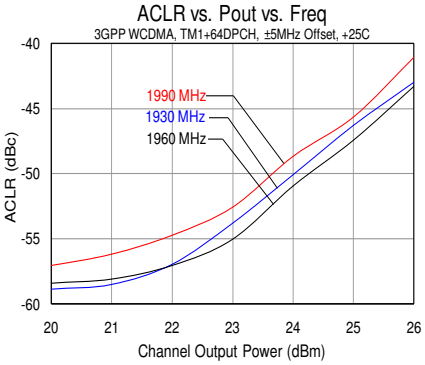
Typical Performance Plots 1930 - 1990 MHz

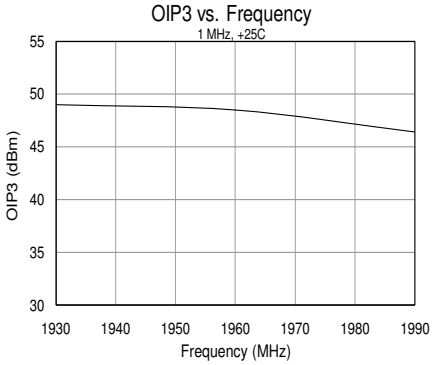




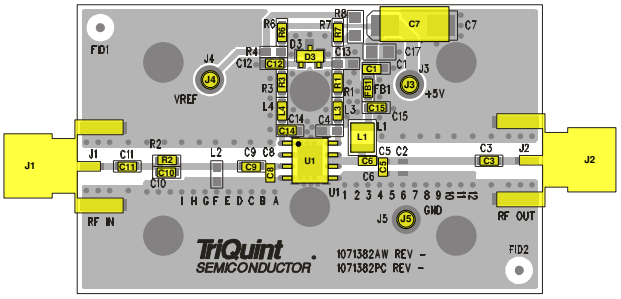


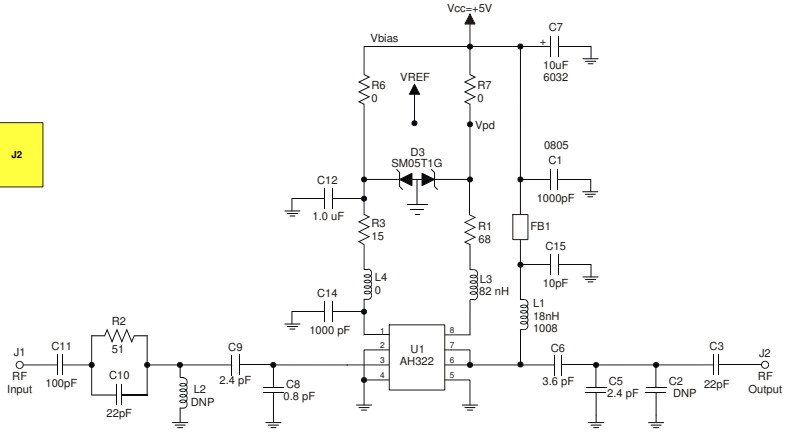






2110 - 2170 MHz Application Circuit (AH322-S8PCB2140)





Notes:

1. Vref can be used as device power down voltage (low = RF off) by swapping R7 with R8.
2. The edge of C5 is placed at 195 mils from the edge of AH322 RFout pin pad (22 ° @ 2140 MHz).
3. The edge of C8 is placed at 0.5 mils from the edge of AH322 RFin pin pad (0 ° @ 2140 MHz).
4. The edge of C9 is placed at 85 mils from the edge of AH322 RFin pin pad (9.9 ° @ 2140 MHz).
5. The multilayer inductor L3 (82 nH) is critical for linearity performance.
6. Zero ohm jumpers may be replaced with copper traces in the target application layout.
7. DNP means Do Not Place.
8. FB1 (Ferrite Bead) prevents bias line resonances by isolating C15 and C1.Steward MI0603K300R-10.

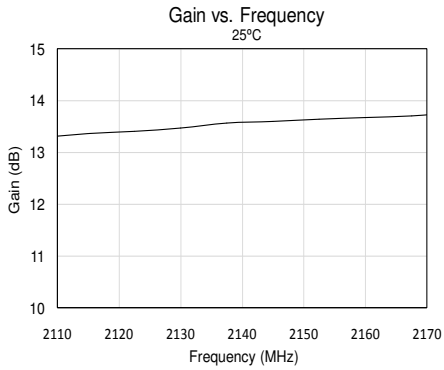
Typical Performance 2110 - 2170 MHz

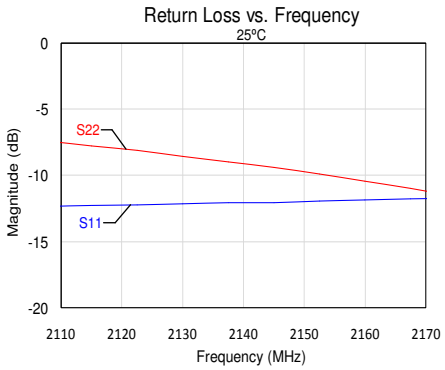
Frequency	MHz	2110	2140	2170
Gain	dB	13.6	13.7	13.7
Input Return Loss	dB	11	10.2	10
Output Return Loss	dB	11	14	17.5
Output P1dB	dBm	+32.9	+32.6	+32.5
WCDMA Channel Power at -50 dBc ACLR [1]	dBm	+23.8	+23.4	+23
Output IP3(24 dBm/tone, 1 MHz spacing) [2]	dBm	+47.9	+50	+49.8
Noise Figure	dB	4.7	4.7	4.7
Supply Voltage, Vcc	V		+5	
Quiescent Collector Current, Icq	mA		500	

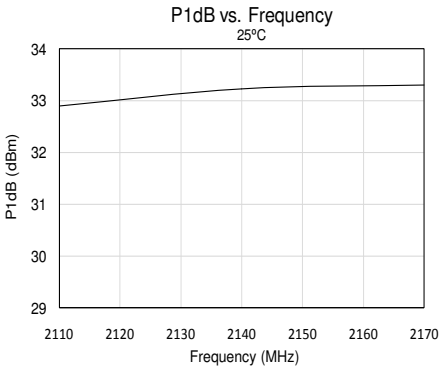
Notes:

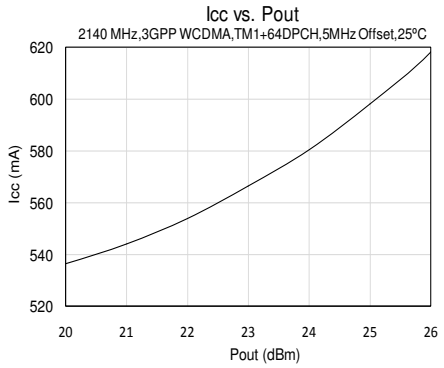
1. ACLR test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset PAR = 10.2 dB @ 0.01% Prob.
2. OIP3 is measured at 24 dBm / tone output power with 1 MHz spacing.

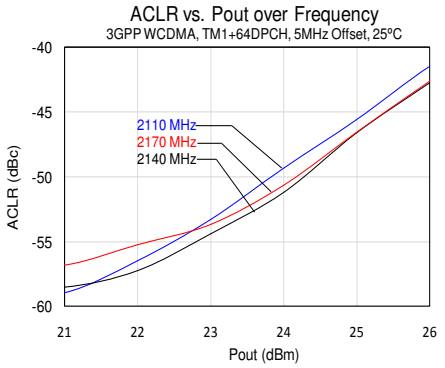
Typical Performance Plots 2110 - 2170 MHz

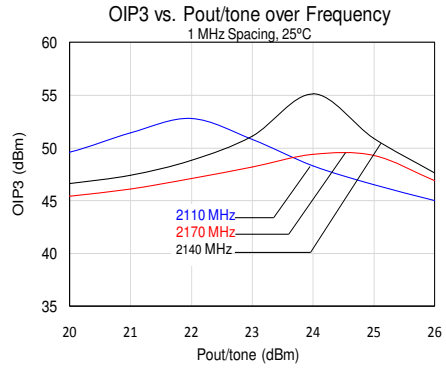




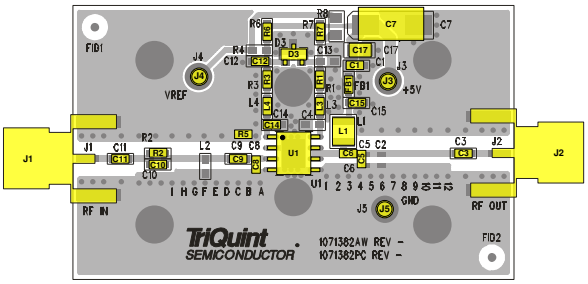


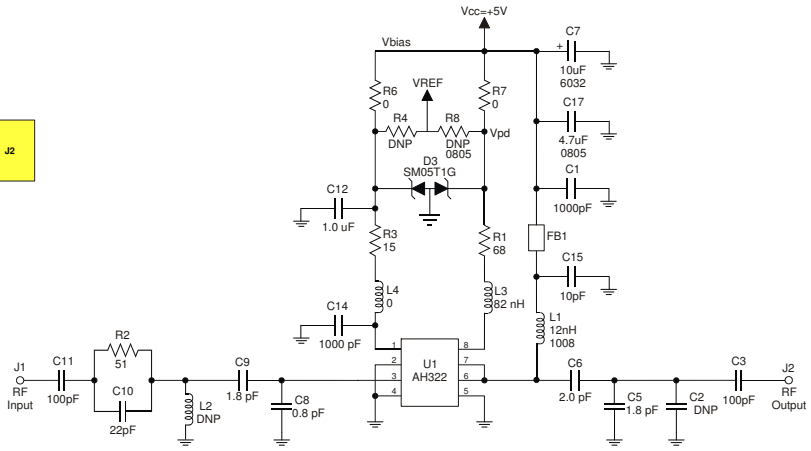






2570 - 2740 MHz Application Circuit





Notes:

1. Vref can be used as device power down voltage (low = RF off) by swapping R7 with R8.
2. The edge of C5 is placed at 160 mils from the edge of AH322 RFout pin pad (22.6 ° @ 2655 MHz).
3. The edge of C8 is placed at 0.5 mils from the edge of AH322 RFout pin pad (0 ° @ 2655 MHz).
4. The multilayer inductor L3 (82 nH) is critical for linearity performance.
5. Zero ohm jumpers may be replaced with copper traces in the target application layout.
6. DNP means Do Not Place.
7. FB1 (Ferrite Bead) prevents bias line resonances by isolating C15 and C1.Steward MI0603K300R-10.

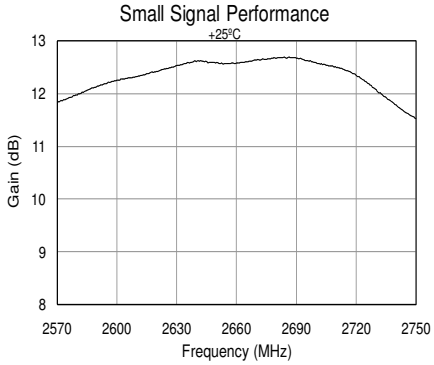
Typical Performance 2570 - 2740 MHz

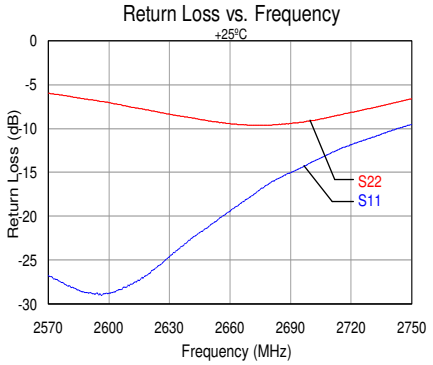
Frequency	MHz	2570	2655	2740
Gain	dB	11.8	12.6	11.8
Input Return Loss	dB	26.7	20	10.2
Output Return Loss	dB	6	9.3	7
Output P1dB	dBm	+31.7	+31.9	+30.4
Channel Power @ 2.5% EVM [1]	dBm	+23.9	+24.5	+23
WCDMA Channel Power at -50 dBc ACLR [2]	dBm	+21.6	+22.6	+21
Output IP3(21 dBm/tone, 1 MHz spacing) [3]	dBm	+44.4	+45.1	+43.3
Noise Figure	dB	5.9	6.2	6.7
Supply Voltage, Vcc	V	+5		
Quiescent Collector Current, Icq	mA	500		

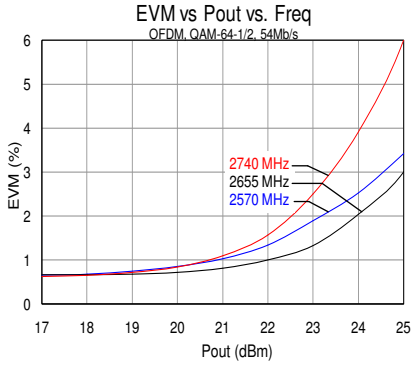
Notes:

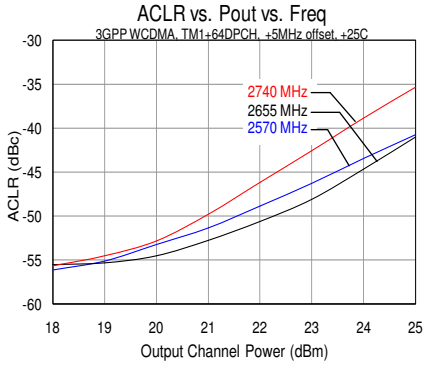
1. EVM Test set-up: 802.16 – 2004 OFDMA, 64QAM – ½, 1024 FFT, 20 symbols, 30 subchannels.
2. ACLR Test set-up: 3GPP WCDMA, TM1±64 DPCH, ±5MHz offset PAR = 10.2 dB @ 0.01% Prob.
3. OIP3 is measured at 21 dBm / tone output power with 1 MHz spacing.

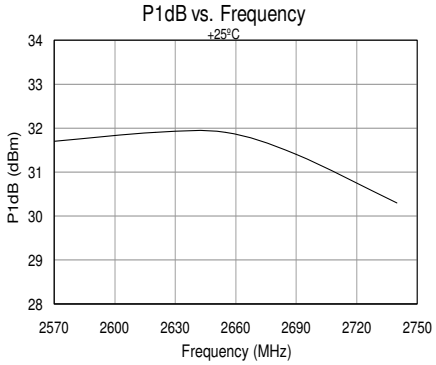
Typical Performance Plots 2570 - 2740 MHz

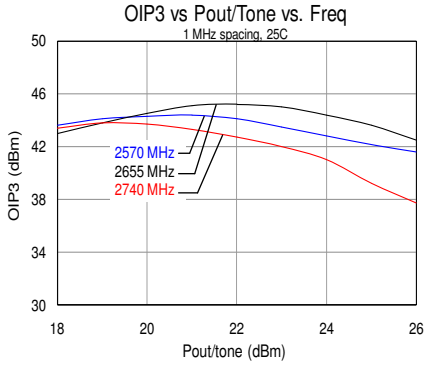




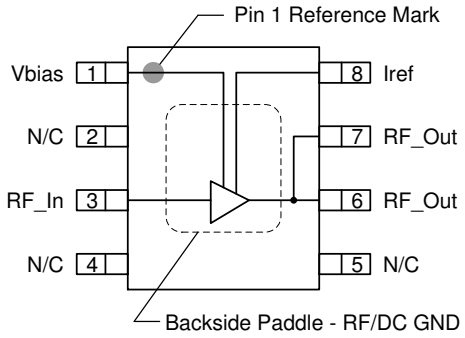








Pin Description



Pin	Symbol	Description
1	Vbias	Voltage supply for active bias. Connect to same supply voltage as Vcc.
2, 4, 5	N/C	No internal connection. This pin can be grounded or N/C on PCB.
3	RF_in	RF Input. Requires matching for operation.
6	RF_out	RF Output and DC supply voltage.
7	RF_out	See pin 6.
8	Iref	Reference current into internal active bias current mirror. Current into Iref sets device quiescent current. Also, can be used as on/off control.
Backside Paddle	RF/DC GND	Use recommended via pattern shown on page 20 and ensure good solder attach for optimum thermal and electrical performance.

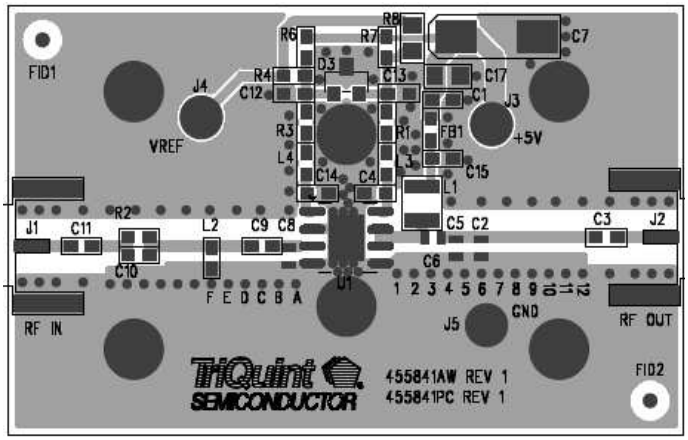
Application Board Information

PC Board Layout

Top RF layer is .014" Getek, ϵ_r = 4.0, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line details: width = .030", spacing = .026".

The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitors – C8, C5 and C2. The markers and vias are spaced in .050" increments.

The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.



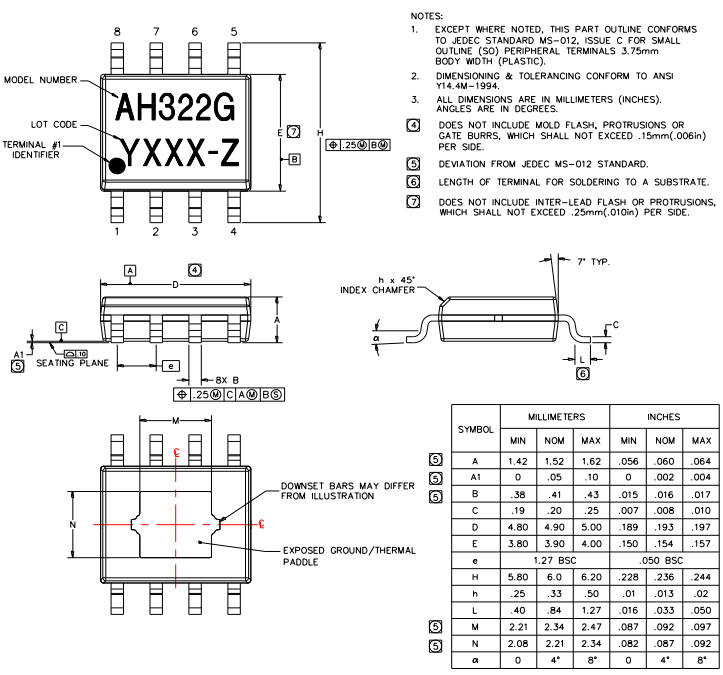
For further technical information, Refer to www.TriQuint.com

Mechanical Information

Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is NiPdAu. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

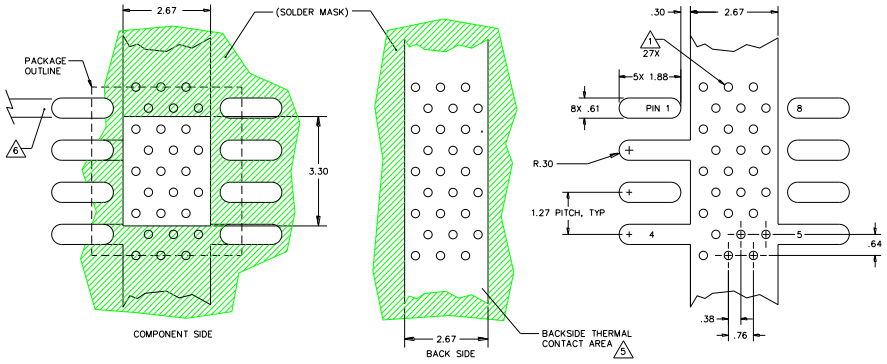
The AH225 will be marked with an "AH322G" designator with a lot code marked below the part designator. The "Y" represents the last digit of the year the part was manufactured, the "XXXX" is an auto-generated number, and "Z" refers to a wafer number in a lot batch.



NOTES:
1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MS-012, ISSUE C FOR SMALL OUTLINE (SO) PERIPHERAL TERMINALS 3.75mm BODY WIDTH (PLASTIC).
2. DIMENSIONING & TOLERANCING CONFORM TO ANSI Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS (INCHES). ANGLES ARE IN DEGREES.
4. DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS, WHICH SHALL NOT EXCEED .15mm(.006in) PER SIDE.
5. DEVIATION FROM JEDEC MS-012 STANDARD.
6. LENGTH OF TERMINAL FOR SOLDERING TO A SUBSTRATE.
7. DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSIONS, WHICH SHALL NOT EXCEED .25mm(.010in) PER SIDE.

SYMBOL	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.42	1.52	1.62	.056	.060	.064
A1	0	.05	.10	0	.002	.004
B	.38	.41	.43	.015	.016	.017
C	.19	.20	.25	.007	.008	.010
D	4.80	4.90	5.00	.189	.193	.197
E	3.80	3.90	4.00	.150	.154	.157
e	1.27 BSC			.050 BSC		
H	5.80	6.0	6.20	.228	.236	.244
h	.25	.33	.50	.01	.013	.02
L	.40	.84	1.27	.016	.033	.050
M	2.21	2.34	2.47	.087	.092	.097
N	2.08	2.21	2.34	.082	.087	.092
α	0	4°	8°	0	4°	8°

Mounting Configuration



Notes:
1. A heat sink underneath the area of the PCB for the mounted device is strictly required for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010") or equivalent.
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heat sink. Ensure that the ground / thermal via region contact the heat sink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heat sink.
6. RF Trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters (inches). Angles are in degrees.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1C
Value:	Passes ≥ 1000 V to < 2000V.
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22A114

ESD Rating:	Class IV
Value:	Passes ≥ 1000 V min.
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22C101

MSL Rating

The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°.

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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