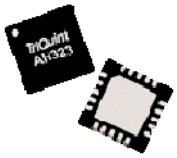
AH323

2W High Linearity 5V 2-Stage Amplifier

Applications

- Base stations / Repeaters
- High Power Amplifiers
- 2G / 3G / 4G Wireless Infrastructure
- Femtocells
- LTE / WCDMA / CDMA / EDGE

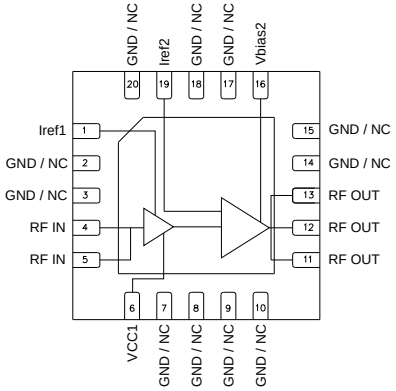


20-pin 5x5mm leadless QFN package

Product Features

- 700-2700 MHz
- 27.2 dB Gain @ 2.14 GHz
- +33 dBm P1dB
- High linearity: +50 dBm OIP3
- 24 dBm Output Power @ -50 dBc WCDMA ACLR
- Integrated interstage matching
- Excellent return loss (>14 dB at I/O)
- +5V Supply Voltage
- MTTF > 1000 Years

Functional Block Diagram



General Description

The AH323 is a high dynamic range two-stage driver amplifier in a low-cost surface-mount package. The amplifier is able to achieve high performance across a broad range of frequencies with +50 dBm OIP3 and +33 dBm P1dB while only consuming 680 mA current. The InGaP/GaAs HBT integrates two high performance amplifier stages onto a MMIC to allow for a more compact system design. The integrated interstage match minimizes performance variation that would otherwise be attributed to external matching component value and placement tolerances. The AH323 is available in a standard lead-free /green/RoHS-compliant 20-pin 5x5mm QFN package. All devices are 100% RF and DC tested.

The AH323 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. This driver amplifier is able to deliver high power while maintaining superior ACLR performance. The integrated active bias circuitry in the devices enable excellent linearity performance over temperature with little variance.

The AH323 is footprint compatible with other TriQuint 2W devices such as the AH314 for 2.3-2.9GHz applications and the AH315 for 3.3-3.8GHz applications.

Pin Configuration

Pin #	Symbol
6	Vcc1
1	Iref1
19	Iref2
4,5	RF Input
11,12,13	RFout / Vcc2
16	Vbias2
Backside Paddle	GND
2,3,7,8,9,10,14,15,17,18,20	N/C or GND

Ordering Information

Part No.	Description
AH323-G	2W 5V 2-stage Amplifier
AH323-PCB2140	2140 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power, CW, 50Ω,T = 25°C	+18 dBm
Device Voltage,Vcc	+8 V
Device Current	1900 mA
Power Dissipation	8 W
Thermal Resistance (jnc. to case) θ_{jc}	11.7 °C/W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
Vcc		+5	+6	V
Tcase	-40		+85	°C
T_J (for >10^6 hours MTTF)			+200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

Electrical Specifications

Test conditions unless otherwise noted: +25°C, +5V Vcc, 2140 MHz, in a tuned application circuit.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		700		2700	MHz
Test Frequency			2140		MHz
Gain		24.2	27.2		dB
Input Return Loss			25		dB
Output Return Loss			17		dB
Output P1dB		+32.4	+33.1		dBm
Output IP3	See Note 1.	+44.5	+50		dBm
WCDMA Channel Power @ -50 dBc ACLR	See Note 2.		+23.9		dBm
Vcc			+5		V
Reference Current (Iref1 + Iref2)			35		mA
Icq (Icq1 + Icq2)		600	700	800	mA

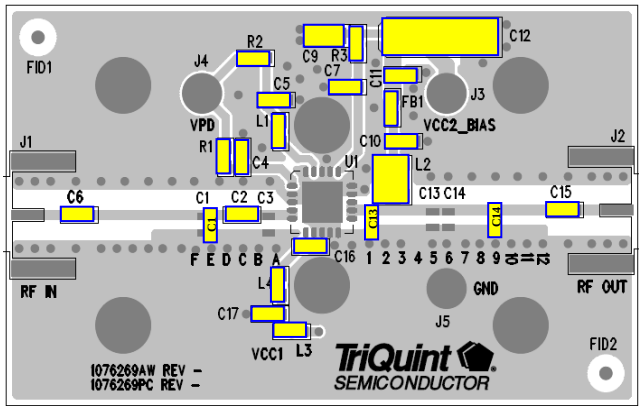
Notes:
1. 3OIP measured with two tones at an output power of +20 dBm / tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule. 2:1 rule gives relative value w.r.t. fundamental tone.
2. 3GPP WCDMA, 1±64DPCH, ±5 MHz, no clipping, PAR = 9.6 dB @ 0.01% Probability.

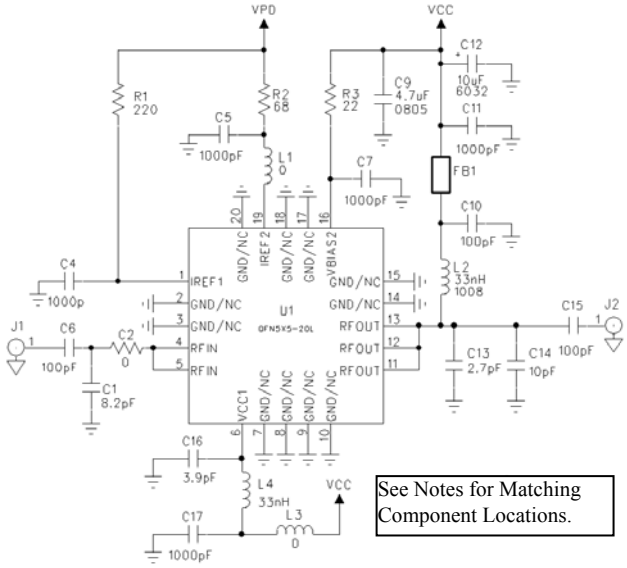
Performance Summary Table

Test conditions unless otherwise noted: +25°C, +5V Vcc, 700 mA Icq, in an application circuit tuned for each frequency.

Frequency	750	850	1850	1960	2140	2650	MHz
Gain	32.5	32	28.8	28.8	27.2	23.6	dB
Input Return Loss	16	14	18	24	25	25	dB
Output Return Loss	10	15	13	20	17	15	dB
Output P1dB	+33	+33.7	+33.3	+33.1	+33.1	+33	dBm
Output IP3 [Note 1]	+45.7	+45.5	+50	+50.3	+50	+47.8	dBm
WCDMA Channel Power @ -50 dBc ACLR	+23.1	+24.1	+23.9	+23.8	+23.9	+23.8	dBm

Reference Design 700-800 MHz





Notes:
1. See PC Board Layout, page 17 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C1 is placed at 250 mils from the U1 device package (10° @ 750 MHz).
6. The edge of C13 is placed at 50 mils from the edge of U1 device package (2° @ 750 MHz).
7. The edge of C14 is placed at 440 mils from the edge of U1 device package (17.5° @ 750 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.
12. C16 is critical for large signal performance.

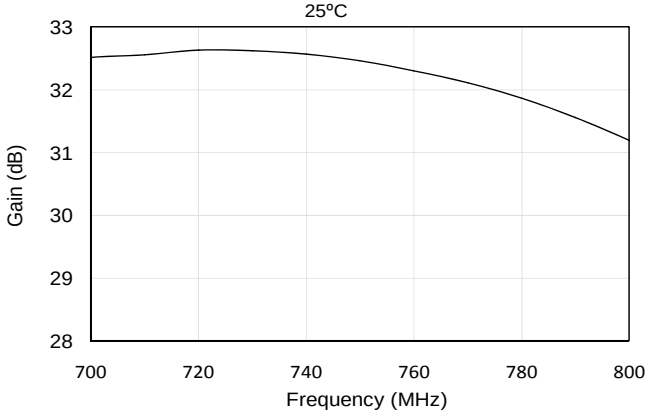
Typical Performance 700-800 MHz

Frequency	MHz	700	750	800
Gain	dB	32.5	32.5	31.2
Input Return Loss	dB	9.5	16	19
Output Return Loss	dB	6.6	10	8
Output P1dB	dBm	+32.5	+33	+32.6
Output IP3 @ 24 dBm/tone, Δf = 1 MHz	dBm	+45	+45.7	+45
WCDMA Channel Power @ -50 dBc ACLR [1]	dBm	+22.7	+23.1	+23.6
Vcc, Vpd	V		+5	
Quiescent Collector Current, Icq (Icq1 + Icq2)	mA		700	
Reference Current (Iref1 + Iref2)	mA		35	

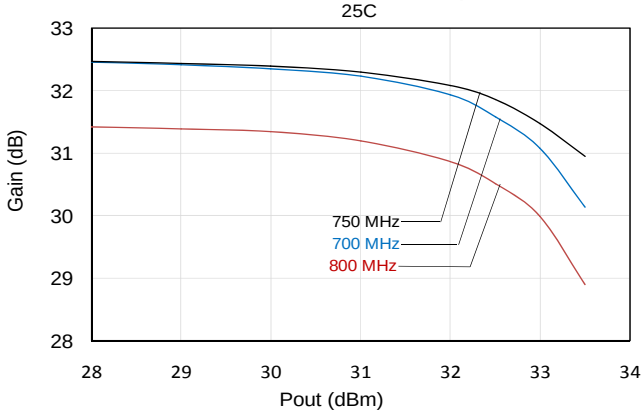
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

Typical Performance Plots 700-800 MHz

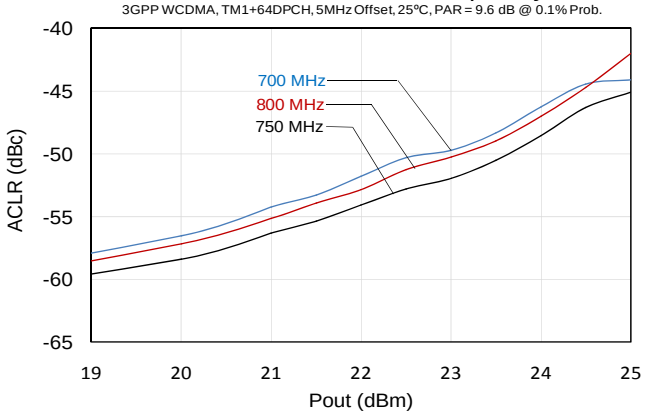
Gain vs. Frequency
25ºC



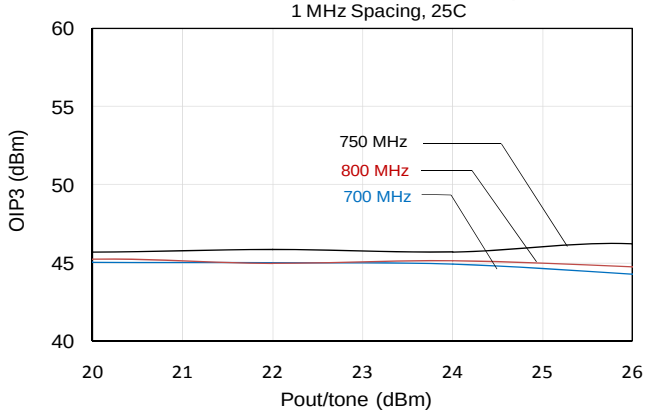
Gain vs. Pout over Frequency
25C



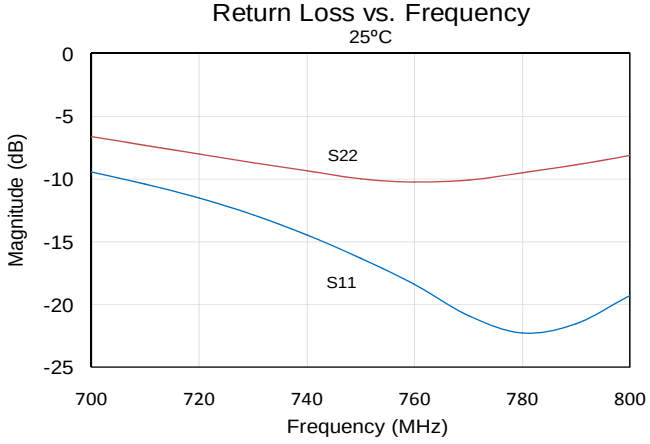
ACLR vs. Pout over Frequency
3GPP WCDMA, TM1+64DPCH, 5MHz Offset, 25ºC, PAR = 9.6 dB @ 0.1% Prob.



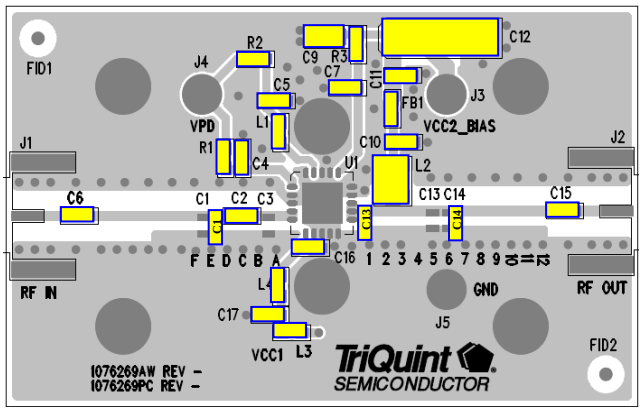
OIP3 vs. Pout/tone over Frequency
1 MHz Spacing, 25C

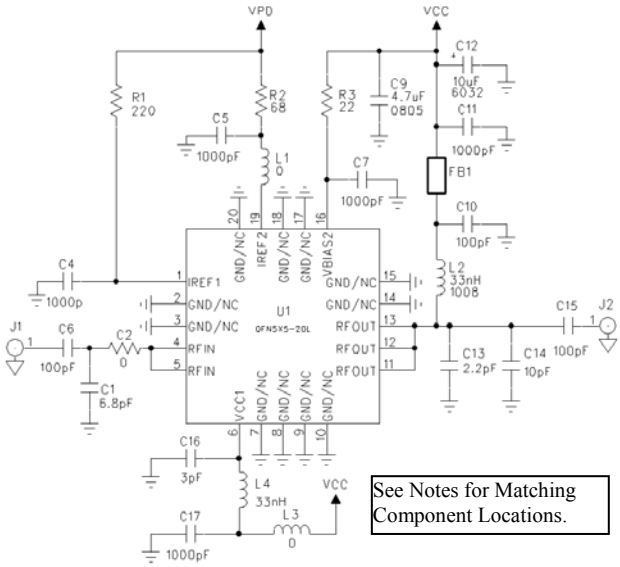


Return Loss vs. Frequency
25ºC



Reference Design 800-900 MHz





See Notes for Matching Component Locations.

Notes:
1. See PC Board Layout, page 17 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C1 is placed at 225 mils from the edge of U1 device package (10º @ 850 MHz).
6. The edge of C13 is placed at 10 mils from the edge of U1 device package (0.5º @ 850 MHz).
7. The edge of C14 is placed at 320 mils from the edge of U1 device package (14.5º @ 850 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.
12. C16 is critical for large signal performance.

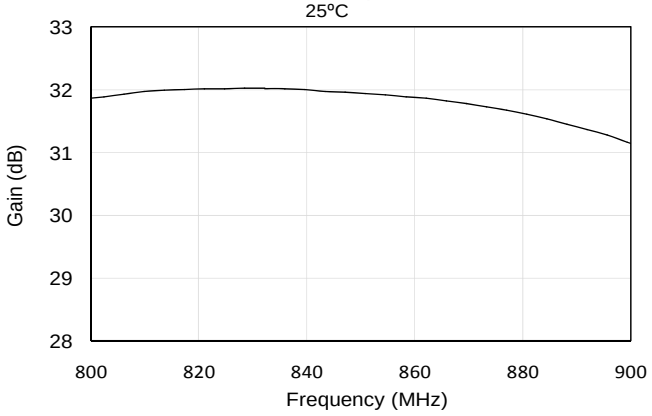
Typical Performance 800-900 MHz

Frequency	MHz	800	850	900
Gain	dB	31.9	32	31.1
Input Return Loss	dB	9	14	23
Output Return Loss	dB	7.7	15	11.7
Output P1dB	dBm	+33	+33.7	+34
Output IP3 @ 24 dBm/tone, Δf = 1 MHz	dBm	+46	+45.5	+45.3
WCDMA Channel Power @ -50 dBc ACLR [1]	dBm	+23.4	+24.1	+24.1
Vcc, Vpd	V		+5	
Quiescent Collector Current, Icq (Icq1 + Icq2)	mA		700	
Reference Current (Iref1 + Iref2)	mA		35	

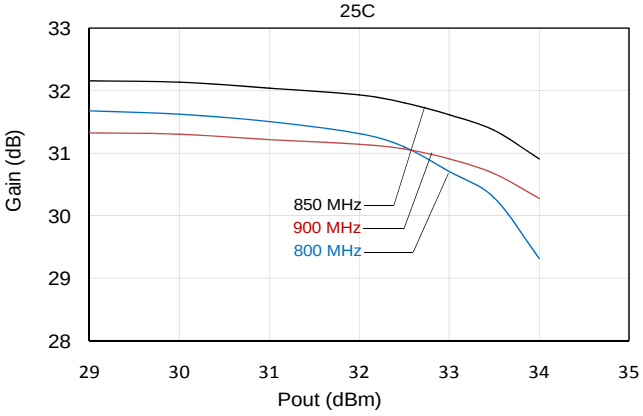
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

Typical Performance Plots 800-900 MHz

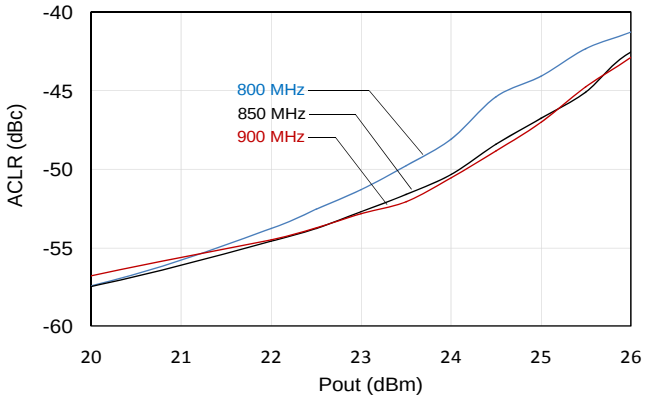
Gain vs. Frequency
25ºC



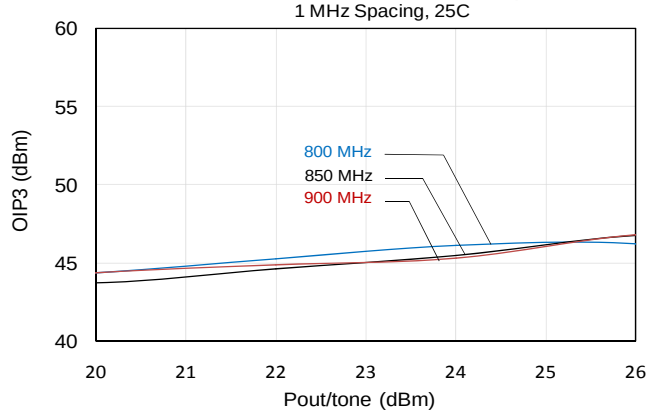
Gain vs. Pout over Frequency
25C



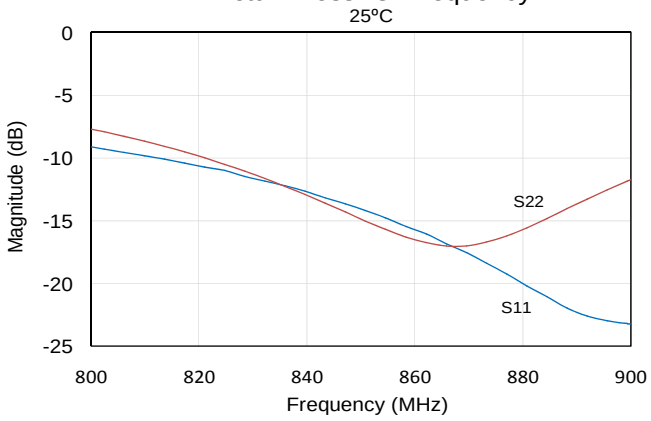
ACLR vs. Pout over Frequency
3GPP WCDMA, TM1+64DPCH, 5MHz Offset, 25ºC, PAR=9.6 dB @ 0.01% Prob.



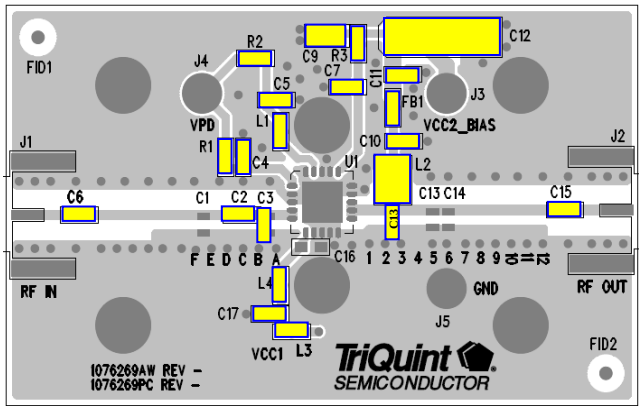
OIP3 vs. Pout/tone over Frequency
1 MHz Spacing, 25C

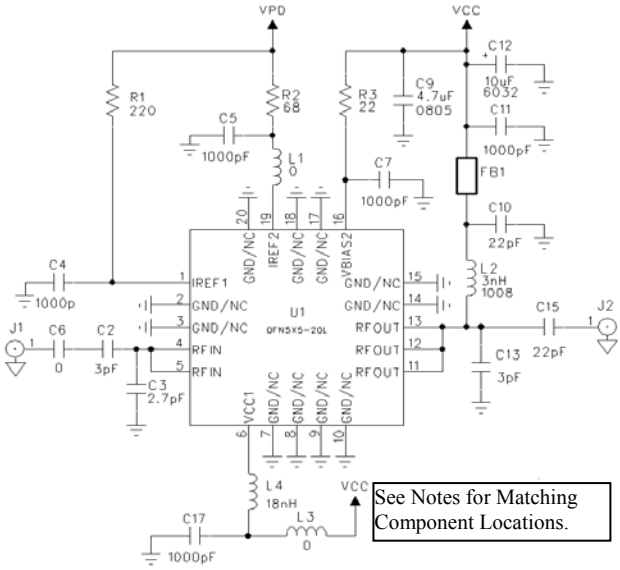


Return Loss vs. Frequency
25ºC



Reference Design 1800-1900 MHz





Notes:
1. See PC Board Layout, page 17 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C2 is placed at 128 mils from the U1 device package (12.5° @ 1850 MHz).
6. The edge of C3 is placed at 70 mils from the edge of U1 device package (7° @ 1850 MHz).
7. The edge of C13 is placed at 110 mils from the edge of U1 device package (10.7° @ 1850 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.

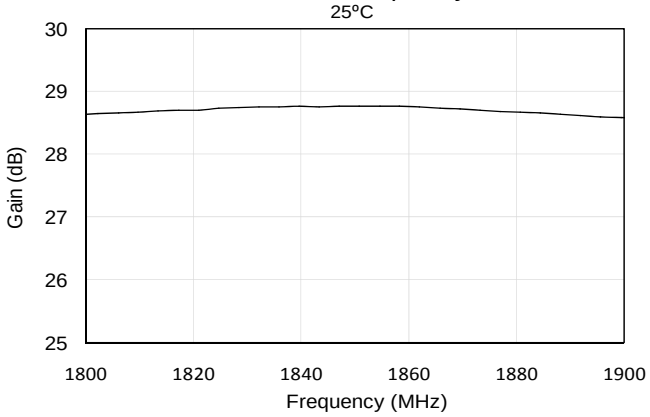
Typical Performance 1800-1900 MHz

Frequency	MHz	1800	1850	1900
Gain	dB	28.6	28.8	28.6
Input Return Loss	dB	13	17.6	20.5
Output Return Loss	dB	10.5	13	14.4
Output P1dB	dBm	+33.2	+33.3	+33.1
Output IP3 @ 24 dBm/tone, Δf = 1 MHz	dBm	+49	+50	+49
WCDMA Channel Power @ -50 dBc ACLR [1]	dBm	+23.7	+23.9	+23.9
Vcc, Vpd	V		+5	
Quiescent Collector Current, Icq (Icq1 + Icq2)	mA		700	
Reference Current (Iref1 + Iref2)	mA		35	

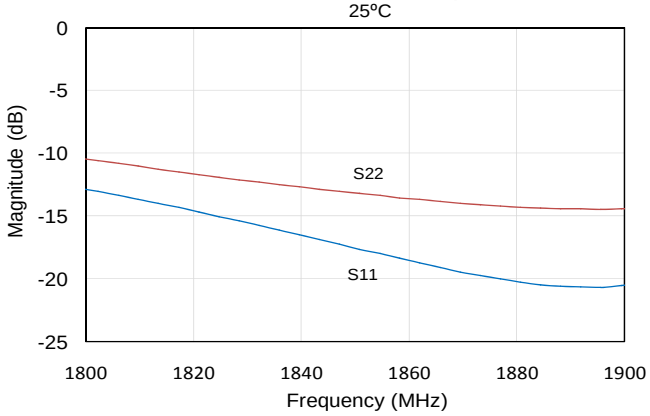
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

Typical Performance Plots 1800-1900 MHz

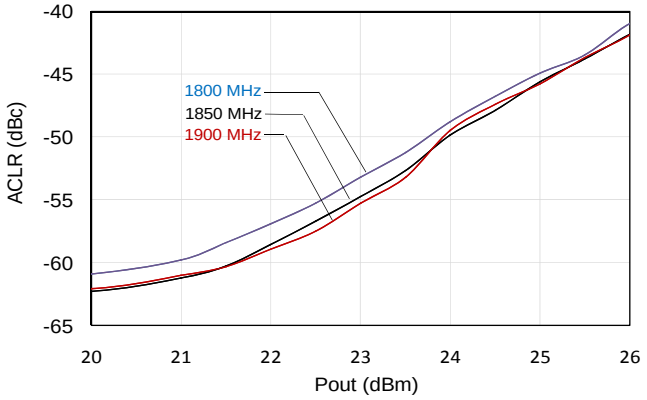
Gain vs. Frequency
25°C



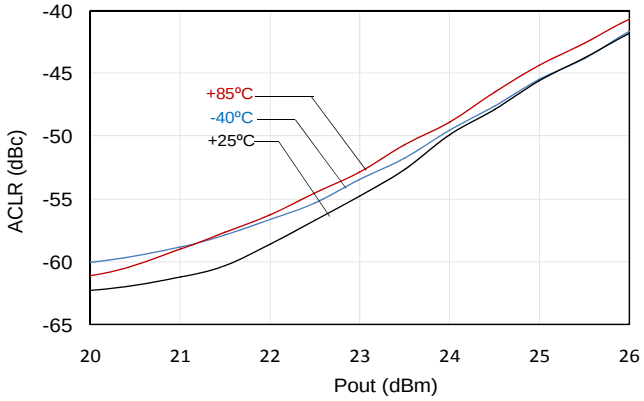
Return Loss vs. Frequency
25°C



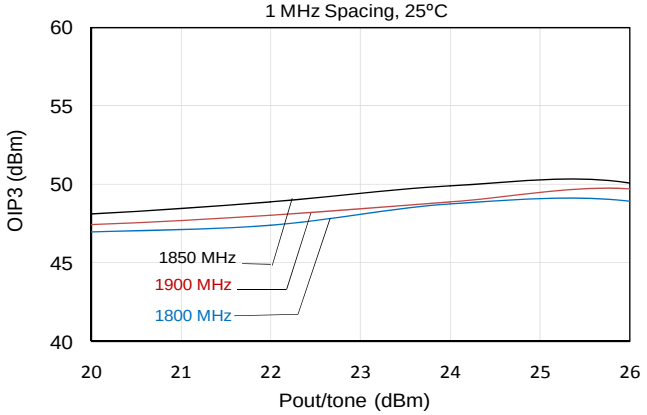
ACLR vs. Pout over Frequency
3GPP WCDMA, TM1+64DPCH, 5MHz Offset, 25°C, PAR=9.6 dB @ 0.01% Prob.



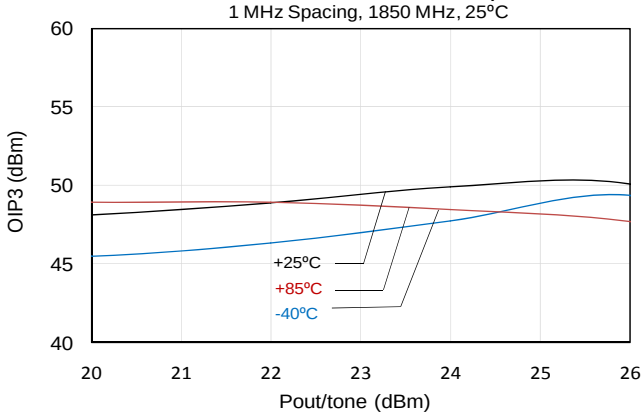
ACLR vs. Pout over Temperature
3GPP WCDMA, TM1+64DPCH, 5MHz Offset, 1850 MHz, PAR=9.6 dB @ 0.01% Prob.



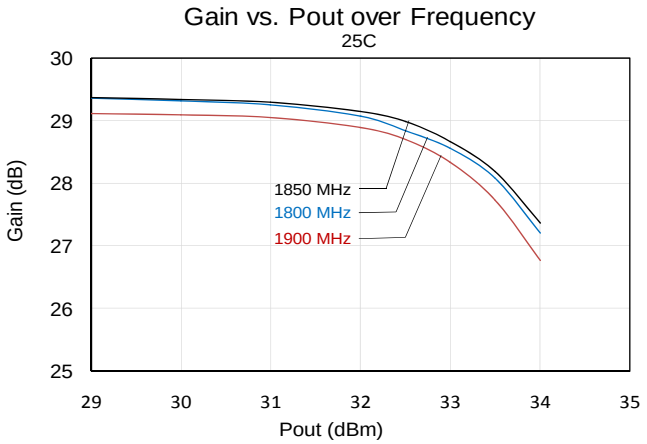
OIP3 vs. Pout/tone over Frequency
1 MHz Spacing, 25°C

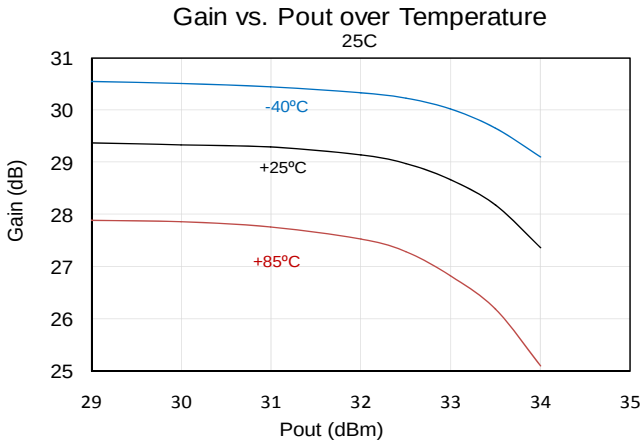


OIP3 vs. Pout/tone over Temperature
1 MHz Spacing, 1850 MHz, 25°C

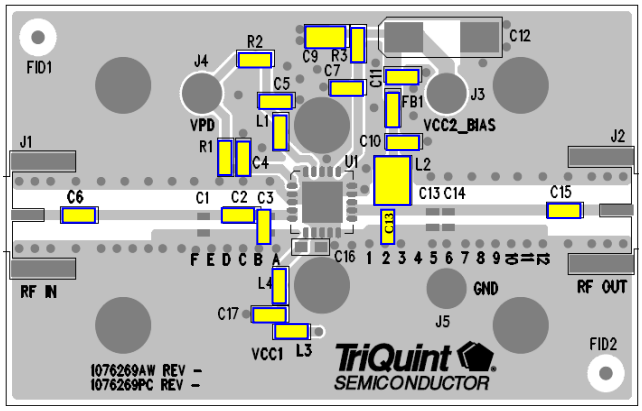


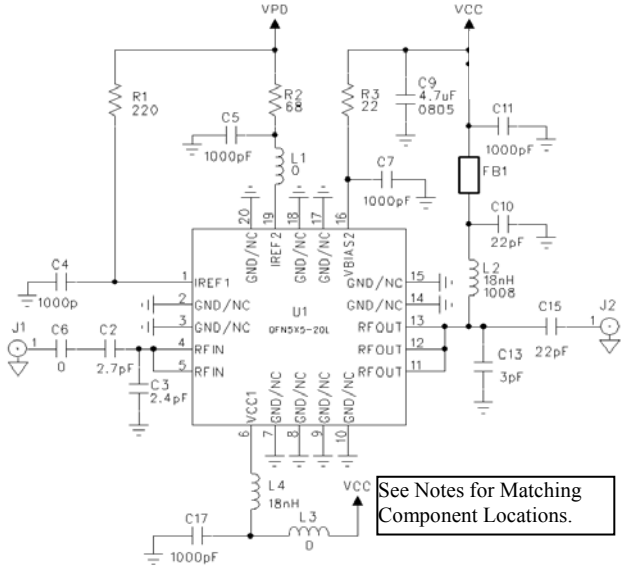
Typical Performance Plots 1800-1900 MHz





Reference Design 1930-1990 MHz





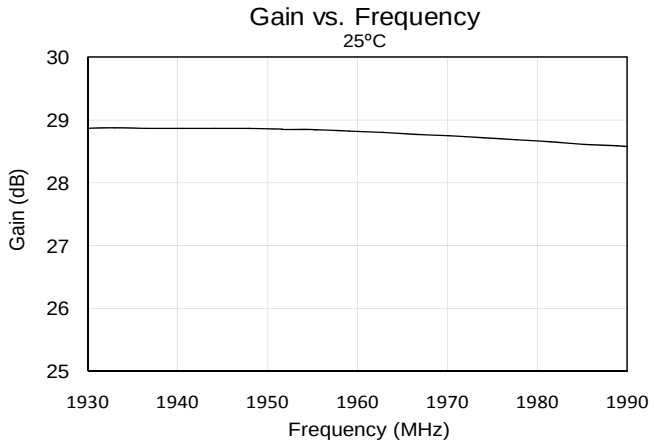
Notes:
1. See PC Board Layout, page 17 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C2 is placed at 128 mils from the U1 device package (13° @ 1960 MHz).
6. The edge of C3 is placed at 70 mils from the edge of U1 device package (7.3° @ 1960 MHz).
7. The edge of C13 is placed at 100 mils from the edge of U1 device package (10.4° @ 1960 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.

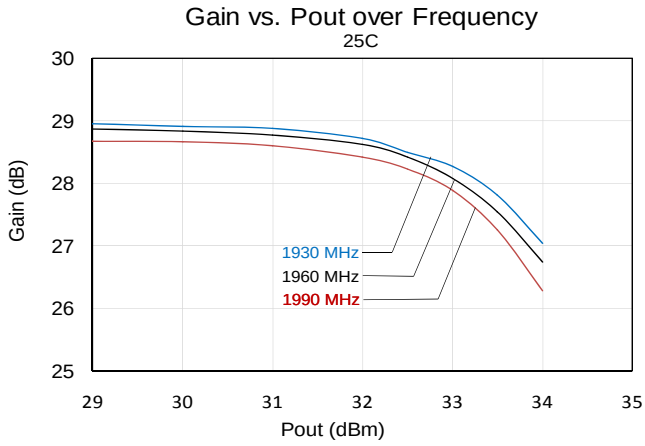
Typical Performance 1930-1990 MHz

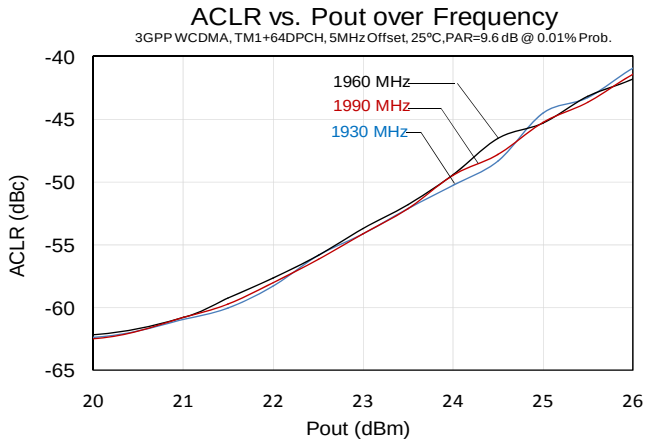
Frequency	MHz	1930	1960	1990
Gain	dB	28.9	28.8	28.6
Input Return Loss	dB	20	24	22
Output Return Loss	dB	16.5	19.6	20.6
Output P1dB	dBm	+33.2	+33.1	+33.1
Output IP3 @ 24 dBm/tone, Δf = 1 MHz	dBm	+50.3	+50.3	+50.3
WCDMA Channel Power @ -50 dBc ACLR [1]	dBm	+24	+23.8	+23.8
Vcc, Vpd	V		+5	
Quiescent Collector Current, Icq (Icq1 + Icq2)	mA		700	
Reference Current (Iref1 + Iref2)	mA		35	

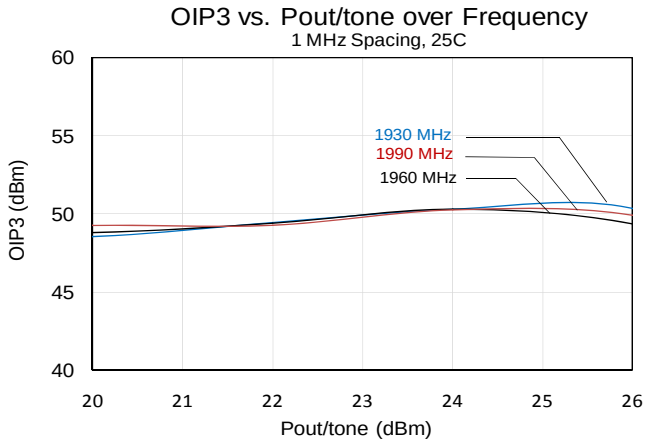
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

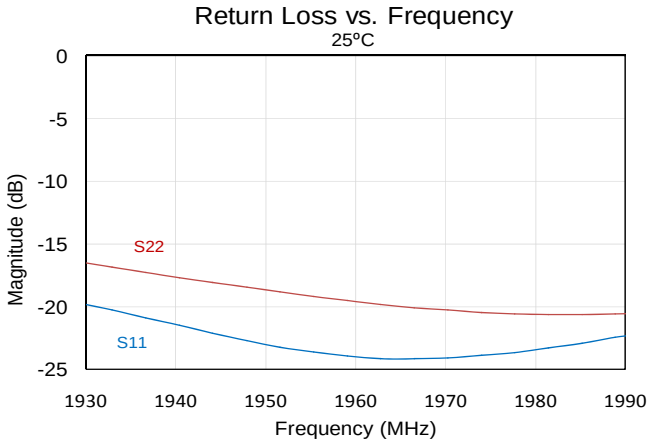
Typical Performance Plots 1930-1990 MHz



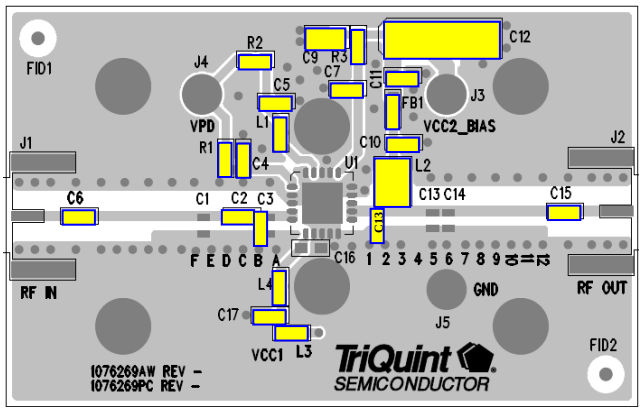


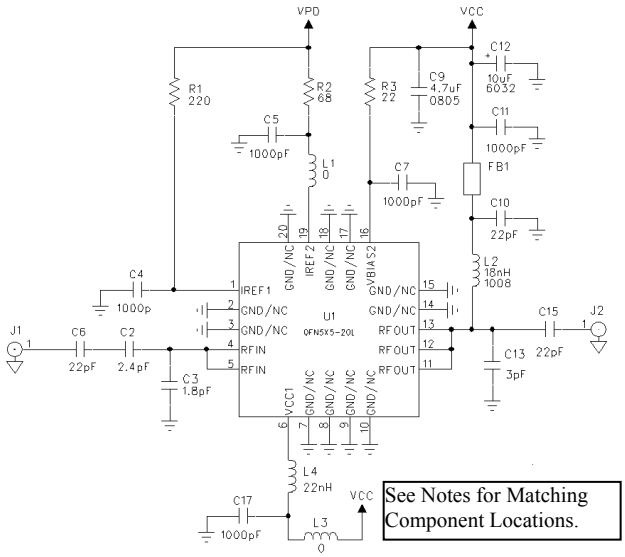






Application Circuit 2110-2170 MHz (AH323-PCB2140)





See Notes for Matching Component Locations.

Notes:
1. See PC Board Layout, page 17 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C2 is placed at 128 mils from the U1 device package (14.5° @ 2140 MHz).
6. The edge of C3 is placed at 80 mils from the edge of U1 device package (9° @ 2140 MHz).
7. The edge of C13 is placed at 70 mils from the edge of U1 device package (8° @ 2140 MHz).
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.
12. Low cost ceramic SQ series capacitors are used for matching.

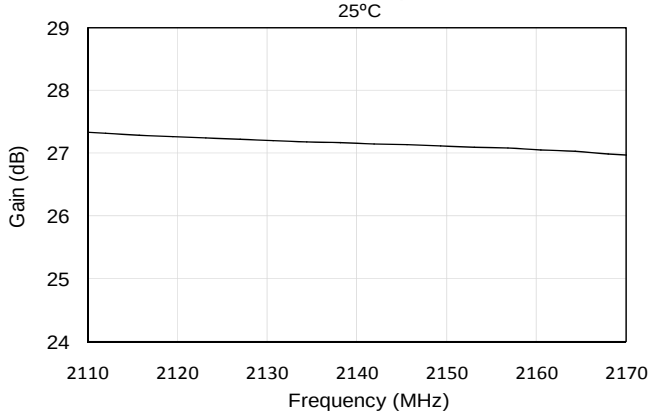
Typical Performance 2110-2170 MHz

Frequency	MHz	2110	2140	2170
Gain	dB	27.3	27.2	27
Input Return Loss	dB	20	25	32
Output Return Loss	dB	17	16.6	17
Output P1dB	dBm	+33.2	+33.1	+33.1
Output IP3 @ 24 dBm/tone, Δf = 1 MHz	dBm	+49.7	+50	+50
WCDMA Channel Power @ -50 dBc ACLR [1]	dBm	+24	+23.9	+23.9
Noise Figure	dB	4.2	4.2	4.3
Vcc, Vpd	V		+5	
Quiescent Collector Current, Icq (Icq1 + Icq2)	mA		700	
Reference Current (Iref1 + Iref2)	mA		35	

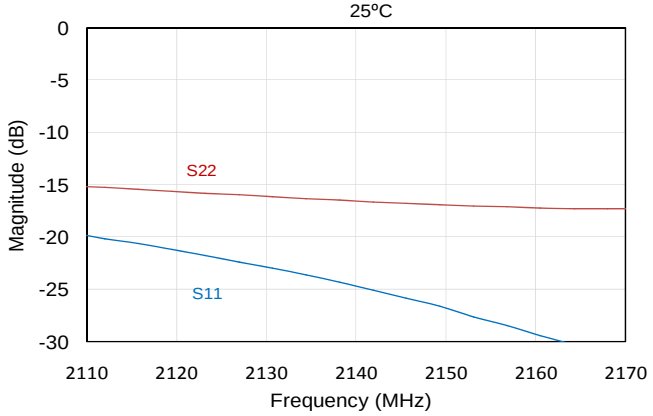
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

Typical Performance Plots 2110-2170 MHz

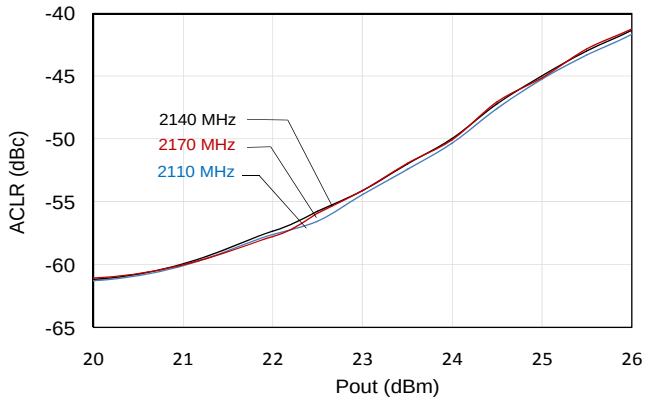
Gain vs. Frequency
25ºC



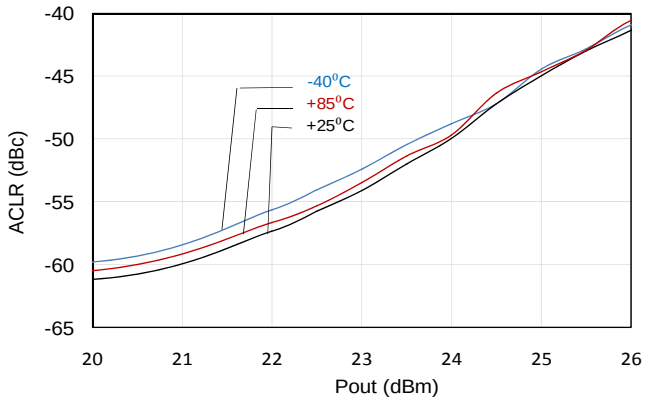
Return Loss vs. Frequency
25ºC



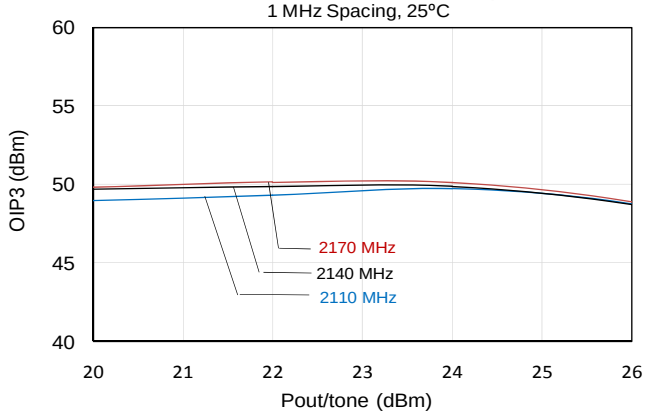
ACLR vs. Pout over Frequency
3GPP WCDMA, TM1+64DPCH, 5MHz Offset, 25ºC, PAR=9.6 dB @ 0.01% Prob.



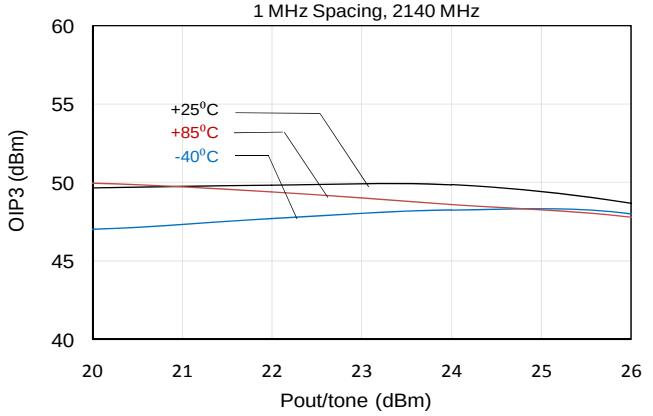
ACLR vs. Pout over Temperature
3GPP WCDMA, TM1+64DPCH, 5MHz Offset, 2140 MHz, PAR=9.6 dB @ 0.01% Prob.



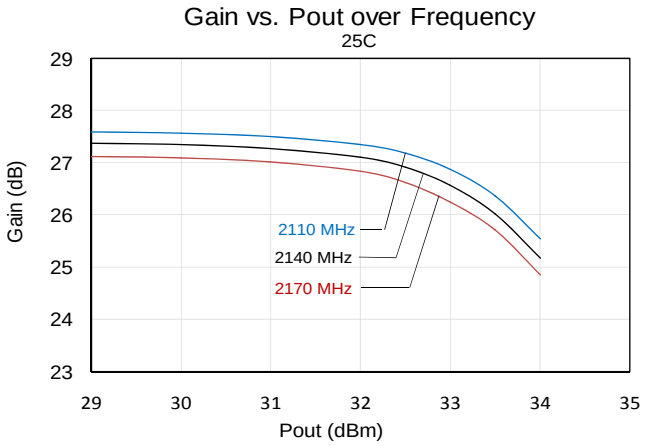
OIP3 vs. Pout/tone over Frequency
1 MHz Spacing, 25ºC

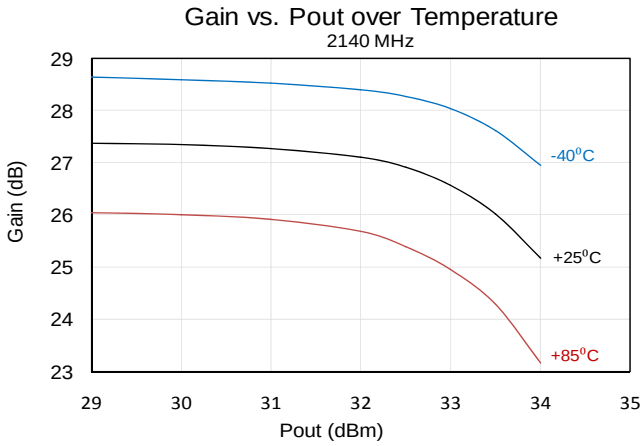


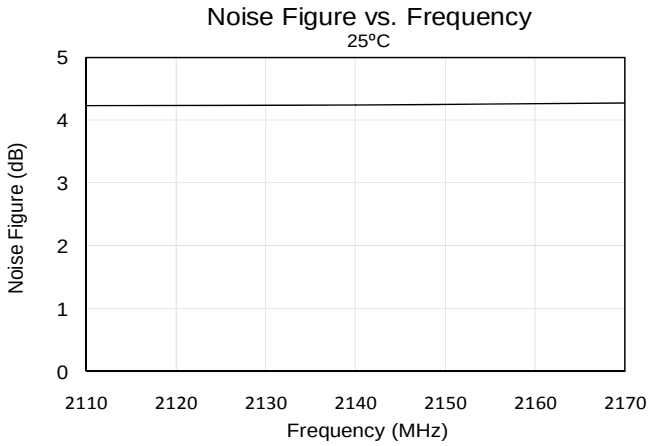
OIP3 vs. Pout/tone over Temperature
1 MHz Spacing, 2140 MHz



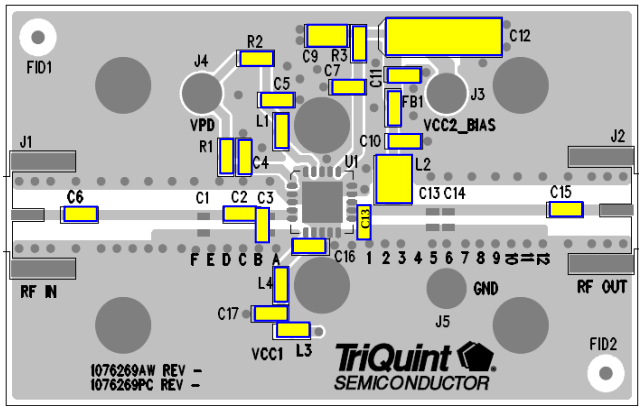
Typical Performance Plots 2110-2170 MHz

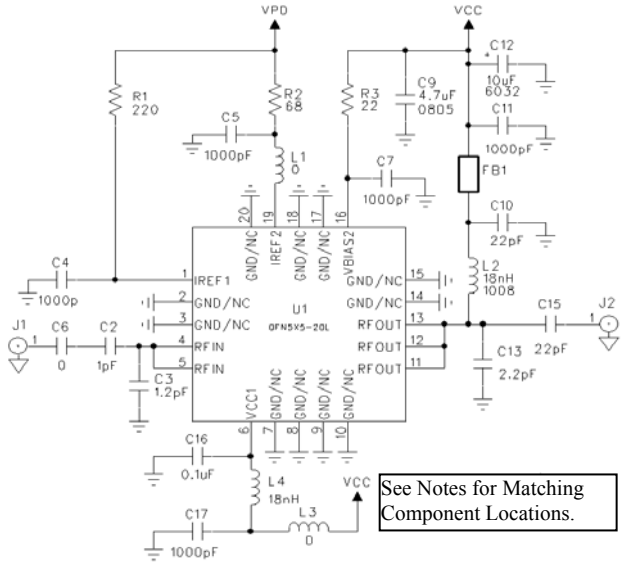






Reference Design 2600-2700 MHz





See Notes for Matching Component Locations.

Notes:
1. See PC Board Layout, page 17 for more information.
2. Vcc1 is connected to Vcc2_bias J3 turret via inner layer line.
3. The primary RF microstrip characteristic line impedance is 50 Ω.
4. Components shown on the silkscreen but not on the schematic are not used.
5. The edge of C2 is placed at 128 mils from the U1 device package (18° @ 2650 MHz).
6. The edge of C3 is placed at 75 mils from the edge of U1 device package (10.5° @ 2650 MHz).
7. The edge of C13 is placed as close as possible to the edge of U1 device package.
8. Zero ohm jumpers may be replaced with copper traces in the target application layout.
9. The locations of C6 and C15 are non-critical. They can be placed closer to the device. C6 can be replaced by 0 ohm jumper.
10. Ferrite Bead FB1 eliminates bias line resonances between C10 and the parasitic inductance of C11. Steward MI0603K300R-10.
11. All components are of 0603 size unless stated otherwise.

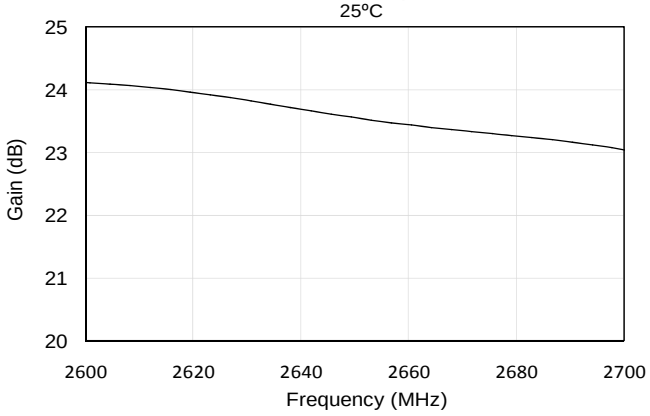
Typical Performance 2600-2700 MHz

Frequency	MHz	2600	2650	2700
Gain	dB	24.1	23.6	23
Input Return Loss	dB	17	25	23
Output Return Loss	dB	14	15	16
Output P1dB	dBm	+33	+33	+32.9
Output IP3 @ 24 dBm/tone, Δf = 1 MHz	dBm	+47.6	+47.8	+46
WCDMA Channel Power @ -50 dBc ACLR [1]	dBm	+23.6	+23.8	+23.8
Vcc, Vpd	V		+5	
Quiescent Collector Current, Icq (Icq1 + Icq2)	mA		700	
Reference Current (Iref1 + Iref2)	mA		35	

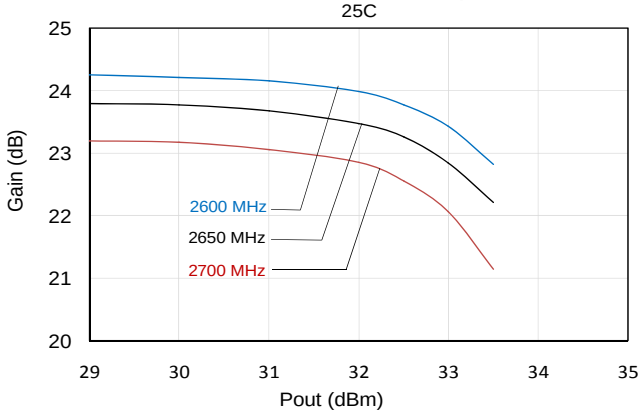
Notes:
1. ACLR Test set-up: 3GPP WCDMA, TM1+64 DPCH, +5MHz offset, PAR = 9.6 dB @ 0.01% Prob.

Typical Performance Plots 2600-2700 MHz

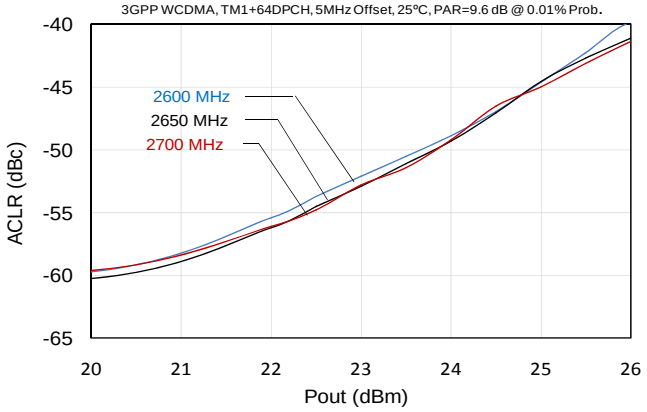
Gain vs. Frequency
25ºC



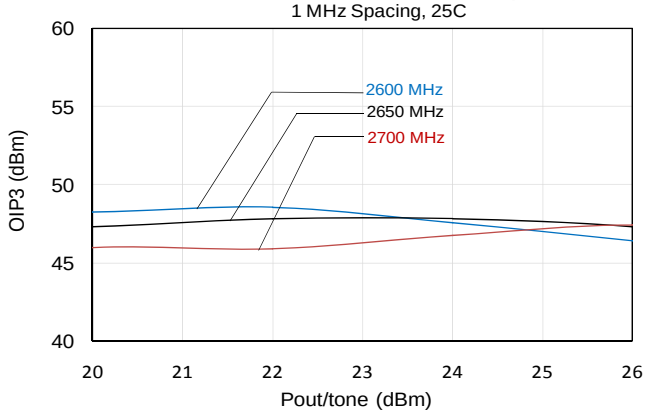
Gain vs. Pout over Frequency
25C



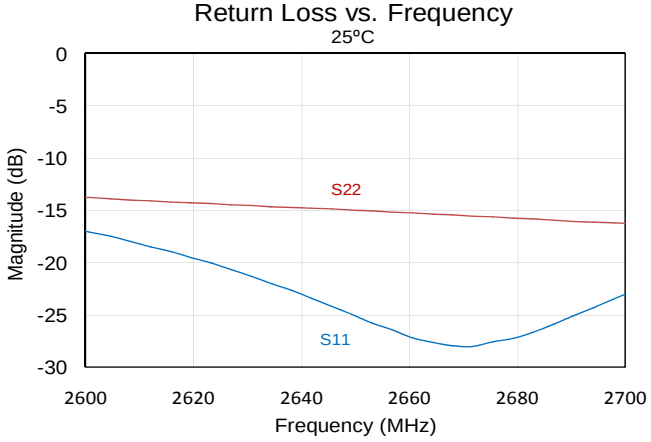
ACLR vs. Pout over Frequency
3GPP WCDMA, TM1+64DPCH, 5MHz Offset, 25ºC, PAR=9.6 dB @ 0.01% Prob.



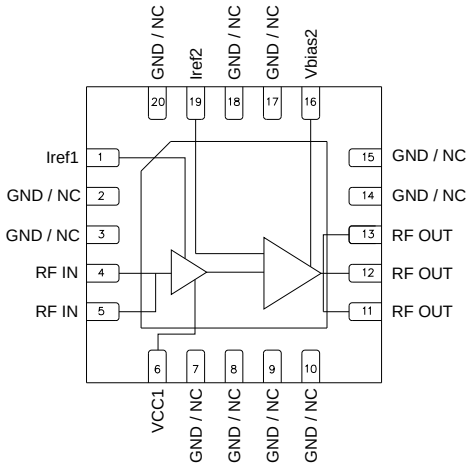
OIP3 vs. Pout/tone over Frequency
1 MHz Spacing, 25C



Return Loss vs. Frequency
25ºC



Pin Description



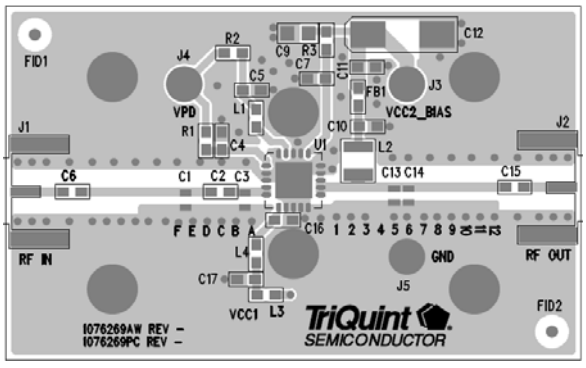
Pin	Symbol	Description
6	Vcc1	Supply voltage for first stage amplifier. RF Choke is needed.
1	Iref1	Reference current into internal active bias current mirror. Current into Iref sets device quiescent current for first stage. It can be used as on/off control. Iref1 current is set by providing +5Vpd through dropping resistor on EVB.
19	Iref2	Reference current into internal active bias current mirror. Current into Iref sets device quiescent current for 2nd stage. It can be used as on/off control. Iref2 current is set by providing +5Vpd through dropping resistor on EVB.
4,5	RFin	Input, requires matching for operation.
11,12,13	RFout/Vcc2	Output, requires matching for operation. Supply voltage for 2nd stage amplifier. RF Choke is needed.
16	Vbias2	Voltage supply for active bias for second stage. Bypass cap is recommended.
2,3,7,8,9,10,14,15,17,18,20	NC / GND	No internal connection. This pin can be grounded or N/C on PCB.
GND	Backside Paddle	Need to be grounded as shown in Mounting Configuration section for good thermal and electrical performance.

Application Board Information

PC Board Layout

Top RF layer is .014" Getek, ϵ_r = 4.0, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line details: width = .030", spacing = .030".

The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitors – C1, C2, C3, C13 and C14. The markers and vias are spaced in .050" increments.



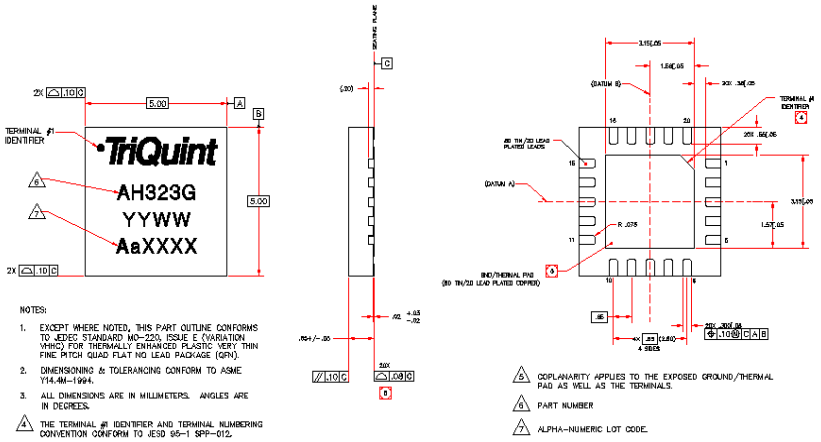
The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.
For further technical information, Refer to www.TriQuint.com

Mechanical Information

Package Information and Dimensions

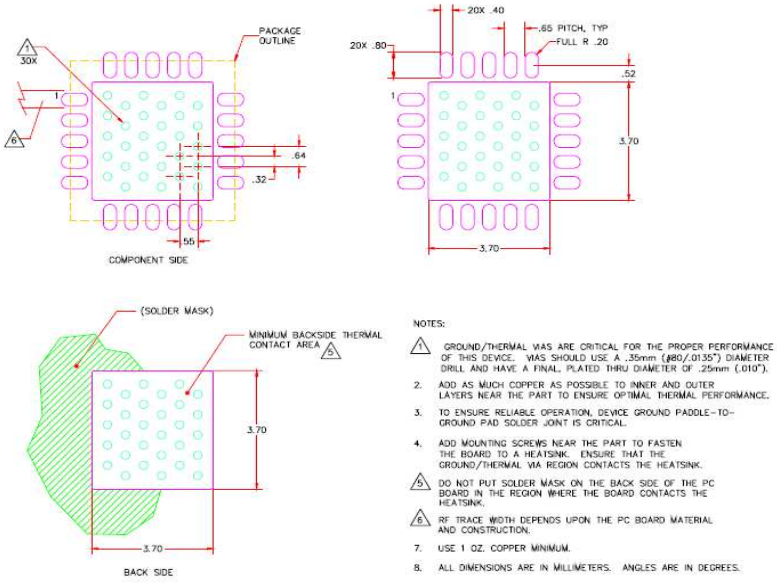
This package is lead-free, RoHS-compliant, and green. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

The component will be laser marked with "AH323G" product label with an alphanumeric lot code on the top surface of the package. The "YY" represents the last digit of the year the part was manufactured, "WW" represents the work week, where the part was manufactured, "Aa" represents the vendor code, and "XXXX" is an auto-generated lot number.



Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.



Notes:
1. A heatsink underneath the area of the PCB for the mounted device is required for proper thermal operation.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1C
Value:	Passes ≥ 1000V to < 2000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 2000V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 3 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

Web: www.triquint.com **Tel:** +1.503.615.9000
Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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