# AH420

**4W High Linearity InGaP HBT Amplifier**

## Product Features

- 400 – 2700 MHz
- +35.7 dBm P1dB
- -49 dBc ACLR @ 26 dBm
- 14 dB Gain @ 2140 MHz
- 800 mA Quiescent Current
- +5 V Single Supply
- MTTF > 100 Years
- Lead-free/green/RoHS-compliant 12-pin 4x5mm DFN Package

## Applications

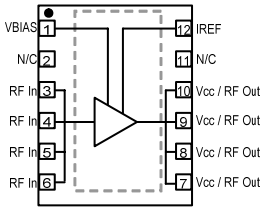
- Final stage amplifiers for Repeaters
- High Power Amplifiers
- Mobile Infrastructure
- LTE / WCDMA / EDGE / CDMA

## Product Description

The AH420 is a high dynamic range amplifier in a low-cost surface mount package. The InGaP/GaAs HBT is able to achieve high performance with -49 dBc ACLR and +35.7 dBm of compressed 1dB power, operating off of a single +5V supply. It is housed in a lead-free/green/RoHS-compliant 4x5mm DFN package. All devices are 100% RF and DC tested.

The AH420 is targeted for use as a final stage amplifier in wireless infrastructure repeaters or as driver stages for high power amplifiers where high performance is required. In addition, the amplifier can be used for a wide variety of other applications within the 400 to 2700 MHz frequency band. By operating off of a single +5V rail, other higher voltage rails are not necessarily needed thus saving system costs. The amplifier also has the flexibility to operate at higher voltage levels to achieve higher compression if needed by the system.

## Functional Diagram




| Function | Pin No. |
|---|---|
| $RF_{IN}$ | 3,4,5,6 |
| $RF_{OUT}$ | 7,8,9,10 |
| $I_{REF}$ | 12 |
| $V_{BIAS}$ | 1 |
| NC | 2,11 |

## Specifications

| Parameter | Units | Min | Typ | Max |
|---|---|---|---|---|
| Operational Bandwidth | MHz | 400 | | 2700 |
| Test Frequency | MHz | | 2140 | |
| Output Channel Power | dBm | | +26 | |
| Gain | dB | 13 | 14 | 16 |
| Input Return Loss | dB | | 12 | |
| Output Return Loss | dB | | 7.4 | |
| ACLR [2] | dBc | | -49 | |
| Output P1dB | dBm | | +35.7 | |
| Output IP3 [4] | dBm | +46.5 | +50 | |
| Quiescent Collector Current [3] | mA | 710 | 800 | 900 |
| Iref | mA | | 20 | |
| Vcc, Vbias | V | | +5 | |

1. Test conditions unless otherwise noted: 25ºC, +5V Vsupply, 2140 MHz, in tuned application circuit.
2. W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.2 dB @ 0.01% Probability, 3.84 MHz BW
3. This corresponds to the quiescent current under small-signal conditions into pins 6, 7, and 8 when the current setting resistor, R4 connected to the Iref pin, is at 82 Ω.
4. OIP3 is measured with two tones at out an output power of +27 dBm/tone separated by 1 MHz. The suppression on the largest IM3 product is used to calculate the 3OIP using a 2:1 rule.

## Typical Performance

| Parameter | Units | Typical | | |
|---|---|---|---|---|
| Frequency | MHz | 940 | 1960 | 2140 |
| Channel Power | dBm | +27 | +27 | +26 |
| Gain | dB | 16 | 14.1 | 14 |
| Input Return Loss | dB | 14 | 19 | 12 |
| Output Return Loss | dB | 6.4 | 7 | 7.4 |
| ACLR [2] | dBc | -46.5 | -48 | -49 |
| Output P1dB | dBm | +35.2 | +35.6 | +35.7 |
| Noise Figure | dB | 6.6 | 5.3 | 5.6 |
| Output IP3 [4] | dBm | +50 | +49 | +50 |
| Quiescent Collector Current [3] | mA | | 800 | |
| Iref | mA | | 20 | |
| Vcc, Vbias | V | | +5 | |

5. The amplifier has been tested for ruggedness to be capable of handling:
   10:1 VSWR @ 5Vcc, 2140MHz, +35.2dBm CW Pout, 25 °C
   10:1 VSWR @ 5Vcc, 940MHz, +28.5dBm IS-95A Pout, 25 °C
   10:1 VSWR @ 5Vcc, 2140MHz, +26.5dBm WCDMA Pout, 25 °C

## Absolute Maximum Ratings

| Parameter | Rating |
|---|---|
| Storage Temperature | -65 to +150 °C |
| Vcc, Vbias | +14 V |
| RF Input Power, CW, 50 Ω, T=25°C | Input P9dB |
| Reference Current, Iref | 170 mA |
| Dissipated Power, Pmax | 7 W |
| Max Junction Temperature, $T_J$ For $10^6$ hours MTTF | 158 °C |
| Thermal Resistance, $\Theta_{JC}$ | 10.6 °C / W |

Operation of this device above any of these parameters may cause permanent damage.

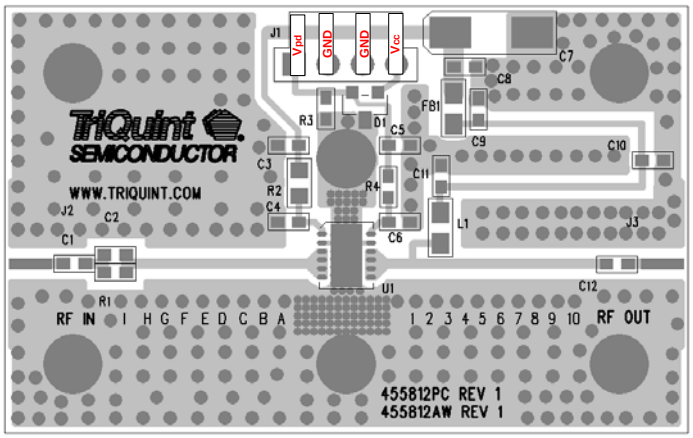
## Ordering Information

| Part No. | Description |
|---|---|
| AH420-EG | 4W High Linearity InGaP HBT Amplifier |
| AH420-EPCB900 | 920-960 MHz Evaluation Board |
| AH420-EPCB1960 | 1930-1990 MHz Evaluation Board |
| AH420-EPCB2140 | 2110-2170 MHz Evaluation Board |

Standard T/R size = 1000 pieces on a 7" reel.

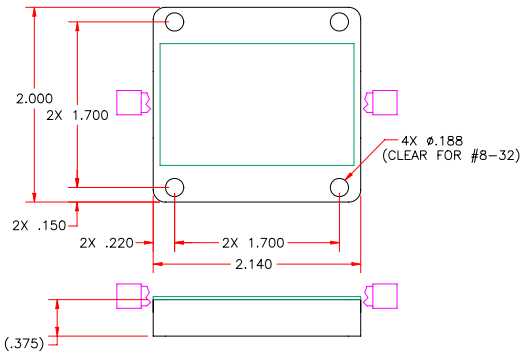
Specifications and information are subject to change without notice.

## Application Circuit PC Board Layout




Circuit Board Material: 0.014" GETEK, single layer, 1 oz copper, $\varepsilon_r = 4.2$,
Microstrip line details: width = .030", marker spacing = .050"

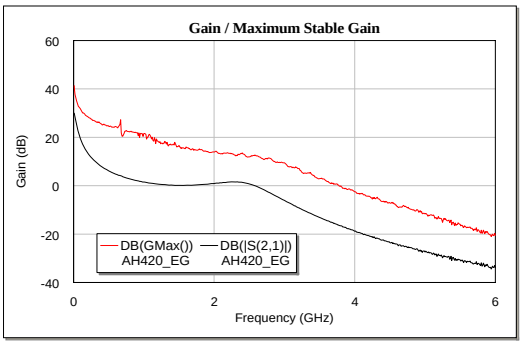
## Baseplate Configuration

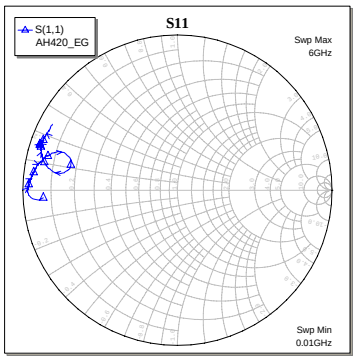


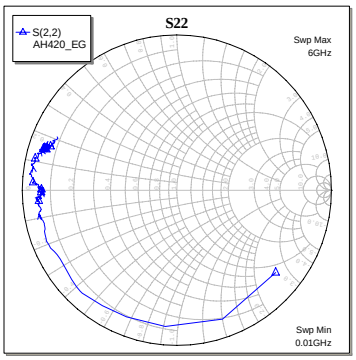

Notes:
1. Please note that for reliable operation, the evaluation board will have to be mounted to a much larger heat sink during operation and in laboratory environments to dissipate the power consumed by the device. The use of a convection fan is also recommended in laboratory environments.
2. The area around the module underneath the PCB should not contain any soldermask in order to maintain good RF grounding.

## Typical Device Data

S-Parameters ($V_{CC}$= +5 V, $I_{CC}$ = 800 mA, 25 °C, unmatched 50 ohm system)




**Notes:**
The gain for the unmatched device in 50 ohm system is shown as the trace in black color. For a tuned circuit for a particular frequency, it is expected that actual gain will be higher, up to the maximum stable gain. The maximum stable gain is shown in the red line.

S-Parameters ($V_{CC}$ = +5 V, $I_{CQ}$ = 800 mA, 25 °C, unmatched 50 ohm system, calibrated to device leads)

| Freq (MHz) | S11 (dB) | S11 (deg) | S21 (dB) | S21 (deg) | S12 (dB) | S12 (deg) | S22 (dB) | S22 (deg) |
|---|---|---|---|---|---|---|---|---|
| 10 | -1.22 | -176.79 | 29.97 | 155.67 | -52.77 | 64.11 | -1.61 | -39.70 |
| 50 | -0.44 | -177.23 | 24.42 | 117.15 | -45.04 | 32.25 | -1.05 | -122.90 |
| 100 | -0.31 | -178.77 | 19.17 | 103.73 | -44.01 | 11.29 | -1.16 | -150.31 |
| 300 | -0.28 | 179.40 | 10.27 | 90.61 | -43.22 | 5.32 | -0.94 | -169.59 |
| 500 | -0.30 | 178.17 | 6.16 | 84.91 | -43.10 | -0.42 | -0.93 | -174.28 |
| 700 | -0.40 | 176.72 | 3.74 | 79.16 | -43.48 | 36.07 | -1.02 | -177.33 |
| 900 | -0.43 | 175.77 | 2.09 | 74.69 | -41.72 | 5.11 | -1.07 | -177.23 |
| 1100 | -0.50 | 173.96 | 0.99 | 69.01 | -41.21 | -1.08 | -1.11 | -178.10 |
| 1300 | -0.59 | 171.86 | 0.42 | 62.55 | -40.35 | -4.63 | -1.15 | -178.55 |
| 1500 | -0.74 | 169.75 | 0.16 | 55.48 | -39.33 | -10.41 | -1.21 | -179.14 |
| 1700 | -0.98 | 167.20 | 0.25 | 46.05 | -38.86 | -20.47 | -1.24 | -179.88 |
| 1900 | -1.40 | 164.19 | 0.63 | 34.50 | -38.13 | -34.84 | -1.24 | 179.85 |
| 2100 | -2.04 | 161.94 | 1.22 | 18.13 | -36.71 | -51.74 | -1.19 | 179.15 |
| 2300 | -2.78 | 163.47 | 1.53 | -4.61 | -35.70 | -78.76 | -0.95 | 178.06 |
| 2500 | -2.88 | 169.61 | 0.74 | -32.66 | -36.03 | -114.19 | -0.62 | 175.59 |
| 2700 | -2.04 | 171.93 | -1.59 | -58.88 | -37.72 | -145.67 | -0.52 | 171.28 |
| 2900 | -1.32 | 169.73 | -4.55 | -77.51 | -39.74 | -179.01 | -0.55 | 168.08 |
| 3100 | -0.95 | 167.05 | -7.58 | -90.68 | -41.31 | 163.85 | -0.68 | 165.55 |
| 3300 | -0.78 | 164.66 | -10.52 | -100.04 | -42.50 | 141.73 | -0.80 | 164.25 |
| 3500 | -0.69 | 162.98 | -13.08 | -106.66 | -43.74 | 129.82 | -0.87 | 162.92 |
| 3700 | -0.63 | 161.89 | -15.60 | -112.19 | -42.73 | 112.53 | -0.90 | 162.24 |
| 3900 | -0.61 | 161.39 | -17.79 | -116.53 | -43.74 | 105.15 | -0.92 | 161.57 |
| 4100 | -0.58 | 161.33 | -19.66 | -121.50 | -43.35 | 107.61 | -0.92 | 161.67 |
| 4300 | -0.54 | 161.51 | -21.87 | -124.38 | -42.62 | 97.03 | -0.97 | 162.11 |

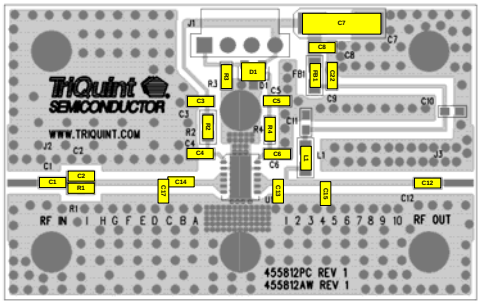
**Device S-parameters are available for download off of the website at: http://www.tqs.com**

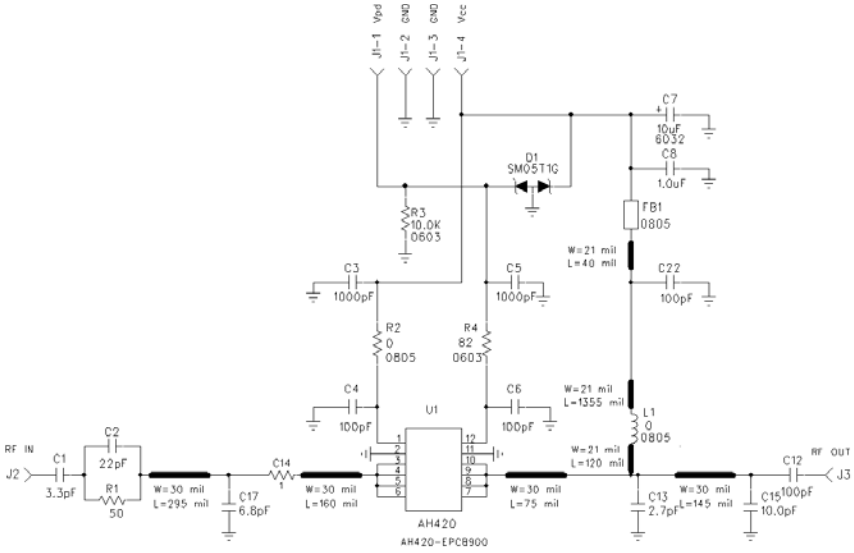
## 920-960 MHz Reference Design (AH420-EPCB900)

**W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.2 dB @ 0.01% Probability, 3.84 MHz BW**

### Typical W-CDMA Performance at 25°C

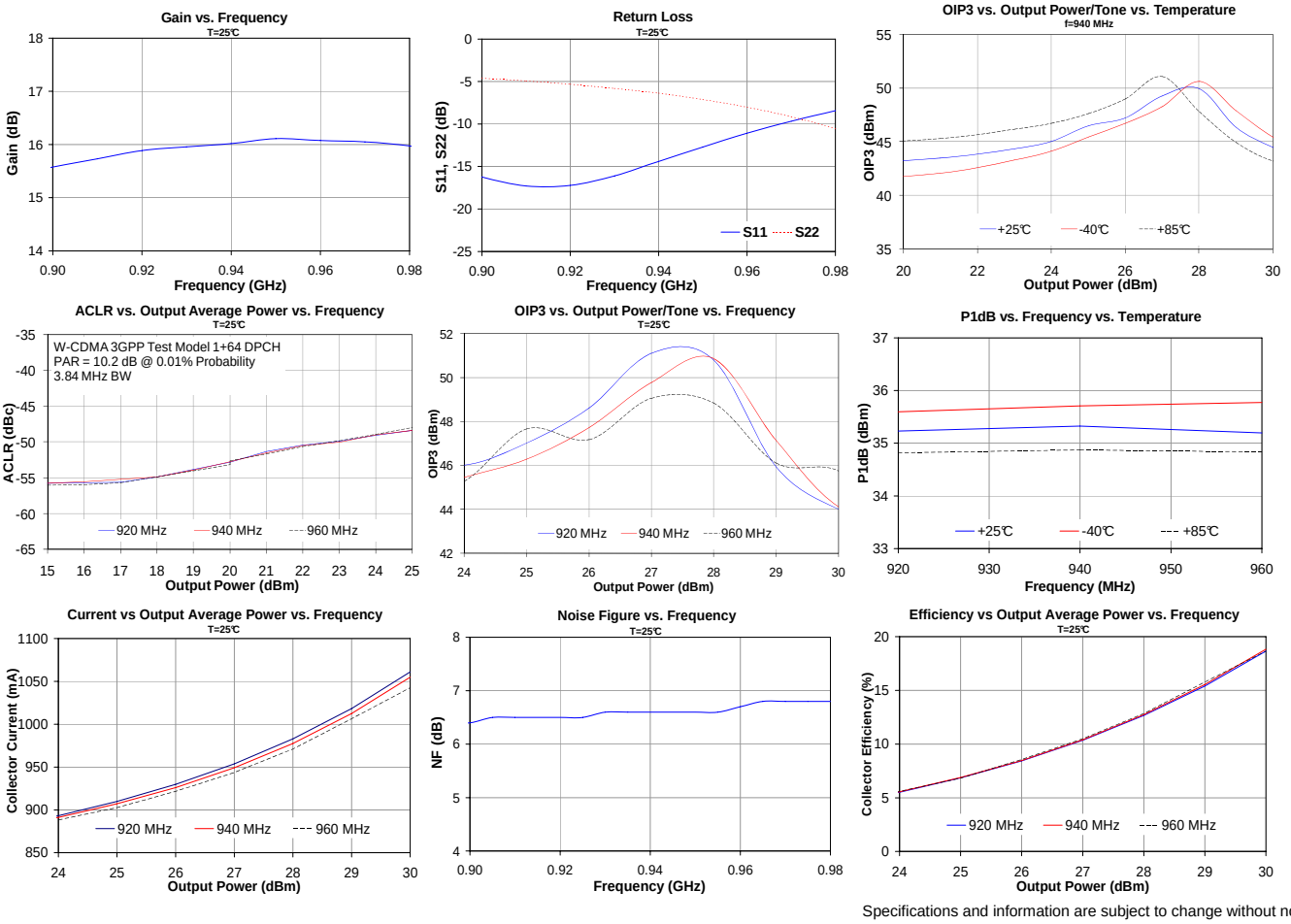
| Frequency (MHz) | 920 | 940 | 960 | Units |
|---|---|---|---|---|
| Channel Power | +27 | +27 | +27 | dBm |
| Power Gain | 15.9 | 16 | 16.1 | dB |
| Input Return Loss | 17 | 14 | 11 | dB |
| Output Return Loss | 5.3 | 6.4 | 8.0 | dB |
| ACLR | -47 | -46.5 | -46.5 | dBc |
| P1dB | +35.2 | +35.2 | +35.2 | dBm |
| Output IP3<br>At 27dBm/tone, 1MHz spacing | +51 | +50 | +49 | dBm |
| Noise Figure | 6.5 | 6.6 | 6.7 | dB |
| Quiescent Current, Icq | 800 | | | mA |
| Vpd, Vcc | +5 | | | V |




Notes:

1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd and Vcc or damage will occur to D1.
3. Components shown on the silkscreen but not on the schematic are not used.
4. Vpd used for device power down (low=RF off)
5. The edge of C13 is placed at 75mil from AH420 RFout pin. (3.9° @ 940 MHz)
6. The edge of C15 is placed 145mil from the edge of C13. (7.5° @ 940 MHz)
7. The edge of C14 is placed at 150mil from AH420 Rfin pin. (7.7° @ 940 MHz)
8. The edge of C17 is placed against the edge of C14.
9. 0 Ω jumpers can be replaced with copper trace in target application.



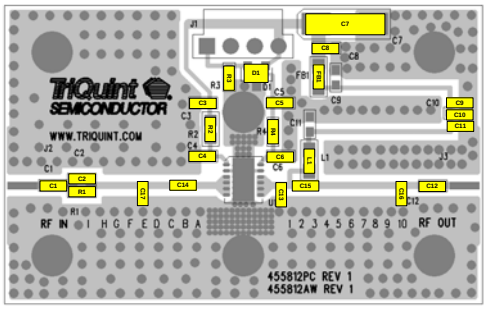

Specifications and information are subject to change without notice

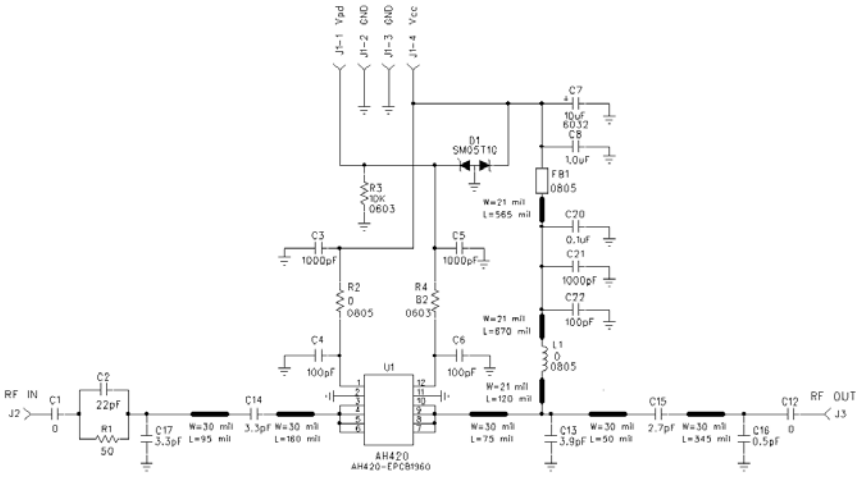
## 1930-1990 MHz Reference Design (AH420-EPCB1960)

**W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.2 dB @ 0.01% Probability, 3.84 MHz BW**

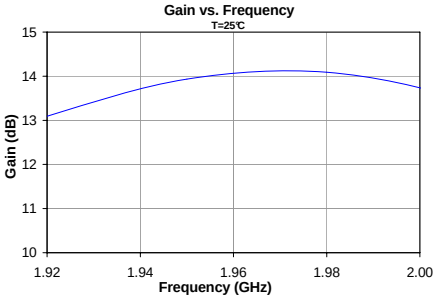
### Typical W-CDMA Performance at 25°C

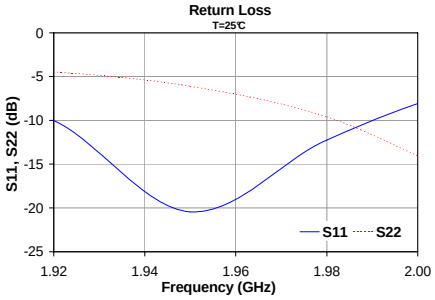
| Frequency (MHz) | 1930 | 1960 | 1990 | Units |
|---|---|---|---|---|
| Channel Power | +27 | +27 | +27 | dBm |
| Power Gain | 13.4 | 14.1 | 14.1 | dB |
| Input Return Loss | 13 | 19 | 11 | dB |
| Output Return Loss | 4.7 | 7 | 12 | dB |
| ACLR | -49 | -48 | -47 | dBc |
| P1dB | +35.6 | +35.6 | +35.6 | dBm |
| Output IP3<br>At 27dBm/tone, 1MHz spacing | +49 | +49 | +49 | dBm |
| Noise Figure | 5.6 | 5.3 | 5.3 | dB |
| Quiescent Current, Icq | 800 | | | mA |
| Vpd, Vcc | +5 | | | V |

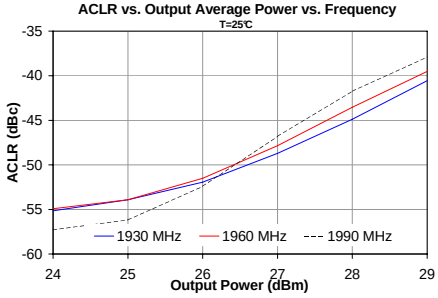


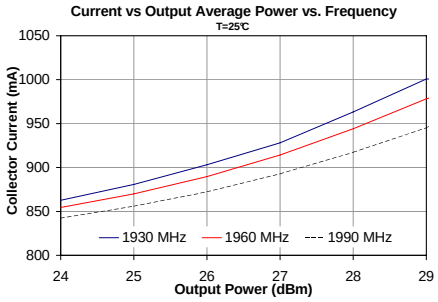



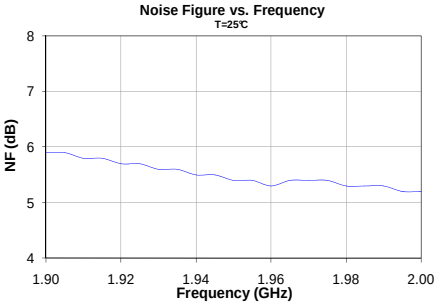

Notes:
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd and Vcc or damage will occur to D1.
3. Components shown on the silkscreen but not on the schematic are not used.
4. Vpd used for device power down (low=RF off)
5. The edge of C13 is placed at 75mil from AH420 RFout pin. (8.0° @ 1960 MHz)
6. The edge of C15 is placed 50mil from the edge of C13. (5.3° @ 1960 MHz)
7. The edge of C16 is placed at 345mil from the edge of C15. (37° @ 1960 MHz)
8. The edge of C14 is placed at 160mil from AH420 Rfin pin. (17.2° @ 1960 MHz)
9. The edge of C17 is placed 95mil from the edge of C14. (10.2° @ 1960 MHz)
10. 0 Ω jumpers can be replaced with copper trace in target application.



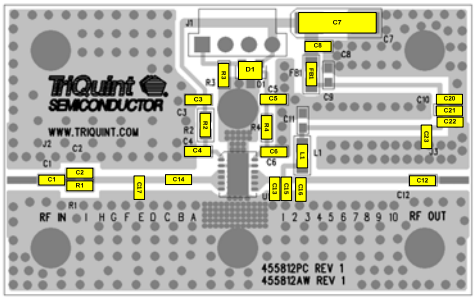



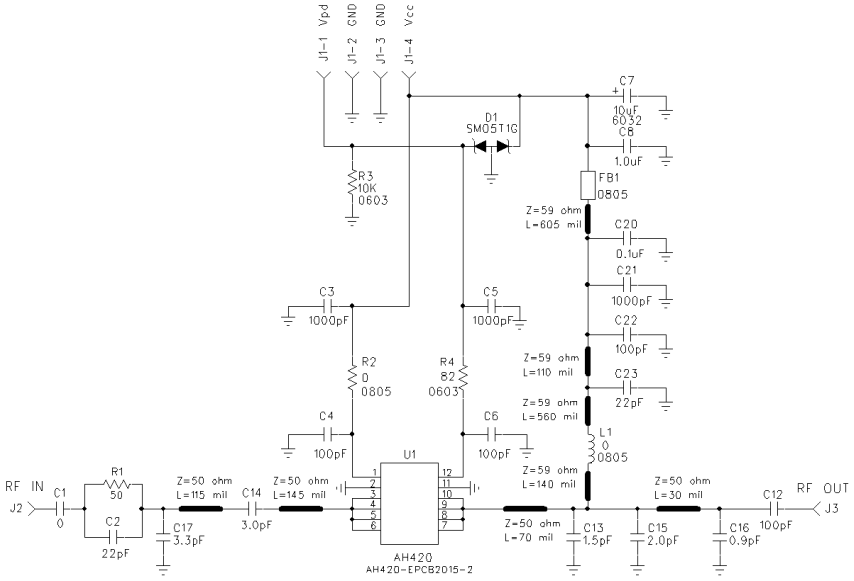
## 2010-2025 MHz Application Circuit Performance Plots

**TD-SCDMA 3 Carrier, PAR = 10 dB @ 0.01% Probability, 1.28 MHz BW**

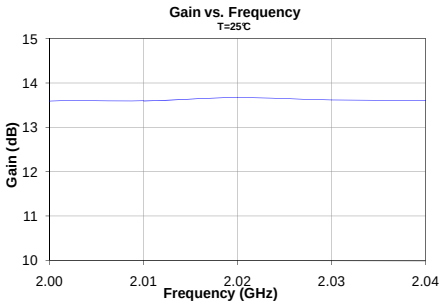
### Typical TD-SCDMA Performance at 25°C

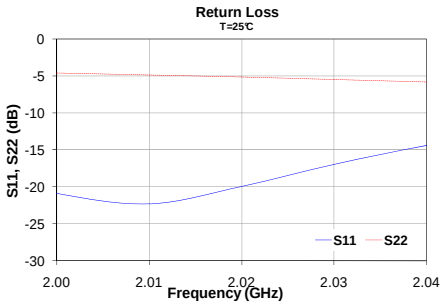
| Frequency (MHz) | 2010 | 2015 | 2025 | Units |
|---|---|---|---|---|
| Channel Power | 24 | 24 | 24 | dBm |
| Power Gain | 13.6 | 13.6 | 13.7 | dB |
| Input Return Loss | 22 | 21 | 20 | dB |
| Output Return Loss | 4.8 | 5 | 5.1 | dB |
| ACLR | -50 | -50 | -50 | dBc |
| P1dB | +34 | +34 | +34 | dBm |
| Output IP3<br>At +25 dBm/tone, 1MHz spacing | +56 | +56 | +55 | dBm |
| Noise Figure | 5.5 | 5.5 | 5.5 | dB |
| Quiescent Current, Icq | 800 | | | mA |
| Vpd | +5 | | | V |
| Vcc | +5 | | | V |

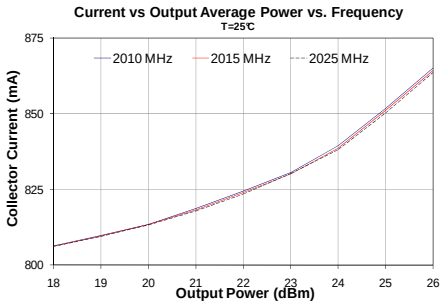


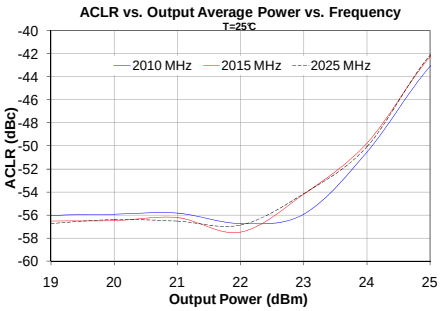




Notes:
1. The primary RF microstrip line is 50 Ω.
2. Components shown on the silkscreen but not on the schematic are not used.
3. The edge of C13 is placed at 70 mil from AH420 RFout pin. (7.7° @ 2015 MHz)
4. The edge of C15 is placed nex to the edge of C13.
5. The edge of C16 is placed 30 mil from the edge of C15. (3.3° @ 2015 MHz)
6. The edge of C14 is placed at 145 mil from AH420 RFin pin. (16° @ 2015 MHz)
7. The edge of C17 is placed 115 mil from the edge of C14. (12.7° @ 2015 MHz)



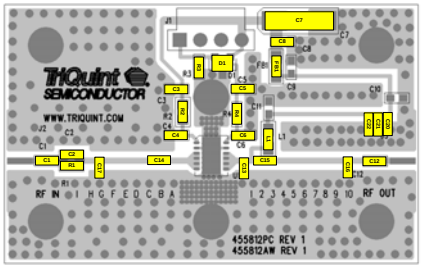



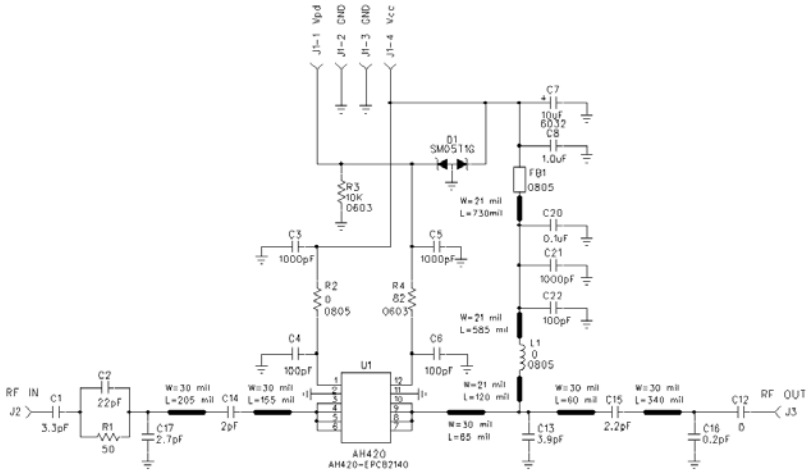
## 2110-2170 MHz Reference Design (AH420-EPCB2140)

**W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10.2 dB @ 0.01% Probability, 3.84 MHz BW**

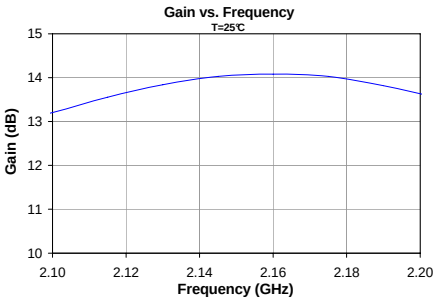
### Typical W-CDMA Performance at 25°C

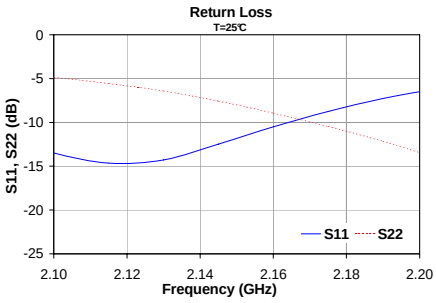
| Frequency (GHz) | 2110 | 2140 | 2170 | Units |
|---|---|---|---|---|
| Channel Power | +26 | +26 | +26 | dBm |
| Power Gain | 13.3 | 14 | 14 | dB |
| Input Return Loss | 14 | 12 | 10 | dB |
| Output Return Loss | 5 | 7.4 | 9 | dB |
| ACLR | -50 | -49 | -50 | dBc |
| P1dB | +35.8 | +35.7 | +35.2 | dBm |
| Output IP3<br>At 27dBm/tone, 1MHz spacing | +49 | +50 | +50 | dBm |
| Noise Figure | 5.8 | 5.6 | 5.5 | dB |
| Quiescent Current, Icq | 800 | | | mA |
| Vpd, Vcc | +5 | | | V |

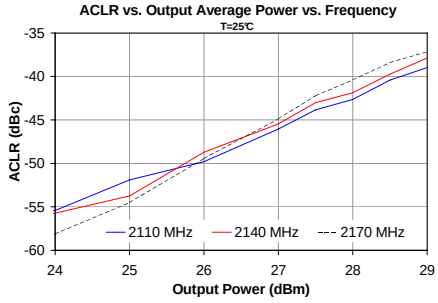


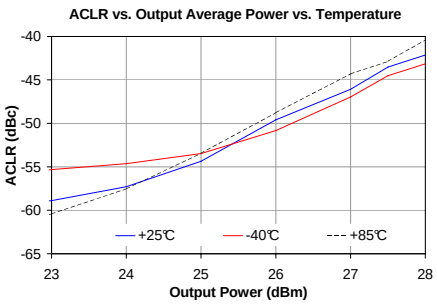



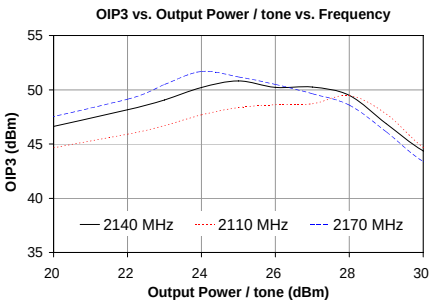

Notes:
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd and Vcc or damage will occur to D1.
3. Components shown on the silkscreen but not on the schematic are not used.
4. Vpd used for device power down (low=RF off)
5. The edge of C13 is placed at 65mil from AH420 RFout pin. (7.6° @ 2140 MHz)
6. The edge of C15 is placed 60mil from the edge of C13. (7.0° @ 2140 MHz)
7. The edge of C16 is placed 340mil from the edge of C15. (39.9° @ 2140 MHz)
8. The edge of C14 is placed at 155mil from AH420 RFin pin. (18.2° @ 2140 MHz)
9. The edge of C17 is placed 205mil from the edge of C14. (24.0° @ 2140 MHz)
10. 0 Ω jumpers can be replaced with copper trace in target application.

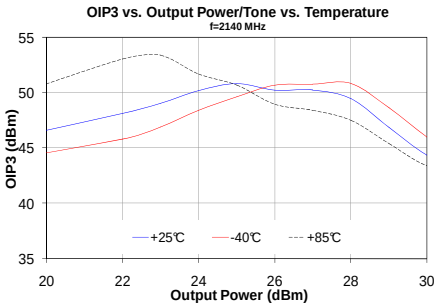


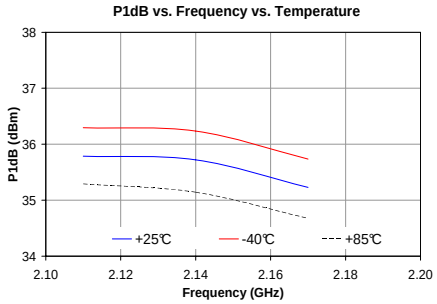



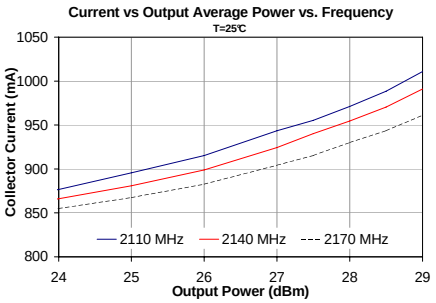



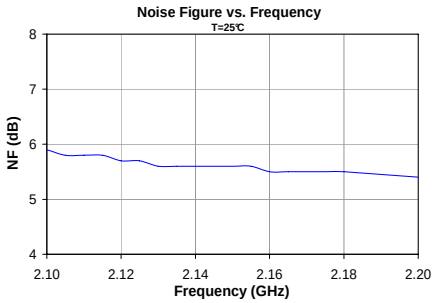



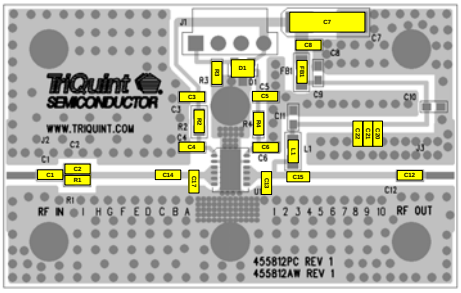

Specifications and information are subject to change without notice

## 2.3-2.4 GHz Application Circuit Performance Plots

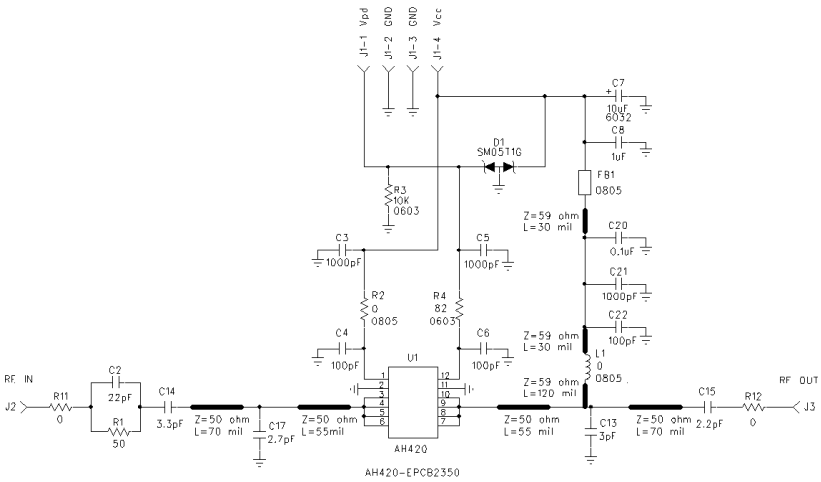
**802.16-2004 O-FDMA, 64QAM-1/2, 1024-FFT, 20 symbols and 30 subchannels, 5 MHz Carrier BW**

### Typical O-FDMA Performance at 25°C

| Frequency (GHz) | 2.3 | 2.35 | 2.4 | Units |
|---|---|---|---|---|
| Channel Power | +27 | +27 | +27 | dBm |
| Gain | 12.8 | 13.2 | 13.6 | dB |
| Input Return Loss | 18 | 16 | 13 | dB |
| Output Return Loss | 4 | 5.2 | 7.3 | dB |
| EVM | 2 | 1.9 | 2 | % |
| Operating Current, Icc | 955 | 920 | 890 | mA |
| Collector Efficiency | 10.4 | 11 | 11 | % |
| Quiescent Current, Icq | 800 | | | mA |
| Vcc, Vpd | +5 | | | V |

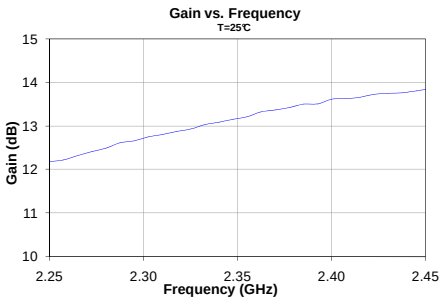


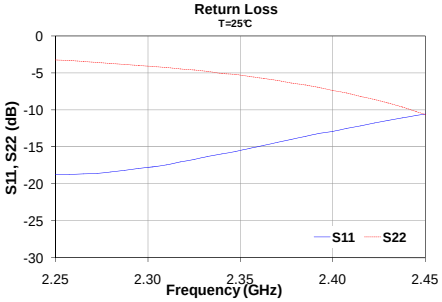

Circuit Board Material: 0.014" GETEK, single layer, 1 oz copper, $\varepsilon_r$ = 4.2, Microstrip line details: width = .030", spacing = .030"

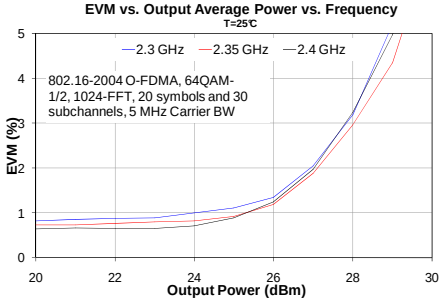


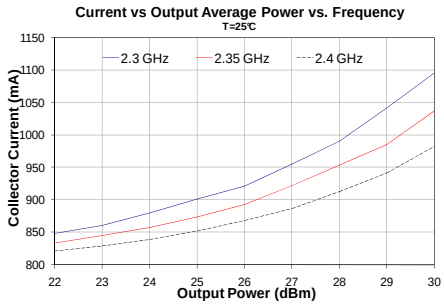

Notes:

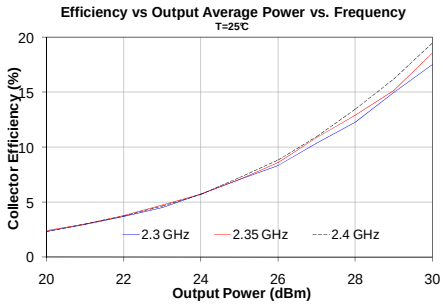
1. The primary RF microstrip line is 50 Ω.
2. Do not exceed 5.5V on Vpd or Vcc or damage to D1 will occur.
3. Components shown on the silkscreen but not on the schematic are not used.
4. C1 & C12 can be replaced with a copper trace.
5. 0 Ω jumpers can be replaced with copper trace in target application.
6. The edge of C17 is placed 55 mil from the AH420 RFin pin. (7.1° @ 2.35 GHz)
7. The edge of C14 is placed 70 mil from the edge of C17. (9.0° @ 2.35 GHz)
8. The edge of C13 is placed 55 mil from the AH420 RFout pin. (7.1° @ 2.35 GHz)
9. The edge of C15 is placed 70 mil from the edge of C13. (9.0° @ 2.35 GHz)

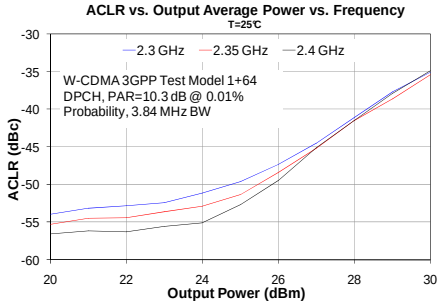


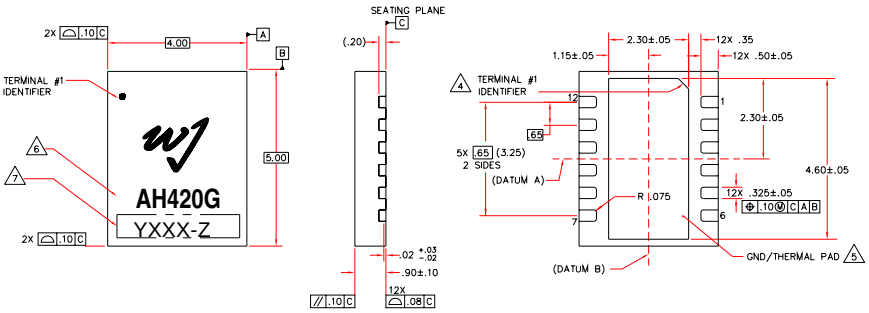



## Mechanical Information

This package is lead-free/green/RoHS-compliant. The plating material on the backside metallization is Matte Tin. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

## Outline Drawing

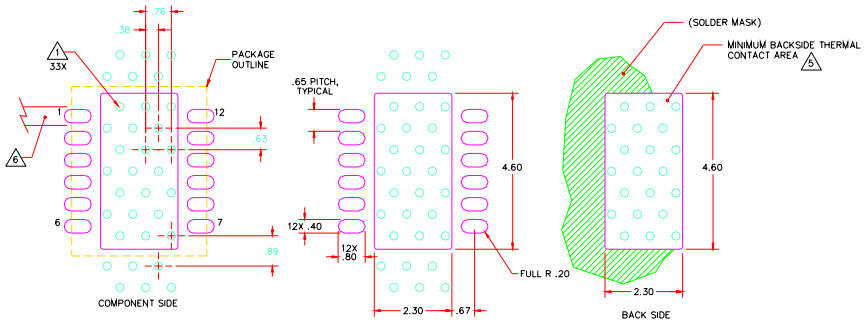



NOTES:

1. EXCEPT WHERE NOTED, THIS PART OUTLINE CONFORMS TO JEDEC STANDARD MO-229, ISSUE C (VARIATION VJGC) FOR THERMALLY ENHANCED PLASTIC VERY THIN FINE PITCH QUAD FLAT NO LEAD PACKAGE (QFN).
2. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.4M-1994.
3. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.

4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION CONFORM TO JESD 95-1 SPP-012.
5. COPLANARITY APPLIES TO THE EXPOSED GROUND/THERMAL PAD AS WELL AS THE TERMINALS.
6. PART NUMBER
7. ALPHA-NUMERIC LOT CODE.

## Mounting Configuration / Land Pattern




Notes:

1. A heatsink underneath the area of the PCB for the mounted device is recommended for proper thermal operation. Damage to the device can occur without the use of one.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.
4. Mounting screws can be added near the part to fasten the board to a heatsink. Ensure that the ground / thermal via region contacts the heatsink.
5. Do not put solder mask on the backside of the PC board in the region where the board contacts the heatsink.
6. RF trace width depends upon the PC board material and construction.
7. Use 1 oz. Copper minimum.
8. All dimensions are in millimeters

## Product Marking

The AH420 will be marked with an "AH420G" designator with a lot code marked below the part designator. The "Y" represents the last digit of the year the part was manufactured, the "XXX" is an auto-generated number, and "Z" refers to a wafer number in a lot batch.

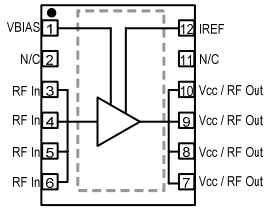
Tape and reel specifications for this part are located on the website in the "Application Notes" section.

## ESD / MSL Information

**Caution!** ESD sensitive device.

| | |
|---|---|
| ESD Rating: | Class 1A |
| Value: | Passes ≥250V to <500V |
| Test: | Human Body Model (HBM) |
| Standard: | JEDEC Standard JESD22-A114 |
| ESD Rating: | Class IV |
| Value: | Passes ≥ 1000V min. |
| Test: | Charged Device Model (CDM) |
| Standard: | JEDEC Standard JESD22-C101 |
| MSL Rating: | Level 3 at +260 °C convection reflow |
| Standard: | JEDEC Standard J-STD-020 |

## Functional Pin Layout




| Pin | Function |
|---|---|
| 1 | VBIAS |
| 2, 11 | No Connect |
| 3, 4, 5, 6 | RF Input |
| 7, 8, 9, 10 | VCC / RF Output |
| 12 | IREF |