TQP8M9013

½ W High Linearity 5V 2-Stage Amplifier

Applications

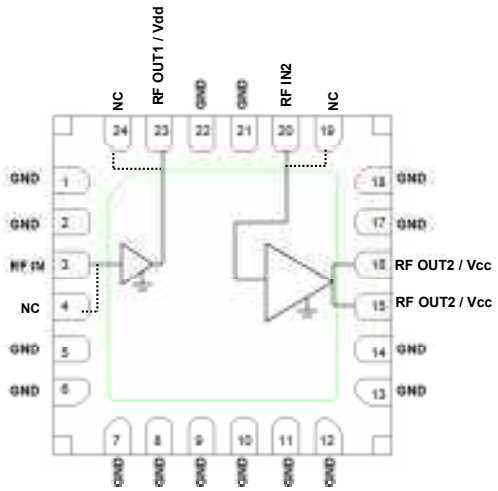
- Repeaters
- Mobile Infrastructure
- LTE / WCDMA / CDMA / EDGE

24-pin 4x4mm leadless QFN package

Product Features

- 700-3800 MHz
- 29.5 dB Gain @ 2140 MHz
- +28 dBm P1dB
- +44 dBm Output IP3
- 2.9 dB Noise Figure
- +5V Supply Voltage
- MTTF > 1000 Years

Functional Block Diagram



General Description

The TQP8M9013 is a high dynamic range two-stage driver amplifier in a low-cost surface-mount package. The amplifier is able to achieve high performance across a broad range with +44 dBm OIP3, +28 dBm P1dB, and 2.9 dB Noise Figure while drawing 225 mA current at 2140 MHz. The product consists of a high linearity, low noise amplifier stage, followed by a ½W high linearity driver amplifier.

The TQP8M9013 is available in a standard lead-free /green/RoHS-compliant 24-pin 4x4mm QFN package. All devices are 100% RF and DC tested.

The TQP8M9013 is targeted for use as a driver amplifier in wireless infrastructure where high linearity, medium power, and high efficiency are required. Internal biasing allows the amplifier to maintain high linearity over temperature and operate directly off a single +5V supply. This combination makes the device an excellent candidate for transceiver line cards in current and next generation multi-carrier 3G/4G base stations or repeaters.

Pin Configuration

Pin #	Symbol
3	Amp1 RF Input
15, 16	Amp2 RF Output / Vcc
20	Amp2 RF Input
23	Amp1 RF Output / Vdd
Pins 4, 19, and 24 are N/C internally, but may be connected as signal pins on the PCB.	
All other pins are N/C internally.	

Ordering Information

Part No.	Description
TQP8M9013	½W 5V 2-stage Amplifier
TQP8M9013-PCB900	900 MHz Evaluation Board
TQP8M9013-PCB2140	2140 MHz Evaluation Board

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Storage Temperature	-65 to 150 °C
RF Input Power, CW, 50Ω,T = 25°C	+10 dBm
V_{dd}, Amp Stage 1	+5.5 V
V_{cc}, Amp Stage 2	+8.0 V
Thermal Resistance (jnc. to case) θ_{jc} Amp Stage 1	76.3 °C/W
Thermal Resistance (jnc. to case) θ_{jc} Amp Stage 2	64.3 °C/W

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V_{cc}		5	6.0	V
V_{dd}		4.5	5.0	V
T (case)	-40		85	°C
T_J Amp 1			160	°C
T_J Amp 2			200	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.
T_J (Max Junction Temperature) maintain MTTF ≥ 10^6 hours

Electrical Specifications

Test conditions: 25ºC, +5V V_{cc}, V_{dd} supplied through +5V with 6.2Ω dropping resistor on tuned application circuit for 2350 MHz shown on Page 14.

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		700		3800	MHz
Test Frequency			2350		MHz
Gain		25.5	28.4	30	dB
Input Return Loss			-15		dB
Output Return Loss			-10		dB
Output P1dB		+26.5	+27.5		dBm
Output IP3	See Note 1.	+38	+42		dBm
Channel Power @ -50 dBc ACLR	See Note 2.		+18		dBm
Noise Figure			2.9		dB
Supply Voltage, Vcc			+5		V
Quiescent Current, Icq		180	225	265	mA

Notes:
1. OIP3 is measured with two tones separated by 1 MHz at 11dBm output power/tone. The suppression on the largest IM3 product is used to calculate the OIP3 using a 2:1 rule.
2. Signal: W-CDMA 3GPP Test Model 1+64 DPCH, PAR = 10 dB @ 0.01% Probability, 3.84 MHz BW

Performance Summary Table

Test conditions unless otherwise noted: +25ºC, +5V Vcc, 225 mA Icq, in an application circuit tuned for each frequency.

Frequency	800	900	1500	2140	2350	2600	3500	MHz
Gain	29.5	29.8	24.5	29.7	28.4	26.8	22.4	dB
Input Return Loss	13.1	12.9	15.5	13.1	15.0	11.5	13.0	dB
Output Return Loss	21.2	23.9	13.0	10.7	10.0	19.4	10.8	dB
Output P1dB	+28.4	+29.0	+28.7	+28.0	+27.5	+27.7	+27.7	dBm
Output IP3 [4]	+41	+40	+40.2	+43.4	+41.6	+41.2	+38.0	dBm
WCDMA Channel Power @ -50 dBc ACLR	+17.7	+18.8	+19.5	+18.5	+18.5	+17.9	+18.0	dBm

Notes:
1. OIP3 is measured at 12 dBm Pout / tone with 1 MHz spacing between two tones.
2. 1500 MHz represents data with an interstage resistive attenuation pad in order to target lower gain (24.5 dB).

Design Reference Circuits using TQP8M9013

Amplifier Stage 1

TQP8M9013 first amplifier stage consists of a high linearity, low noise amplifier, which is also available by TriQuint as packaged component solution called the AM1-G. This high dynamic range gain block uses GaAs MESFET technology. This amplifier stage is internally matched and offers maximum linearity into 50 Ω load impedance. It does not require any external matching. For TQP8M9013, the input return loss for a frequency band can be further optimized depending on customer requirements by applying a conjugate match at the input of first stage amplifier. De-embedded s-parameters for this stage are available off of TriQuint website.

Typical Performance of Stage 1 Amplifier

Parameter	Units		
Frequency	MHz	900	1900
Gain	dB	14	12.8
Input Return Loss	dB	10	9
Output Return Loss	dB	27	22
Output P1dB	dBm	18	18
Output IP3	dBm	39	39
Noise Figure	dB	2.4	2.6
Device Voltage	V	4.5	
Current	mA	78	

Amplifier Stage 2

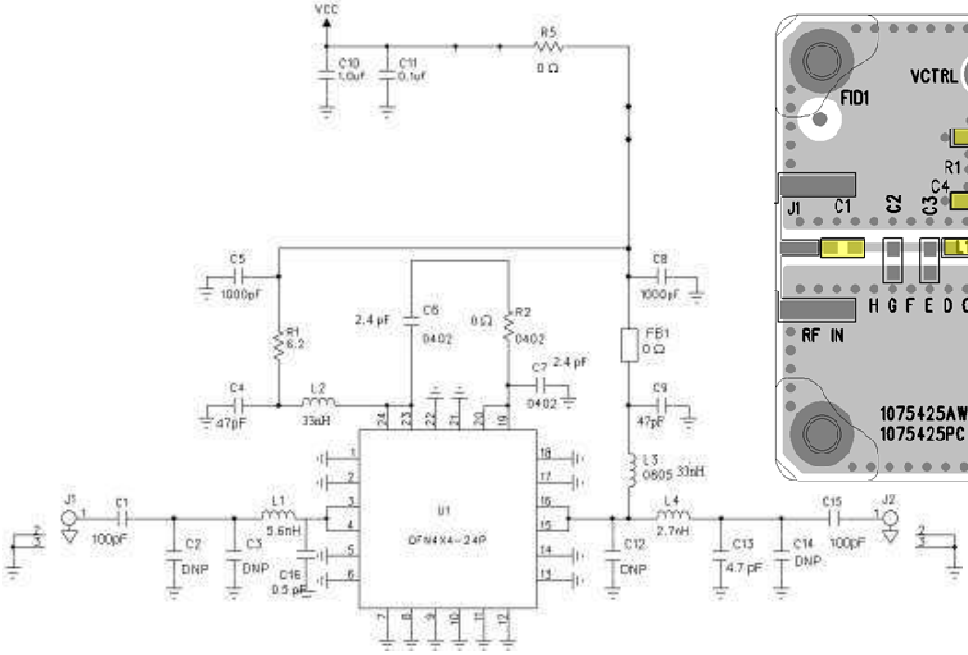
The second stage of the TQP8M9013 is a ½W InGaP/GaAs HBT linear amplifier, which is also available by TriQuint as a packaged component solution called the AH125-89G. In a design that is optimized for input return loss, gain flatness, and linearity, the second stage offers 20 dB gain at 900 MHz and 16.2 dB at 2.14 GHz, as shown in the Table below. For optimum performance, impedance matching circuit at the input and output of Stage 2 amplifier is required. Optimizing a matching network in order to meet all the design specifications may require multiple iterations and with aid of the de-embedded s-parameters in a circuit simulator, it can become less tedious. The de-embedded S-parameter for second stage amplifier can be downloaded off of TriQuint website.

Typical Performance of Stage 2 Amplifier

Parameter	Units			
Frequency	MHz	920	1960	2140
Gain	dB	20	17	16.2
Input Return Loss	dB	20	16	12
Output Return Loss	dB	9.9	9	12
W-CDMA Channel Power @ -50 dBc ACLR	dBm	19	19	19
Output P1dB	dBm	28.1	27.8	28
Output IP3 (4)	dBm	47	47	45
Noise Figure	dB	7.7	4.6	4.4
Device Voltage	V	5		
Quiescent Current	mA	150		

Reference Design 800-1000 MHz (TQP8M9013-PCB900)

Represents data tuned for gain and optimum linearity across the band.



Notes:

1. The distance from U1 device package to the edge of component L4 is 185 mils or E.L. of 9.2° at 0.9 GHz.
2. C13 is placed against the edge of L4.
3. The distance from U1 device package to the edge of C16 is 70 mils or E.L. of 3.5° at 0.9 GHz
4. For always ON applications, control circuitry R3, R4, Q1 are removed and placed 0 Ω jumper at R5.

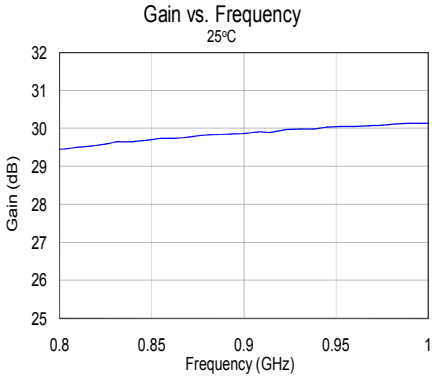
Bill of Material

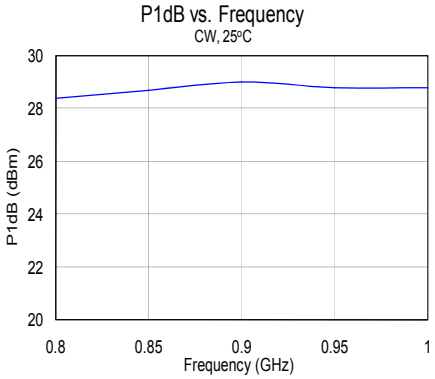
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		2-Stage Driver Amplifier	TriQuint	TQP8M9013
C6, C7	2.4 pF	Cap, Chip, 0402, 25V, +/-0.1pF	AVX	04023J2R4BBS
C9, C4	47 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C1, C15	100 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C5, C8	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C11	0.1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
C10	1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
L3	33 nH	Coil, Wire Wound, 0805, RoHS, 5%	Coilcraft	0805CS-33NXJL_
L2	33 nH	Coil, Wire Wound, 0603, RoHS, 5%	Coilcraft	0603CS-39NXJL_
R1	6.2 Ω	Resistor, Chip, 0603, 5%, 50V	various	
R2	0 Ω	Resistor, Chip, 0402, 5%, 50V	various	
FB1, R5	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C13	4.7 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J4R7BSTR
C16	0.5 pF	Cap, Chip, 0603, 50V, +/-0.05pF	AVX	06035J0R5BSTR
L4	2.7 nH	Ind, Chip, 0603, +/-0.5nH, RoHS	Toko	LL1608-FSL2N7S
C2, C3, C12, C14, R3, R4, Q1		Do Not Place		
L1	5.6 nH	Ind, Chip, 0603, +/-0.5nH, RoHS	Toko	LL1608-FSL5N6S

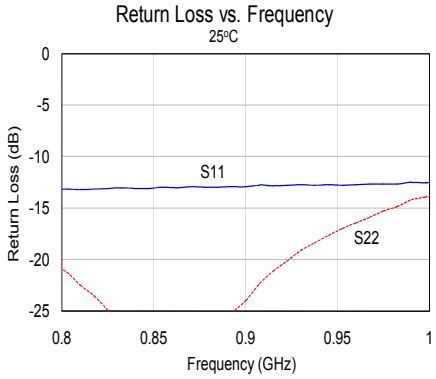
Typical Performance 800-1000 MHz (TQP8M9013-PCB900)

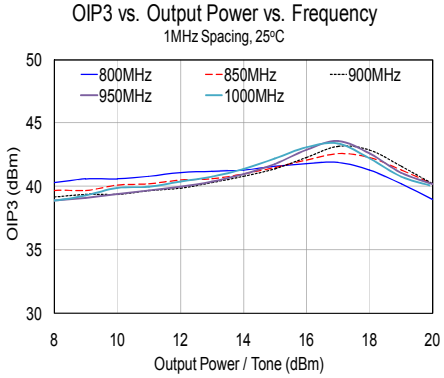
Frequency	MHz	800	850	900	950	1000
Gain [1]	dB	29.5	29.7	29.8	30.0	30.1
Input Return Loss	dB	13.1	13.1	12.9	12.7	12.4
Output Return Loss	dB	21.2	30.0	23.9	17.6	13.5
Output P1dB	dBm	+28.4	+28.7	+29.0	+28.8	+28.8
OIP3 [2]	dBm	+41.9	+42.6	+43.0	+43.3	+43.4
Channel Power @ -50 dBc ACLR [3]	dBm	+17.7	+18.1	+18.8	+18.4	+18.1
Quiescent Current, Icq	mA	225				
Supply Voltage, Vcc	V	+5				

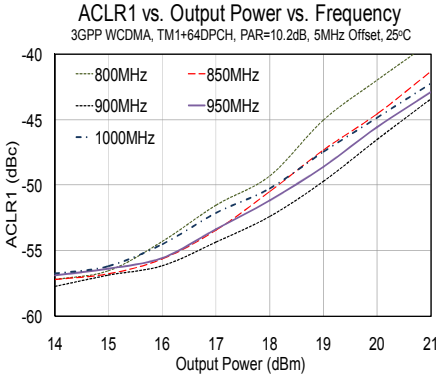
Notes
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 17 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.





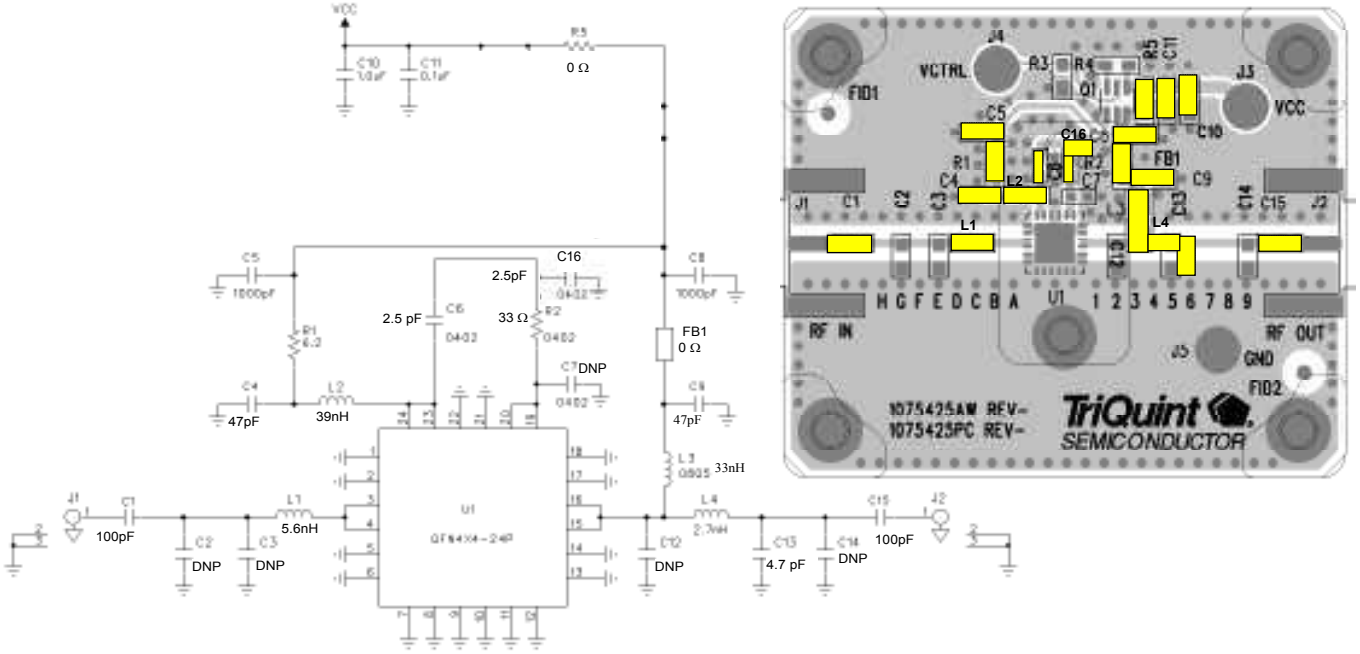






Reference Design 850-900 MHz (24.5 dB Gain)

Represents data with an interstage resistive attenuation pad in order to target lower gain (24.5dB) across the band. OIP3 is slightly degraded due to this configuration.



Notes:

1. The distance from U1 device package to the edge of component L4 is 185 mils or E.L. of 9.2° at 0.9 GHz.
2. C13 is placed against the edge of L4.
3. The distance between C16 and location of R2 is 15mils on the interstage matching circuit.
4. For always ON applications, control circuitry R3, R4, Q1 are removed and placed 0 Ω jumper at R5.

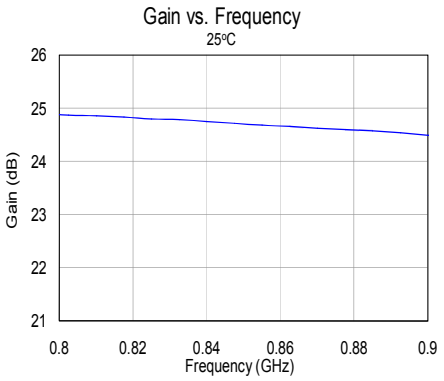
Bill of Material

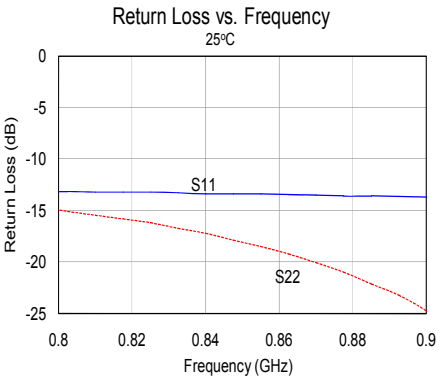
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		2-Stage Driver Amplifier	TriQuint	TQP8M9013
C6, C16	2.5 pF	Cap, Chip, 0402, 25V, +/-0.1pF	AVX	04023J2R5BBS
C9, C4	47 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C1, C15	100 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C5, C8	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C11	0.1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
C10	1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
L3	33 nH	Coil, Wire Wound, 0805, RoHS, 5%	Coilcraft	0805CS-33NXJL_
L2	39 nH	Coil, Wire Wound, 0603, RoHS, 5%	Coilcraft	0603CS-39NXJL_
R1	6.2 Ω	Resistor, Chip, 0603, 5%, 50V	various	
R2	33 Ω	Resistor, Chip, 0402, 5%, 50V	various	
FB1, R5	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C13	4.7 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J4R7BSTR
L4	2.7 nH	Ind, Chip, 0603, +/-0.5nH, RoHS	Toko	LL1608-FSL2N7S
C2, C3, C7, C12, C14, R3, R4, Q1		Do Not Place		
L1	5.6 nH	Ind, Chip, 0603, +/-0.5nH, RoHS	Toko	LL1608-FSL5N6S

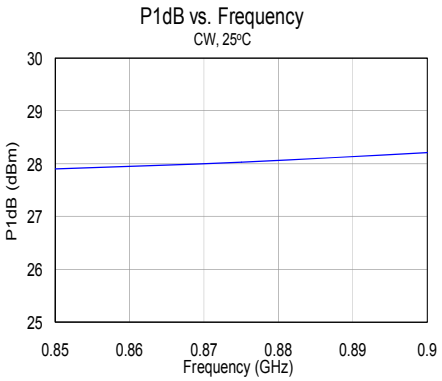
Typical Performance 850-900 MHz (24.5 dB Gain)

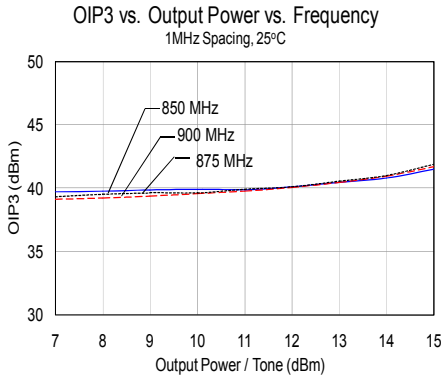
Frequency	MHz	850	875	900
Gain [1]	dB	24.8	24.7	24.6
Input Return Loss	dB	13.3	13.5	13.6
Output Return Loss	dB	17.5	20.0	23.0
Output P1dB	dBm	+28	+28	+28.2
OIP3 [2]	dBm	+39.5	+39.5	+39.5
Channel Power @ -50 dBc ACLR [3]	dBm	+18.5	+18.5	+18.7
Channel Power @ 2.5% EVM [4]	dBm	+20	+20	+20.5
Quiescent Current, Icq	mA		225	
Supply Voltage, Vcc	V		+5	

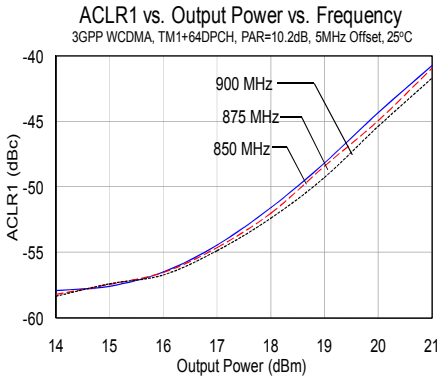
Notes
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 11 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.
4. EVM Test-setup: 802.16-2004 OFDMA, 64QAM-1/2, 1024-FFT, 20 symbols, 30 subchannels.

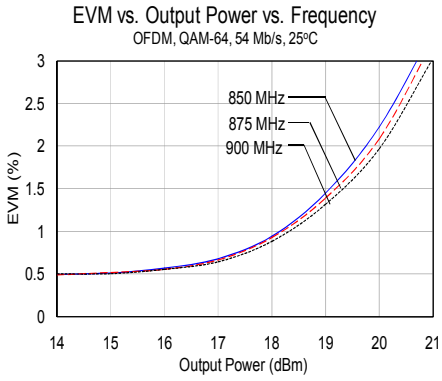






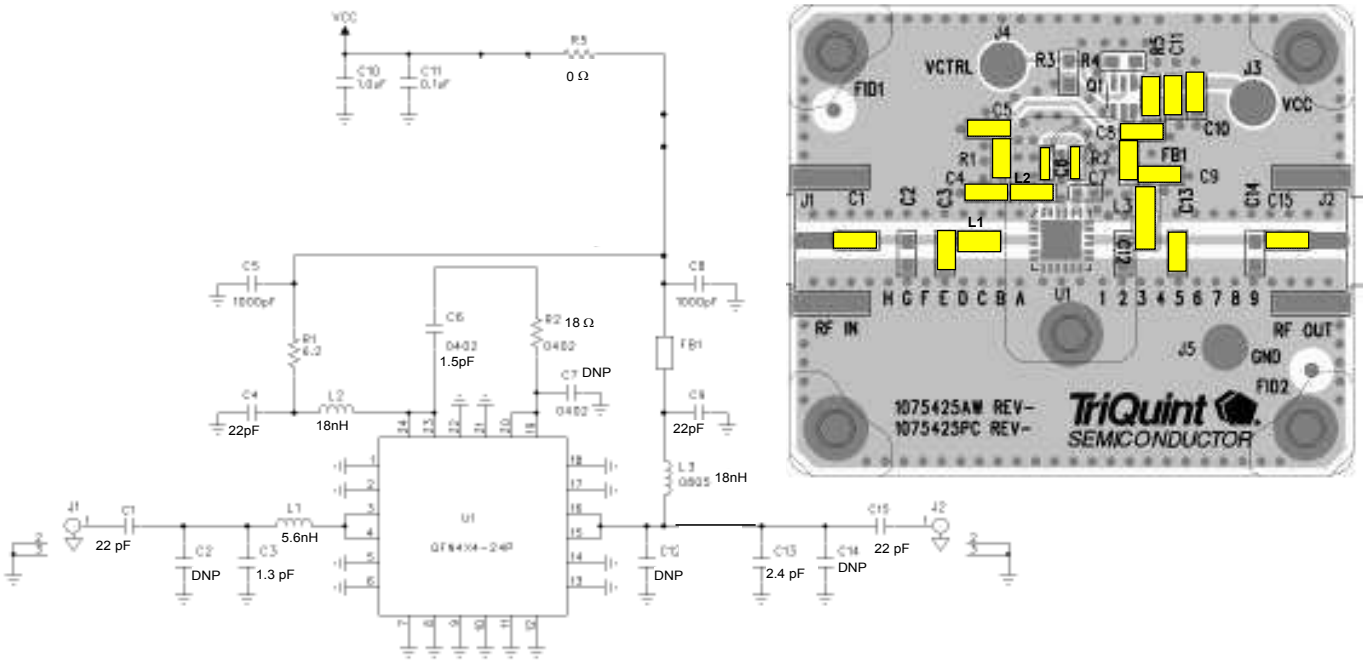






Reference Design 1475-1510 MHz

Represents data with an interstage resistive attenuation pad in order to target lower gain across the band.



Notes:
1. C13 is placed at location '5' on the TQS application board or E.L. of 18.2° at 1.5 GHz from the device RFout pin.
2. L1 is placed at E.L. of 10.7° at 1.5 GHz from the device RFin pin.
3. C3 is placed at location 'E' on the TQS application board or E.L. of 18.2° at 1.5 GHz from the device RFin pin.
4. For always ON applications, control circuitry R3, R4, Q1 are removed and placed 0 Ω jumper at R5.

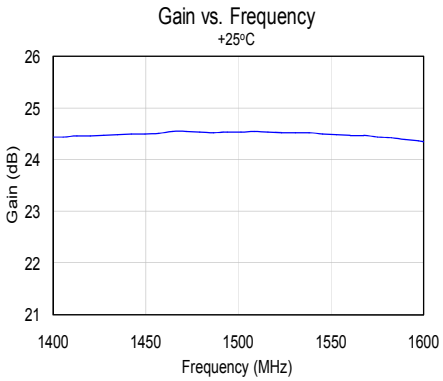
Bill of Material

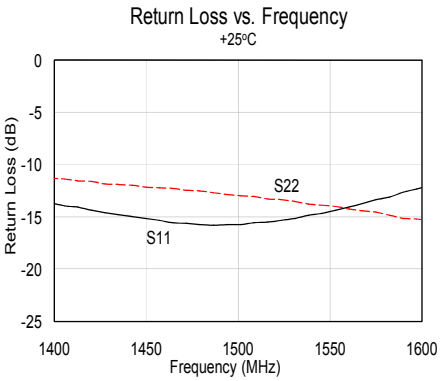
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		2-Stage Driver Amplifier	TriQuint	TQP8M9013
C6	1.5 pF	Cap, Chip, 0402, 25V, +/-0.1pF	AVX	04023J1R5BBS
C9, C4, C1, C15	22 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C5, C8	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C11	0.1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
C10	1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
L3	18 nH	Coil, Wire Wound, 0805, RoHS, 5%	Coilcraft	0805CS-18NXJL_
L2	18 nH	Coil, Wire Wound, 0603, RoHS, 5%	Coilcraft	0603CS-18NXJL_
R1	6.2 Ω	Resistor, Chip, 0603, 5%, 50V	various	
R2	18 Ω	Resistor, Chip, 0402, 5%, 50V	various	
FB1, R5	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C13	2.4 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J2R4BSTR
C3	1.3 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J1R3BSTR
C2, C12, C14, C7, R3, R4, Q1		Do Not Place		
L1	5.6 nH	Ind, Chip, 0603, +/-0.5nH, RoHS	Toko	LL1608-FSL5N6S

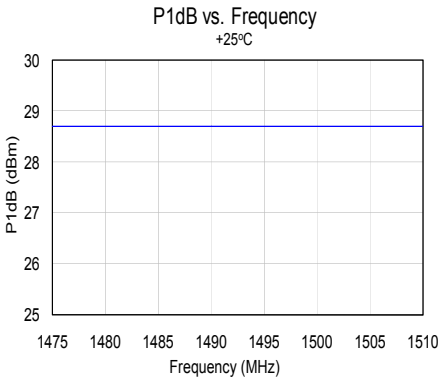
Typical Performance 1475-1510 MHz

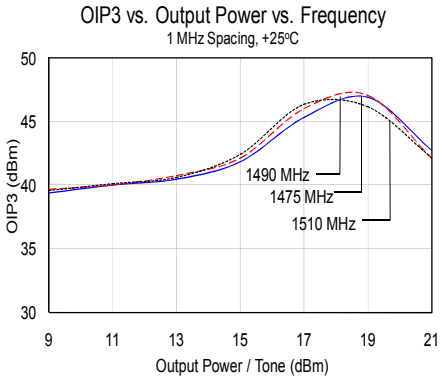
Frequency	MHz	1475	1490	1510
Gain [1]	dB	24.5	24.5	24.5
Input Return Loss	dB	15.7	15.8	15.5
Output Return Loss	dB	12.5	12.8	13.0
Output P1dB	dBm	+28.5	+28.5	+28.5
OIP3 [2]	dBm	+40	+40	+40
Channel Power @ -50 dBc ACLR [3]	dBm	+19.5	+19.5	+19.6
Channel Power @ 2.5% EVM [4]	dBm	+21	+21	+21
Quiescent Current, Icq	mA	225		
Supply Voltage, Vcc	V	+5		

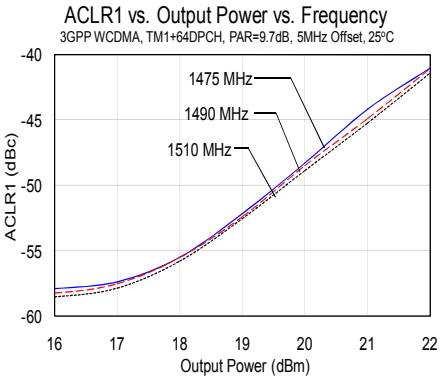
Notes:
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 11 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.
4. EVM test-setup: 802.16-2004 OFDMA, 64QAM-1/2, 1024-FFT, 20 symbols, 30 subchannels.

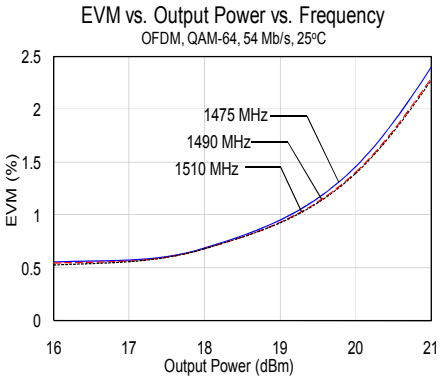






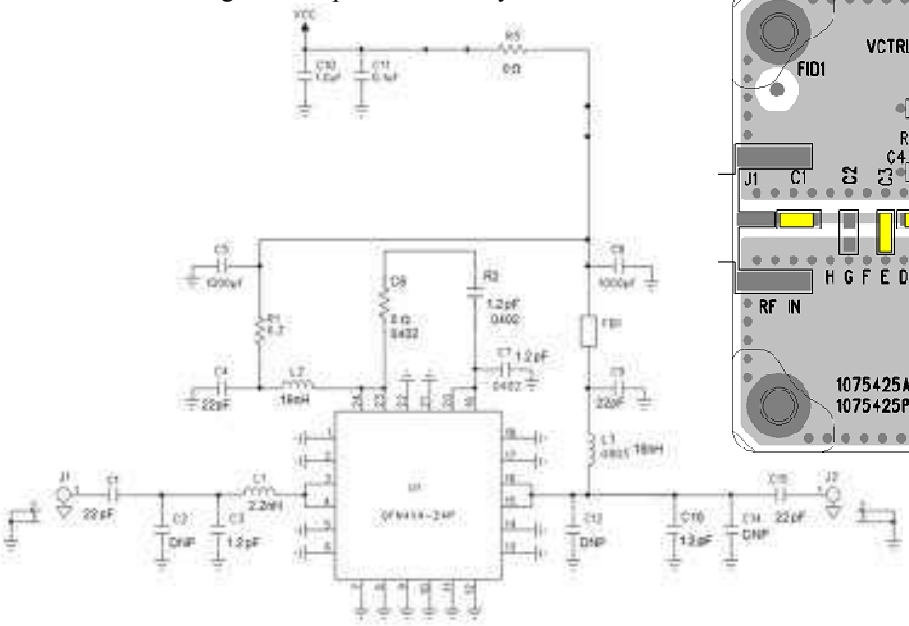


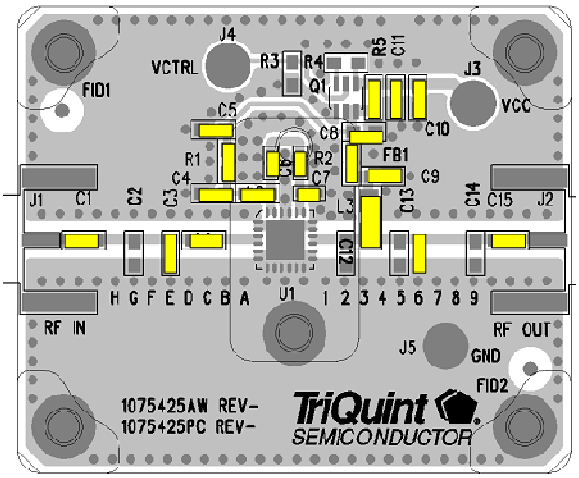




Reference Design 2110-2170 MHz (TQP8M9013-PCB2140)

Represents data tuned for gain and optimum linearity across the band.





1. The distance from U1 device package to the edge of C16 is 266 mils or E.L. of 31.4° at 2.14 GHz.
2. The distance from U1 device package to the edge of C3 is 210 mils or E.L. of 24.7° at 2.14 GHz.
3. For always ON applications, control circuitry R3, R4, Q1 are removed and placed 0 Ω jumper at R5.

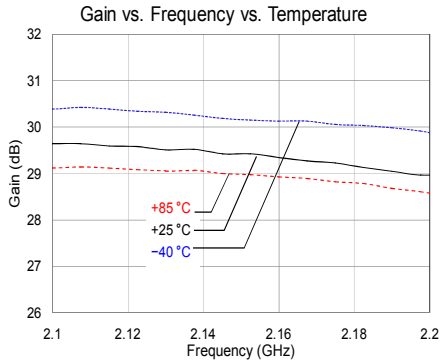
Bill of Material

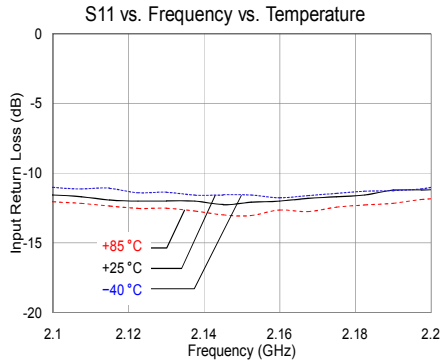
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		2-Stage Driver Amplifier	TriQuint	TQP8M9013
C6	0 Ω	Resistor, Chip, 0402, 5%, 50V	various	
C9, C4, C1, C15	22 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C5, C8	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C11	0.1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
C10	1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
L3	18 nH	Coil, Wire Wound, 0805, RoHS, 5%	Coilcraft	0805CS-18NXJL_
L2	18 nH	Coil, Wire Wound, 0603, RoHS, 5%	Coilcraft	0603CS-18NXJL_
R1	6.2 Ω	Resistor, Chip, 0603, 5%, 50V	various	
R2, C7	1.2 pF	Cap, Chip, 0402, 25V, +/-0.1pF	AVX	04023J1 R2BBS
FB1, R5	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C3, C16	1.2 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J1R2BSTR
C2, C12, C14, R3, R4, Q1		Do Not Place		
L1	2.2 nH	Ind, Chip, 0603, +/-0.5nH, RoHS	Toko	LL1608-FSL2N2S

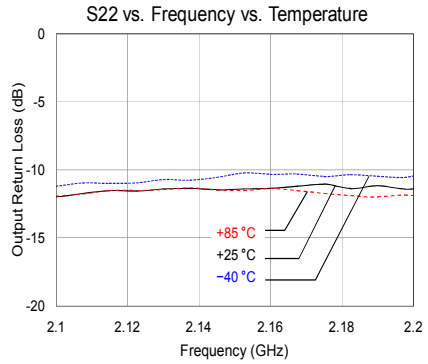
Typical Performance 2110-2170 MHz (TQP8M9013-PCB2140)

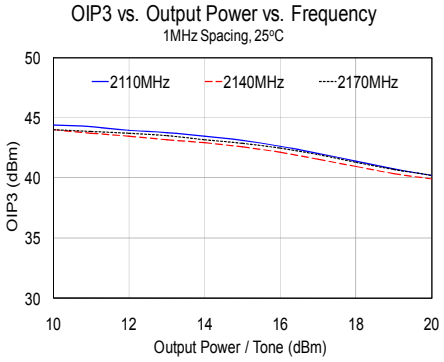
Frequency	MHz	2110	2140	2170
Gain [1]	dB	29.8	29.7	29.4
Input Return Loss	dB	13.2	13.1	12.1
Output Return Loss	dB	10.8	10.7	10.5
Output P1dB	dBm	+28.0	+28.0	+28.1
OIP3 [2]	dBm	+44.2	+43.7	+43.8
Channel Power @ -50 dBc ACLR [3]	dBm	+18.4	+18.5	+18.6
Quiescent Current, Icq	mA		225	
Supply Voltage, Vcc	V		+5	

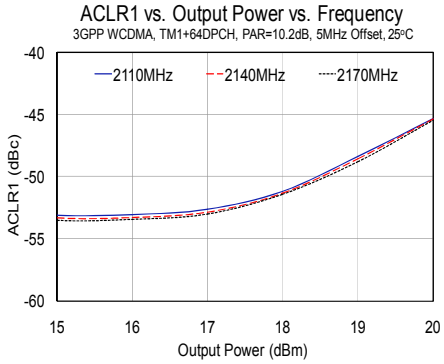
Notes:
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 11 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.

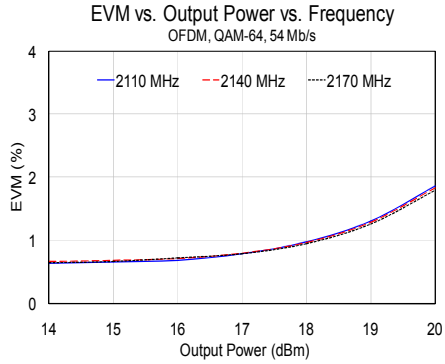


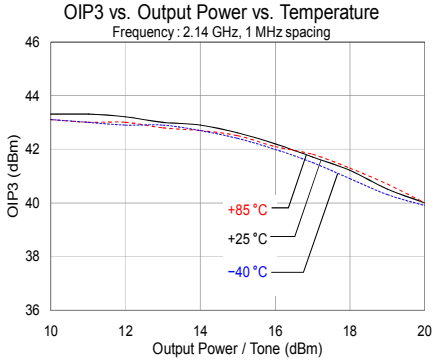


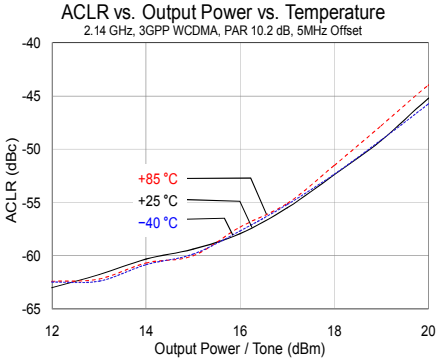


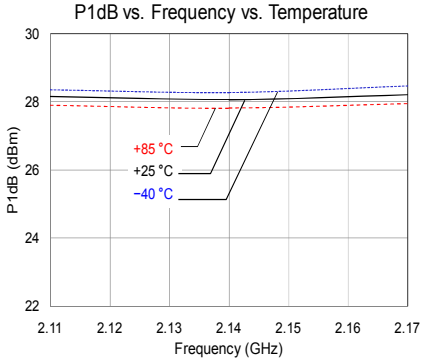






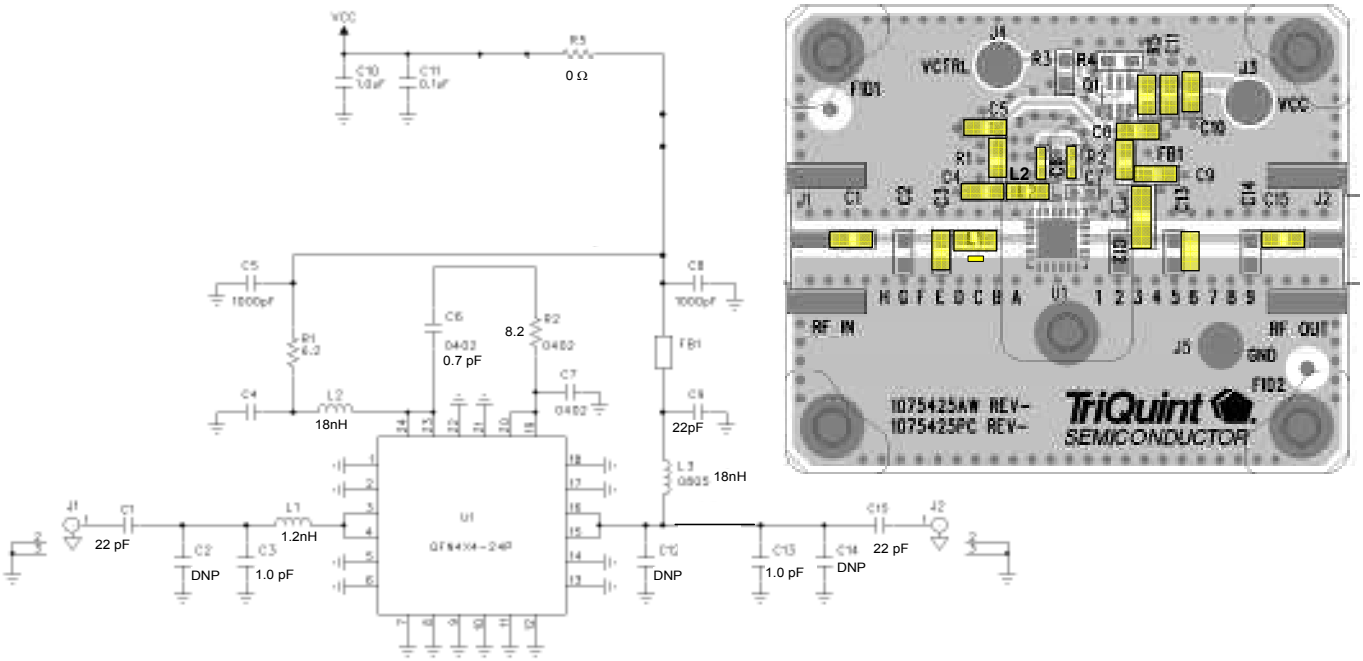






Reference Design 2300-2400 MHz (24 dB Gain)

Represents data with an interstage resistive attenuation pad in order to target lower gain across the band.



Notes:

1. C13 is placed at location '6' on the TQS application board or E.L. of 36.2° at 2.35 GHz from the U1 device package.
2. L1 is placed at E.L of 16.8° at 2.35 GHz from the U1 device package.
3. C3 is placed at location 'E' on the TQS application board or E.L. of 20.3° at 2.35 GHz from the U1 device package.
4. For always ON applications, control circuitry R3, R4, Q1 are removed and placed 0 Ω jumper at R5.

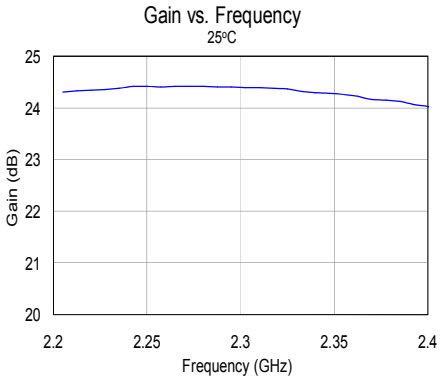
Bill of Material

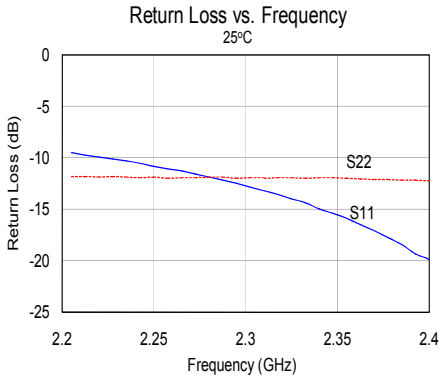
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		2-Stage Driver Amplifier	TriQuint	TQP8M9013
C6	0.7 pF	Cap, Chip, 0402, 25V, +/-0.1pF	AVX	04023J0R7BBS
C9, C4, C1, C15	22 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C5, C8	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C11	0.1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
C10	1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
L3	18 nH	Coil, Wire Wound, 0805, RoHS, 5%	Coilcraft	0805CS-18NXJL_
L2	18 nH	Coil, Wire Wound, 0603, RoHS, 5%	Coilcraft	0603CS-18NXJL_
R1	6.2 Ω	Resistor, Chip, 0603, 5%, 50V	various	
R2	8.2 Ω	Resistor, Chip, 0402, 5%, 50V	various	
FB1, R5	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C3, C13	1.0 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J1R0BSTR
C2, C12, C14, C7, R3, R4, Q1		Do Not Place		
L1	1.2 nH	Ind, Chip, 0603, +/-0.5nH, RoHS	Toko	LL1608-FSL1N2S

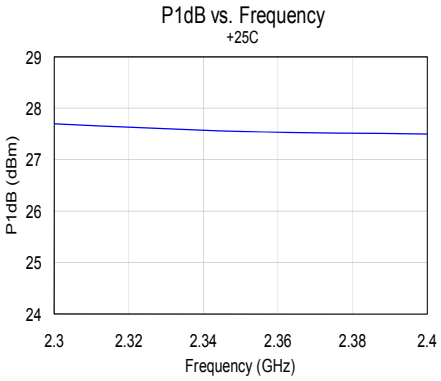
Typical Performance 2300-2400 MHz (24 dB Gain)

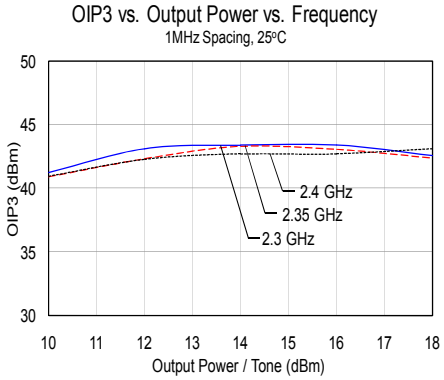
Frequency	MHz	2300	2350	2400
Gain [1]	dB	24.3	24.2	24.0
Input Return Loss	dB	12.6	15.5	20
Output Return Loss	dB	12	12	12.2
Output P1dB	dBm	+27.7	+27.5	+27.5
OIP3 [2]	dBm	+42.5	+42.2	+42.2
Channel Power @ -50 dBc ACLR [3]	dBm	+18.1	+18.0	+18.1
Channel Power @ 2.5% EVM [4]	dBm	+20.5	+20.5	+20.5
Quiescent Current, Icq	mA		225	
Supply Voltage, Vcc	V		+5	

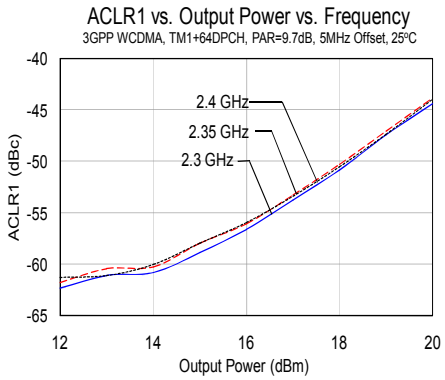
Notes:
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 12 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.
4. EVM test-setup: 802.16-2004 OFDMA, 64QAM-1/2, 1024-FFT, 20 symbols, 30 subchannels.





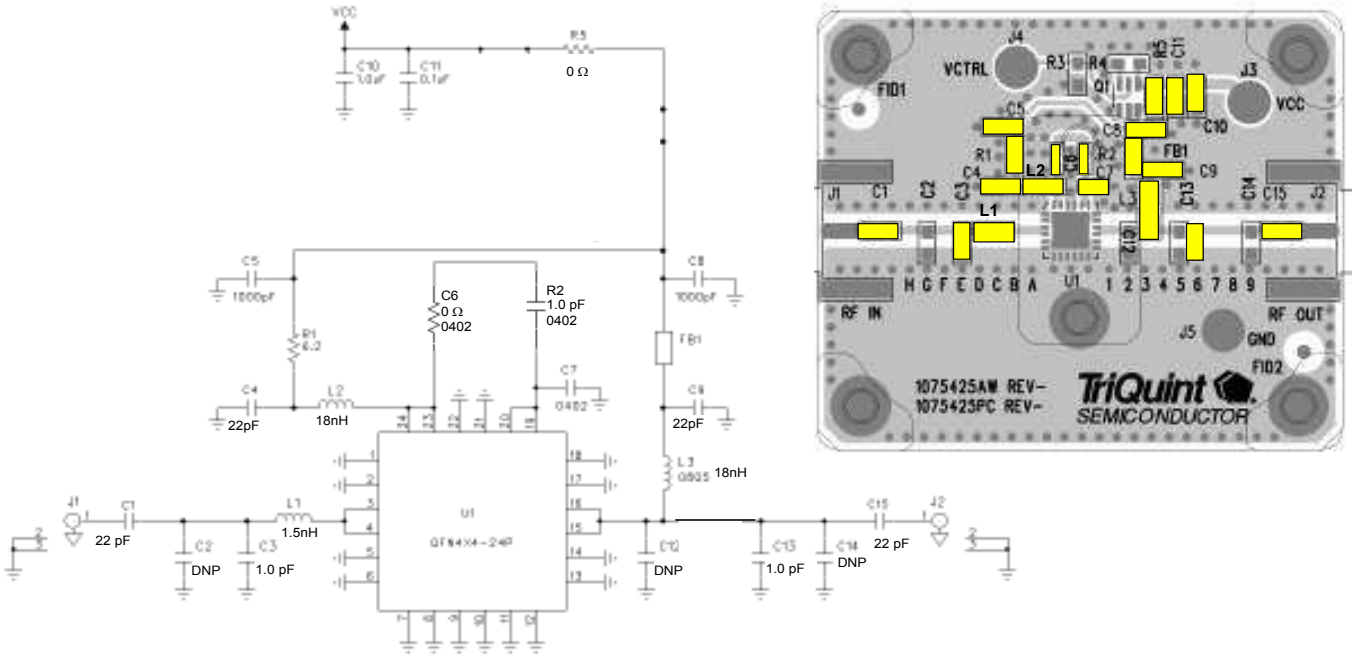






Reference Design 2300-2400 MHz (28 dB Gain)

Represents data tuned for maximum gain and optimum linearity across the band.



Notes:
1. C13 is placed at location '6' on the TQS application board or E.L. of 36.2° at 2.35 GHz from the U1 device package.
2. L1 is placed at E.L of 16.8° at 2.35 GHz from the U1 device package.
3. C3 is placed at location 'E' on the TQS application board or E.L. of 20.3° at 2.35 GHz from the U1 device package.
4. For always ON applications, control circuitry R3, R4, Q1 are removed and place 0 Ω jumper at R5.

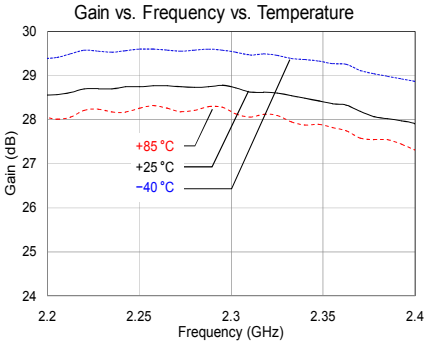
Bill of Material

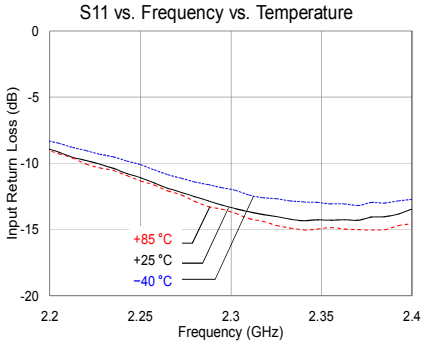
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		2-Stage Driver Amplifier	TriQuint	TQP8M9013
C6	0 Ω	Resistor, Chip, 0402, 5%, 50V	various	
C1, C15, C9, C4	22 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C7, R2	1.0 pF	Cap, Chip, 0402, 25V, +/-0.1pF	AVX	04023J1R0BBS
C5, C8	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C11	0.1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
C10	1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
L3	18 nH	Coil, Wire Wound, 0805, RoHS, 5%	Coilcraft	0805CS-18NXJL_
L2	18 nH	Coil, Wire Wound, 0603, RoHS, 5%	Coilcraft	0603CS-18NXJL_
R1	6.2 Ω	Resistor, Chip, 0603, 5%, 50V	various	
FB1, R5	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C13, C3	1.0 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J1R0BSTR
L1	1.5 nH	Ind, Chip, 0603, +/-0.5nH, RoHS	Toko	LL1608-FSL1N5S
C2, C14, Q1, R4, R3		Do Not Place		

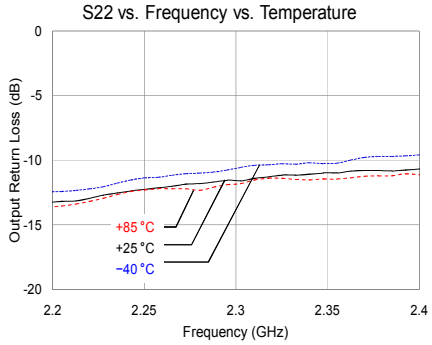
Typical Performance 2300-2400 MHz (28 dB Gain)

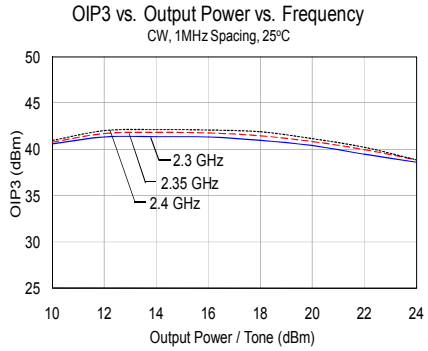
Frequency	MHz	2300	2350	2400
Gain [1]	dB	28.6	28.4	28.0
Input Return Loss	dB	11.5	15.0	19.5
Output Return Loss	dB	10.5	10.0	9.7
Output P1dB	dBm	+27.5	+27.5	+27.5
OIP3 [2]	dBm	+41.5	+42	+42
Channel Power @ -50 dBc ACLR [3]	dBm	+18.0	+18.5	+18.5
Noise Figure	dB	2.9	2.9	3.0
Quiescent Current, Icq	mA		225	
Supply Voltage, Vcc	V		+5	

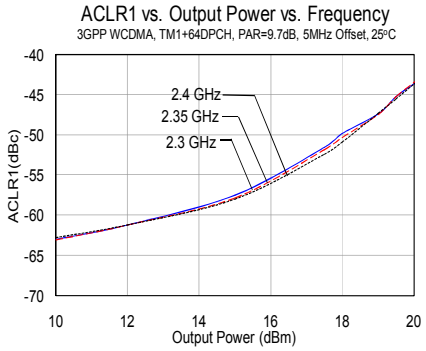
Notes:
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 11 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.

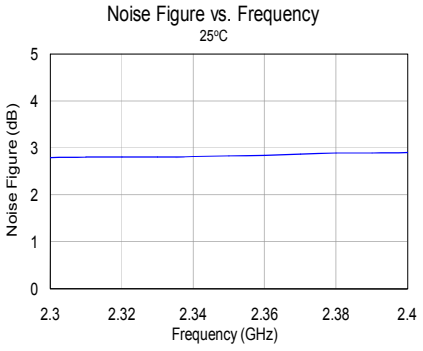


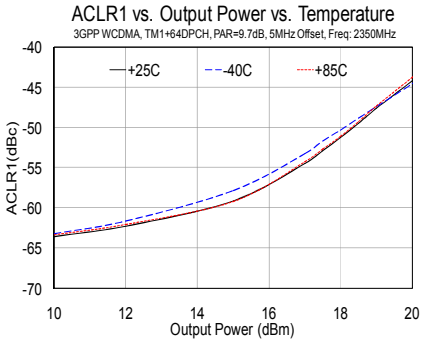


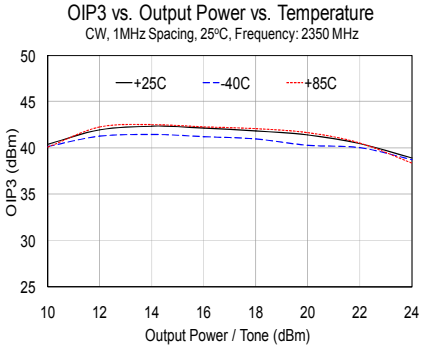


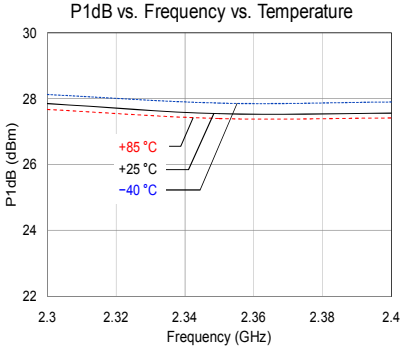




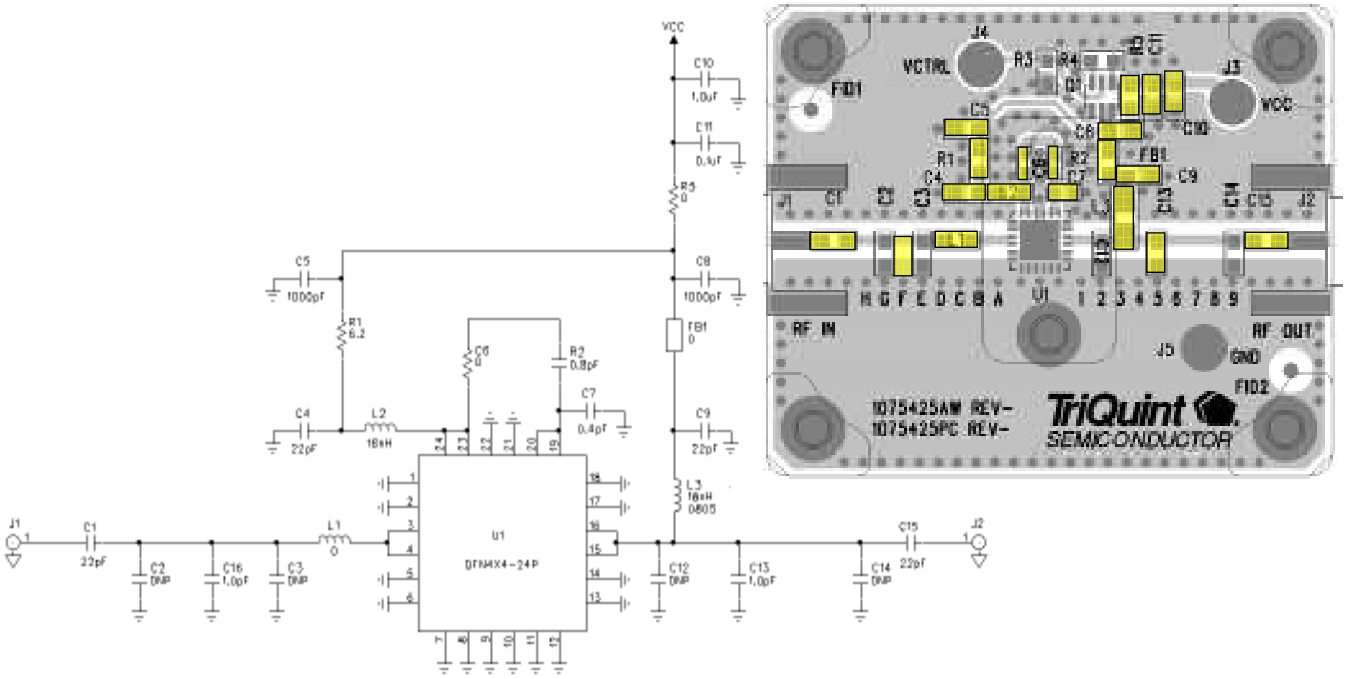








Reference Design 2500-2700 MHz



Notes:
1. The distance from U1 device package to the edge of component C16 is 260 mils or E.L. of 37.2° at 2.6 GHz.
2. C13 is placed at location '5' on the TQS application board.
3. For always ON applications, control circuitry R3, R4, Q1 are removed and place 0Ω jumper at R5.

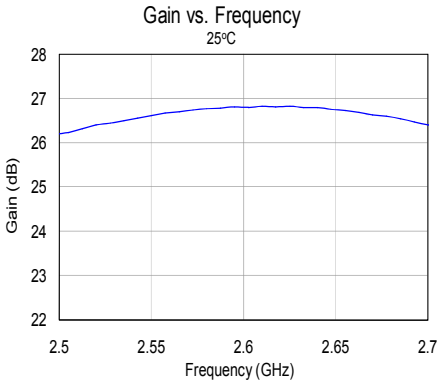
Bill of Material

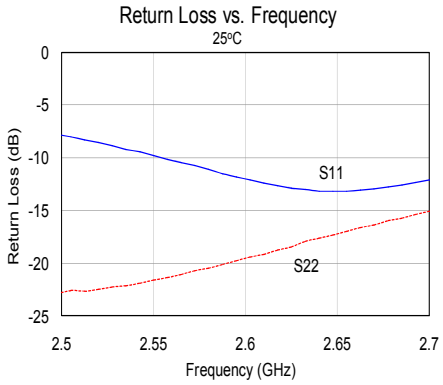
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		2-Stage Driver Amplifier	TriQuint	TQP8M9013
L1, FB1, R5	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C6	0 Ω	Resistor, Chip, 0402, 5%, 50V	various	
R2	0.8 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J0R8BSTR
C7	0.4 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J0R4BSTR
C1, C15, C9, C4	22 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C5, C8	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C11	0.1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
C10	1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
L3	18 nH	Coil, Wire Wound, 0805, RoHS, 5%	Coilcraft	0805CS-18NXJL_
L2	18 nH	Coil, Wire Wound, 0603, RoHS, 5%	Coilcraft	0603CS-18NXJL_
R1	6.2 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C13, C16	1.0 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J1R0BSTR
C2,C3, C7, C13, C14, Q1, R4, R3		Do Not Place		

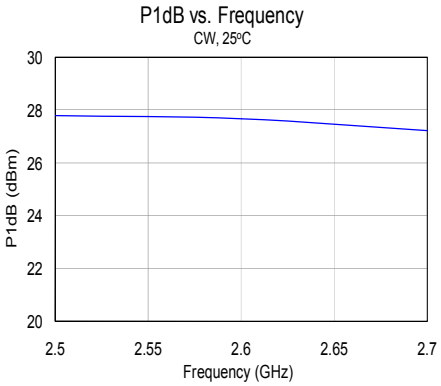
Typical Performance 2500-2700 MHz

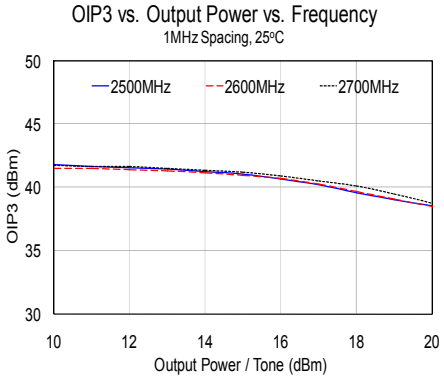
Frequency	MHz	2500	2600	2700
Gain [1]	dB	26.2	26.8	26.4
Input Return Loss	dB	7.7	11.5	12.4
Output Return Loss	dB	22.5	19.4	15.0
Output P1dB	dBm	+27.8	+27.7	+27.2
OIP3 [2]	dBm	+41.5	+41.4	+41.6
Channel Power @ -50 dBc ACLR [3]	dBm	+17.9	+17.9	+17.9
Quiescent Current, Icq	mA	225		
Supply Voltage, Vcc	V	+5		

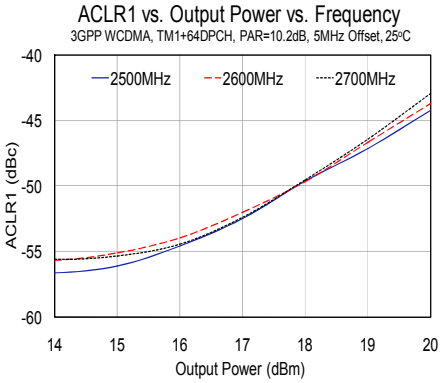
Notes:
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 12 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.



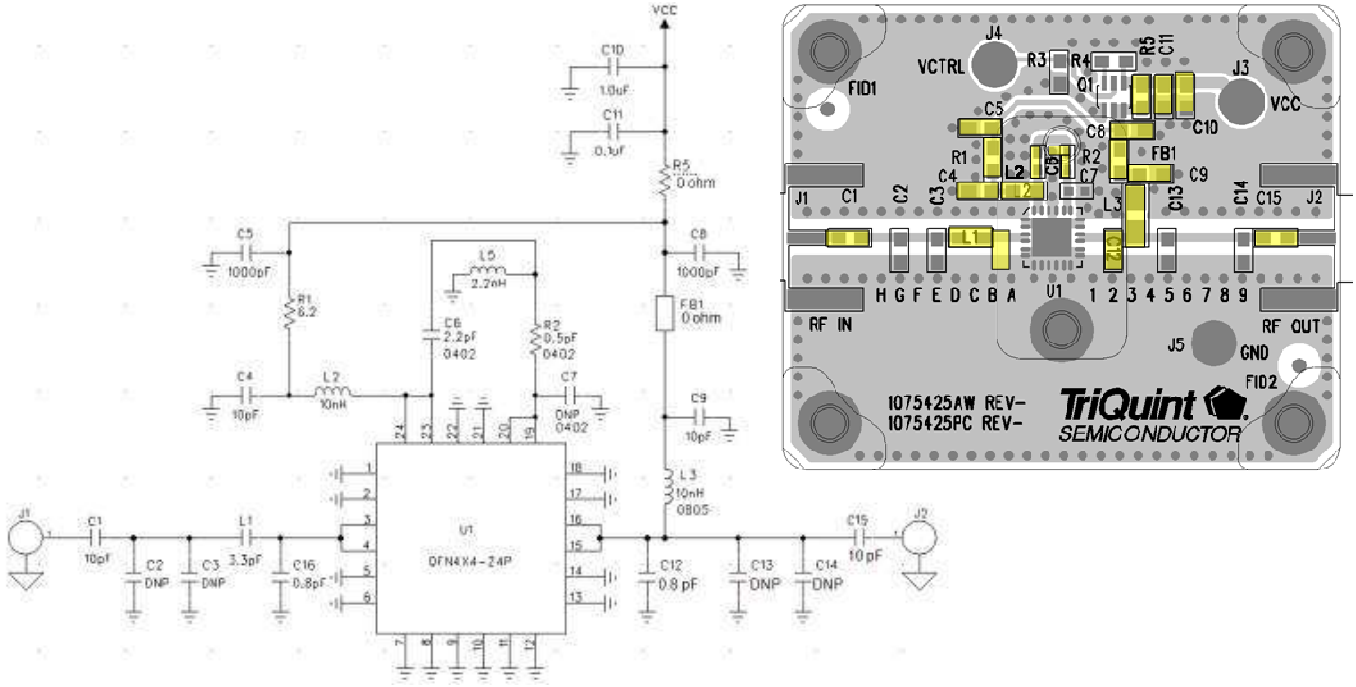








Reference Design 3400-3600 MHz



Notes:
1. The distance from U1 device package to the edge of component C16 is 40 mils E.L. of 7.7° at 3.5 GHz from the U1 device package.
2. C12 is placed at location '2' on the TQS application board.
3. For always ON applications, control circuitry R3, R4, Q1 are removed and place 0Ω jumper at R5.

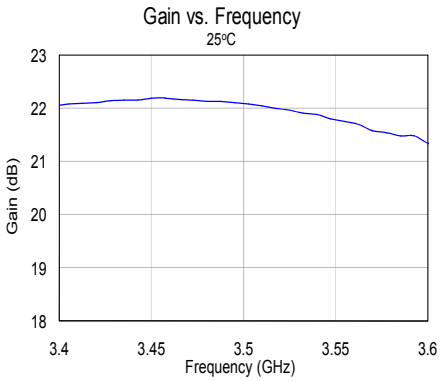
Bill of Material

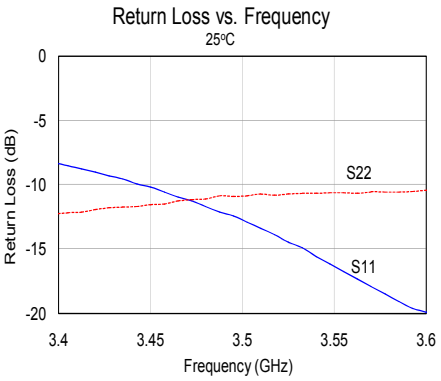
Reference Desg.	Value	Description	Manufacturer	Part Number
U1		2-Stage Driver Amplifier	TriQuint	TQP8M9013
L1	3.3 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J3R3BSTR
C6	2.2 pF	Cap, Chip, 0402, 25V, +/-0.1pF	AVX	04023J2R2BBS
R2	0.5 pF	Cap, Chip, 0402, 25V, +/-0.1pF	AVX	04023J0R5BBS
L5	2.2 nH	Ind, Chip, 0402, +/-0.5nH, RoHS	Toko	LL1005-FHL2N2S
C1, C15, C9, C4	10 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C5, C8	1000 pF	Cap, Chip, 0603, 50V, 5%, NPO	various	
C11	0.1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
C10	1 uF	Cap, Chip, 0603, 25V, +/-10%, X5R	various	
L3	10 nH	Coil, Wire Wound, 0805, RoHS, 5%	Coilcraft	0805CS-100XJLB
L2	10 nH	Coil, Wire Wound, 0603, RoHS, 10%	Toko	LL1608-FSL10NJ
R1	6.2 Ω	Resistor, Chip, 0603, 5%, 50V	various	
FB1, R5	0 Ω	Resistor, Chip, 0603, 5%, 50V	various	
C16, C12	0.8 pF	Cap, Chip, 0603, 25V, +/-0.1pF	AVX	06035J0R8BSTR
C2,C3, C7, C13, C14, Q1, R4, R3		Do Not Place		

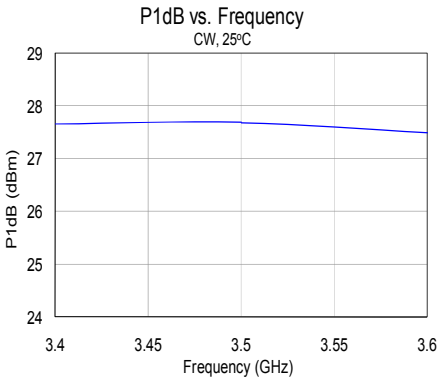
Typical Performance 3400-3600 MHz

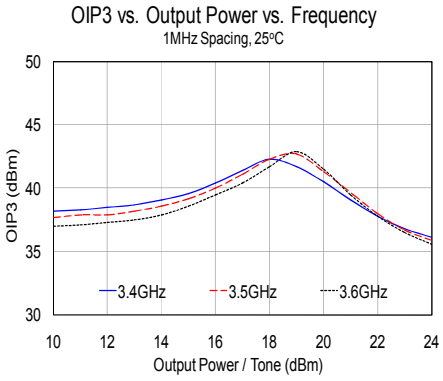
Frequency	MHz	3400	3500	3600
Gain [1]	dB	22.0	22.4	21.6
Input Return Loss	dB	8.5	13.0	20.0
Output Return Loss	dB	12.0	10.8	10.5
Output P1dB	dBm	+27.6	+27.7	+27.5
OIP3 [2]	dBm	+42.3	+42.4	+42.0
Channel Power @ -50 dBc ACLR [3]	dBm	+17.7	+18.0	+17.6
Channel Power @ 2% EVM [4]	dBm	+19.4	+19.6	+19.5
Quiescent Current, Icq	mA	225		
Supply Voltage, Vcc	V	+5		

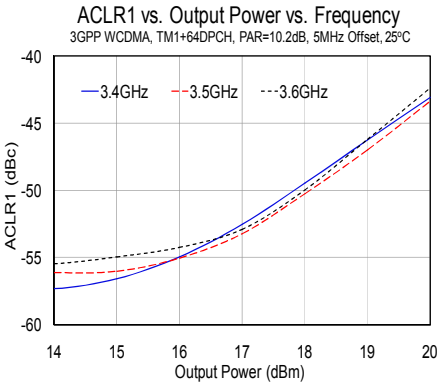
Notes:
1. Test conditions unless otherwise noted: 25 ºC, +5V, in tuned application circuit.
2. OIP3 is measured at 18 dBm Pout / tone with 1 MHz spacing.
3. ACLR test set-up: 3GPP WCDMA, TM1+64DPCH, +5MHz Offset, PAR = 10.2 dB @ 0.01% Probability.
4. EVM test-setup: 802.16-2004 OFDMA, 64QAM-1/2, 1024-FFT, 20 symbols, 30 subchannels.

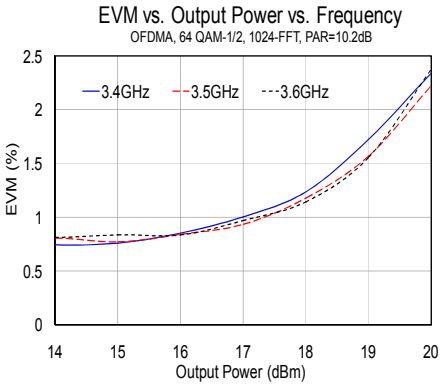












Detailed Device Description

TQP8M9013 is a multi chip module including two GaAs dies packaged in a standard 4x4 mm, 24L QFN plastic package. The amplifier is High Linearity, High Gain, High Efficiency 0.5W driver amplifier, which covers the 0.7 to 3.8 GHz band and operates from a single 5V supply. The dynamic active bias circuit enables stable operation over Bias and Temperature variations and can provide a high linearity at back-off operation.

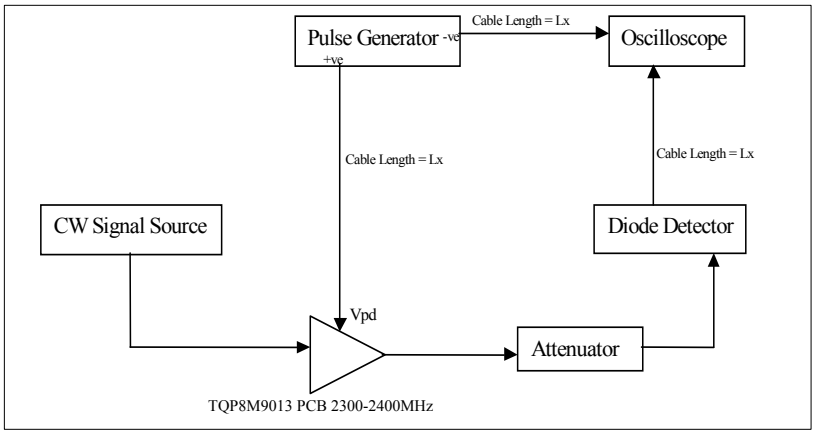
TQP8M9013 incorporates a high linearity, low noise figure gain block as first stage followed by 0.5W, high linearity amplifier. The input and output of the amplifiers are accessible with external pins to allow for customized interstage matching and configure the amplifier for applications within the frequency bandwidth. Matching networks are specific for each band of operation. Reference designs are provided in this datasheet for the popular wireless bands. De-embedded S-parameters are available off the TQS website for tuning to other bands of operation. Further assistance may be requested from TriQuint Applications Engineering, **sjcapplications.engineering@tqs.com**.

Switching Speed Test

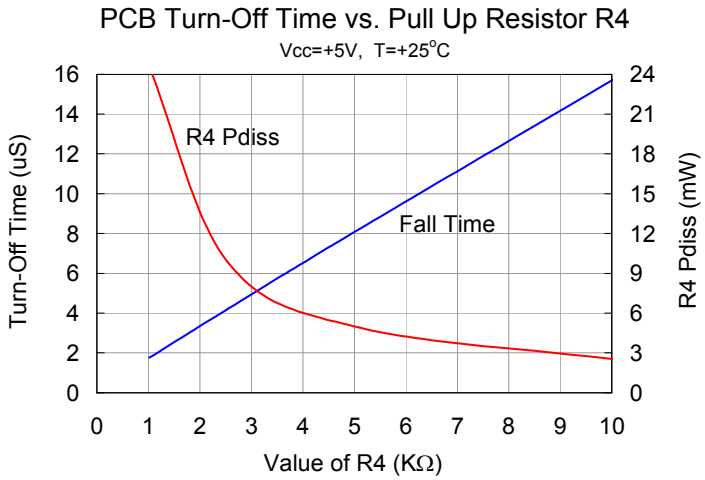
Test Conditions:
Vcc = +5V at 25°C
Output Power = +10dBm @ 2.35 GHz
Rep Rate = 1 KHz, 50% duty cycle
Vctrl amplitude = +5V
Xtal Detector Voltage =15mV (square law)

Application Board tuned for 2300-2400 MHz:
Q1 = NTJD1155L (load switch)
R4 = 3.0Kohm, R3=56K ohm
R5 = Do not place

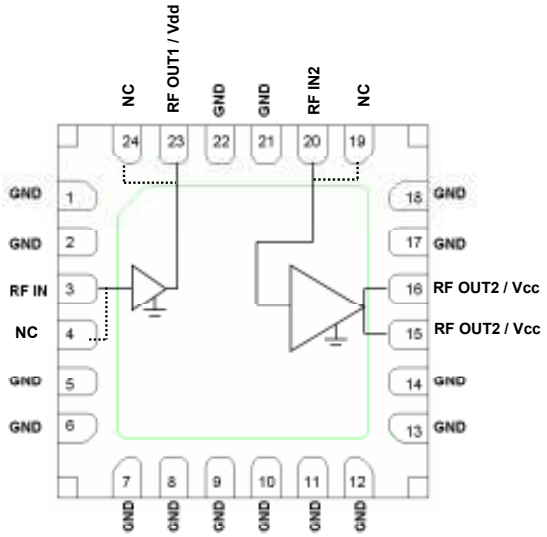
Turn-On Time (50% logic to 90% RF) = 75ns
Turn-Off Time (50% logic to 10% RF) = 5us



Turn-off time directly depends on value of pull-up resistor R4. This allows selecting the best compromise between switching speed and pull-up resistor power dissipation for particular application. The pull-up dissipates power only when the device is on, slightly degrading efficiency. In the off mode power dissipation is zero. Turn-on time is independent of value of pull-up resistor R4.



Pin Description



Pin	Symbol	Description
3	RF IN1	RF Input, Amp Stage 1
23	RF OUT1 / V_{dd}	RF Output, Amp Stage 1 / Vdd
20	RF IN2	RF Input, Amp Stage 2
15, 16	RF OUT2 / V_{cc}	RF Output, Amp Stage 2 / Vcc
4, 19, 24	N/C	Pins 4, 19, and 24 are N/C internally, but may be connected as signal pins on the PCB.
Backside Paddle	GND	Multiple vias should be employed to minimize inductance and thermal resistance; see page 11 for suggested footprint.
1, 2, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 17, 18, 21, 22	GND	These pins are not connected internally but are recommended to be grounded on the PCB for optimal isolation.

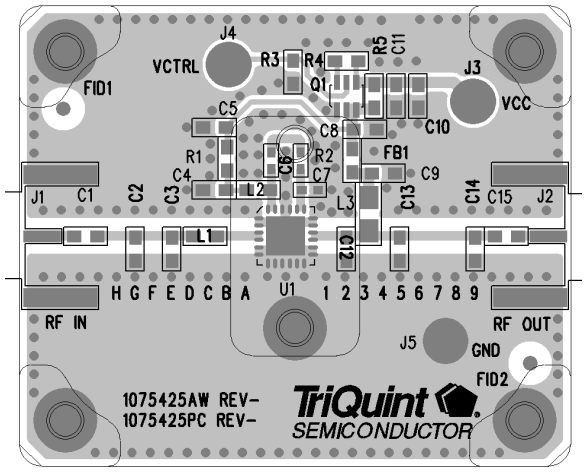
Applications Information

PC Board Layout

Top RF layer is .014" FR4, ϵ_r = 4.3, 4 total layers (0.062" thick) for mechanical rigidity. Metal layers are 1-oz copper. Microstrip line details: width = .026", spacing = .026".

An optional switching circuit is added to the PCB for the use of the amplifier with TDD- based applications. It is also permissible to operate the amplifier direct from a 5V by no-loading R3, R4, and Q1 and placing R5 = 0 Ω.

The silk screen markers 'A', 'B', 'C', etc. and '1', '2', '3', etc. are used as placemarkers for the input and output tuning shunt capacitors. The markers and vias are spaced in .050" increments. The pad pattern shown has been developed and tested for optimized assembly at TriQuint Semiconductor. The PCB land pattern has been developed to accommodate lead and package tolerances. Since surface mount processes vary from company to company, careful process development is recommended.

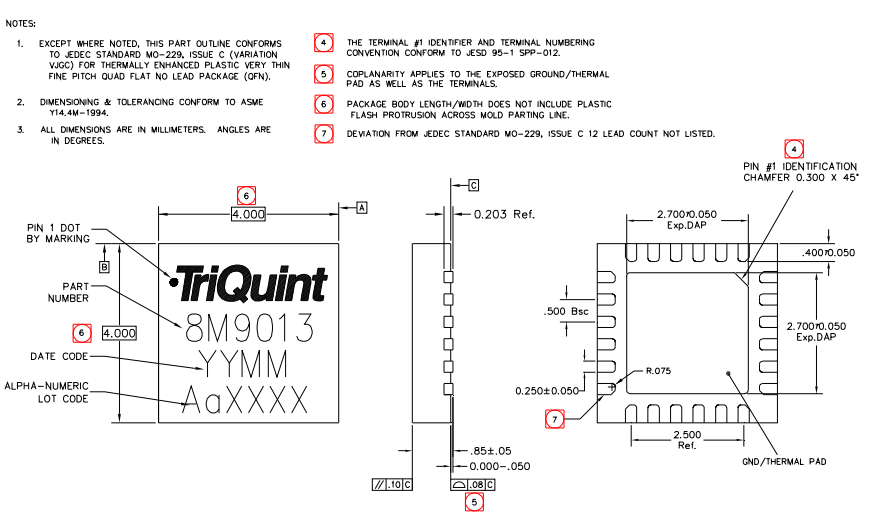


Mechanical Information

Package Information and Dimensions

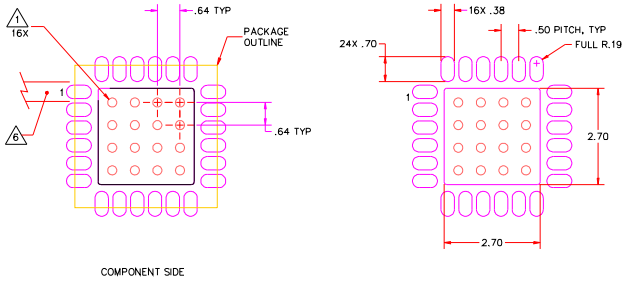
This package is lead-free, RoHS-compliant, and green. The plating material on the pins is annealed matte tin over copper. It is compatible with both lead-free (maximum 260 °C reflow temperature) and leaded (maximum 245 °C reflow temperature) soldering processes.

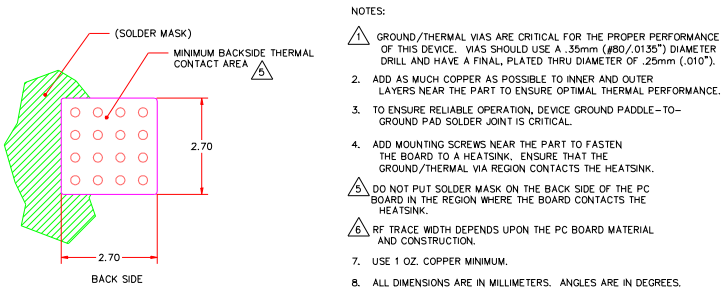
The component will be lasermarked with "8M9013" product label with an alphanumeric lot code on the top surface of the package.



Mounting Configuration

All dimensions are in millimeters (inches). Angles are in degrees.





Notes:
1. A heatsink underneath the area of the PCB for the mounted device is recommended for proper thermal operation.
2. Ground / thermal vias are critical for the proper performance of this device. Vias should use a .35mm (#80 / .0135") diameter drill and have a final plated thru diameter of .25 mm (.010").
3. Add as much copper as possible to inner and outer layers near the part to ensure optimal thermal performance.

Product Compliance Information

ESD Information

Caution! ESD-Sensitive Device

ESD Rating:	Class 1B
Value:	Passes ≥ 500V to ≤ 1000V
Test:	Human Body Model (HBM)
Standard:	JEDEC Standard JESD22-A114

ESD Rating:	Class IV
Value:	Passes ≥ 2000 V
Test:	Charged Device Model (CDM)
Standard:	JEDEC Standard JESD22-C101

MSL Rating

MSL rating 1 at +260 °C convection reflow
The part is rated Moisture Sensitivity Level 1 at 260°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260°

This part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- PFOS Free
- SVHC Free

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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Email: info-sales@tqs.com **Fax:** +1.503.615.8902

For technical questions and application information:

Email: sjcapplications.engineering@tqs.com

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