

TAT7469

CATV 75 Ω pHEMT Dual RF Amplifier



Applications

- Edge QAM gain stage
- MDU Output
- Distribution amplifiers
- Node Transimpedance Amplifier

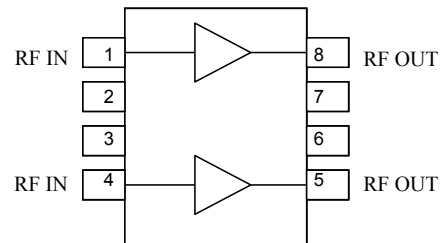
Product Features

- 75 Ω , 50 MHz to 1200 MHz Bandwidth
- Low Noise Figure: 3.2 dB to 1000 MHz
- Adjustable Low Power Consumption
- pHEMT device technology
- SOIC-8 package



SOIC-8 package

Functional Block Diagram



General Description

The TAT7469 is a 75 Ω RF Amplifier designed for CATV use, but capable of operation up to 1200 MHz. The TAT7469 contains two separate amplifiers for push pull applications. It is fabricated using 6-inch GaAs pHEMT technology to optimize performance and cost. Each amplifier contains on-chip active biasing. The bias current set point of each amplifier is adjustable with a single resistor from the input to ground.

Pin Configuration

Pin #	Symbol
1	RF IN A
2, 3, 6, 7	No Internal Connect
4	RF IN B
5	RF OUT B
8	RF OUT A
Backside Slug	GND

Ordering Information

Part No.	Description
TAT7469	75 Ω Dual pHEMT Amplifier (lead-free/RoHS compliant SOIC-8 Pkg)
TAT7469-SC8-EB	Evaluation Board

Standard T/R size = 1000 pieces on a 7" reel.

Specifications

Absolute Maximum Ratings

Parameter	Rating
Device Voltage	+10.0 V
Operating Temperature	-40 to 85 °C

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min	Typ	Max	Units
V _{DD}		5		V
I _{DD}		250		mA
T _J (for > 10 ⁶ hours MTF)			145	°C

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions

Electrical Specifications

Test conditions unless otherwise noted: 25 °C Case Temperature, +5 V V_{DD}

Parameter	Conditions	Min	Typical	Max	Units
Operational Frequency Range		50		1002	MHz
Gain			17.5		dB
Gain Flatness	Note 1		±0.75		dB
Noise Figure			3.2		dB
Input Return Loss	T _o 1000 MHz		18		dB
Output Return Loss	T _o 1000 MHz		23		dB
Output IP3	Note 2		38		dBm
Output IP2	Note 2, Note 3		68		dBm
I _{DD}	5V, Note 4		250		mA
Thermal Resistance (jnt to case) θ_{jc}			13		°C/W

Notes:

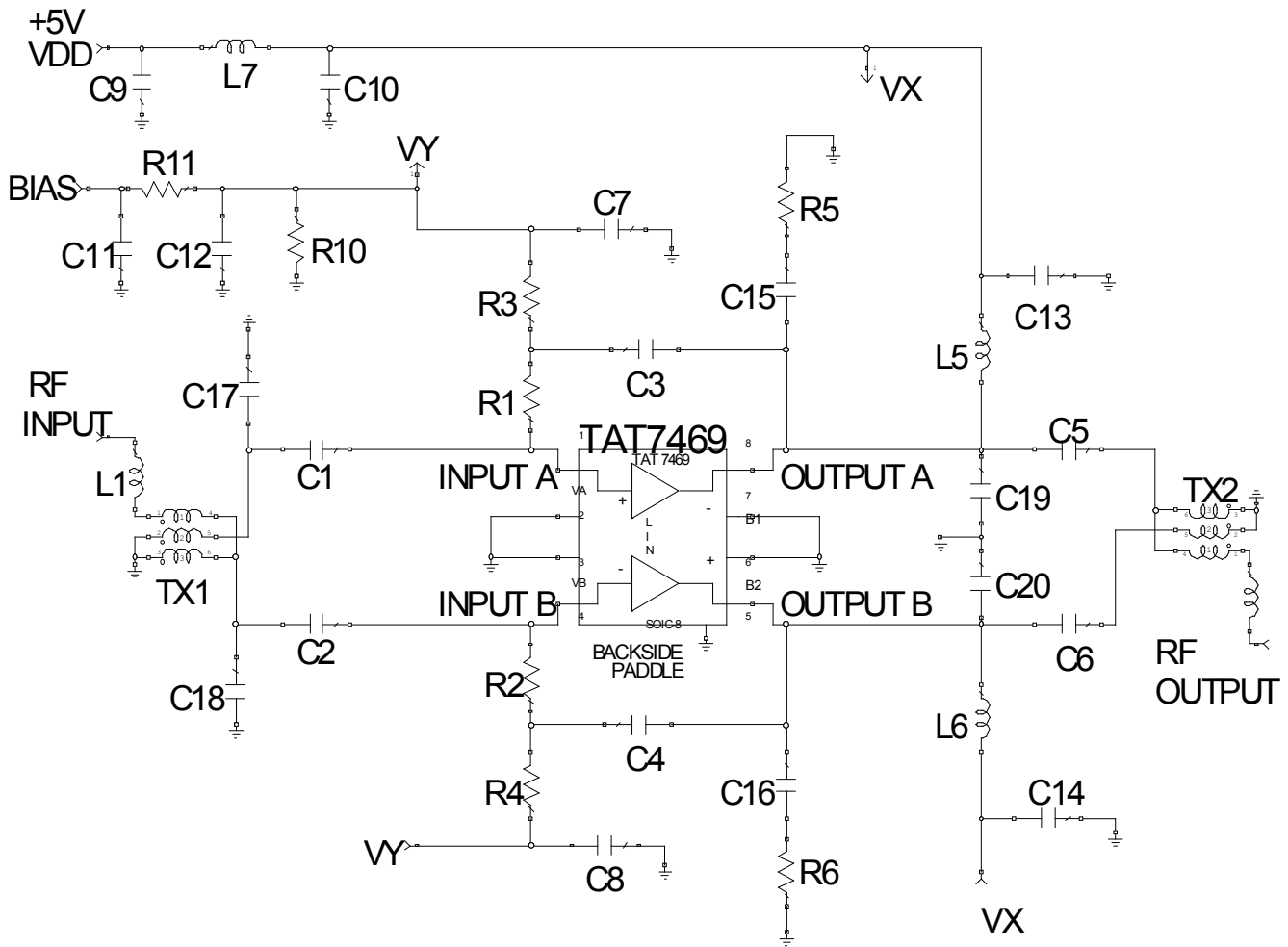
1. Flatness determined by deviation from a straight-line curve fit
2. 10 dBm/tone output, applied tones at 225 MHz and 325 MHz
3. Calculated from difference intermod
4. R3 and R4 are used to set the bias current, 10 k Ω

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Application Circuit Reference Design 50-1002 MHz



Notes:

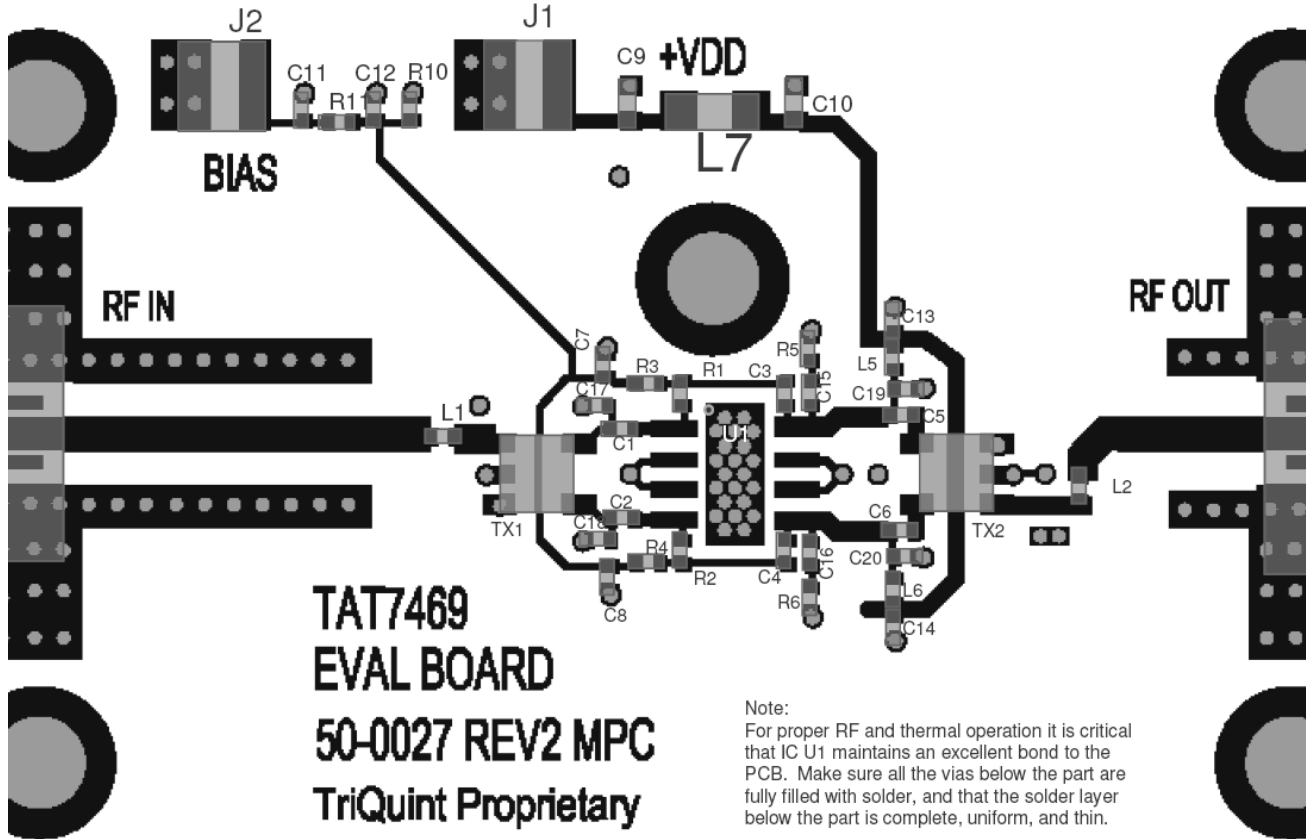
1. See PC Board Layout, page 4 for more information.

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PC Board Layout



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Application Circuit BOM 50-1002 MHz

Bill of Material

Ref. Desg.	Value	Description ⁽¹⁾	Manufacturer	Part Number
U1		75 Ω Dual pHEMT Amplifier	TriQuint	TAT7469
L1	3.6 nH	Chip Coil, 0402, 5 %	CoilCraft	0402CS-3N6XJLW
L2	2.2 nH	Chip Coil, 0402, 5 %	CoilCraft	0402CS-2N2XJLW
L5, L6	560 nH	Chip Coil, 0402, 5 %	CoilCraft	0402AF-561XJLW
L7	0.9 uH	Chip Coil, 1008, 10%	various	
TX1, TX2	1:1	1:1 Balun, 5 – 3000 MHz	MiniCircuits	TC1-33-75G2+
C1, C2, C3, C4, C7, C8, C11, C12, C13, C14	0.01 uF	Ceramic Cap, 0402, 16 V, NPO, 10 %	various	
C5, C6	470 pF	Ceramic Cap, 0402, 50 V, NPO, 10 %	various	
C15, C16	1.0 pF	Ceramic Cap, 0402, 50 V, ± 0.10 pF	AVX	04025A010BAT9A
C17, C18	0.5 pF	Ceramic Cap, 0402, 50 V, ± 0.10 pF	AVX	04025A005BAT9A
C9, C10	0.1 uF	Ceramic Cap, 0603, 16 V, NPO, 10 %	various	
R1, R2	820 Ω	Thick Film Res, 0402, 1 %	various	
R3, R4	10 k Ω	Thick Film Res, 0402, 1 %	various	
R5, R6	30 Ω	Thick Film Res, 0402, 1 %	various	
R10	100 Ω	Thick Film Res, 0402, 1 %	various	
R11	0 Ω	Thick Film Res, 0402	various	
C19, C20	N/L	Do Not Place Parts		
J3, J4	F-Edge Mount	75 Ω Female connector	Amphenol	531-40039

Notes:

1. Or equivalent

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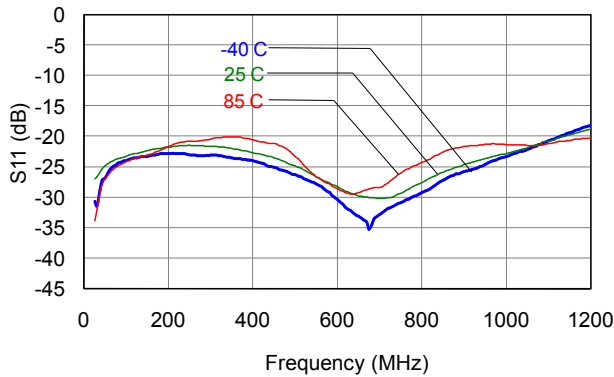
CATV 75 Ω pHEMT Dual RF Amplifier



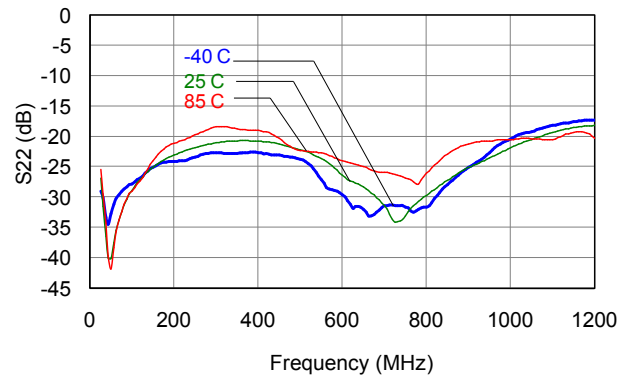
Application Board Typical Performance

$V_{DD} = +5\text{ V}$, $I_{DD} = 235\text{ mA}$ (at 25 °C), Temperatures are case temp

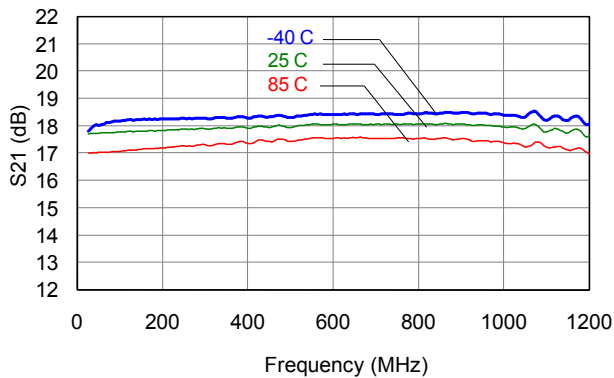
TAT7469 Input Return Loss



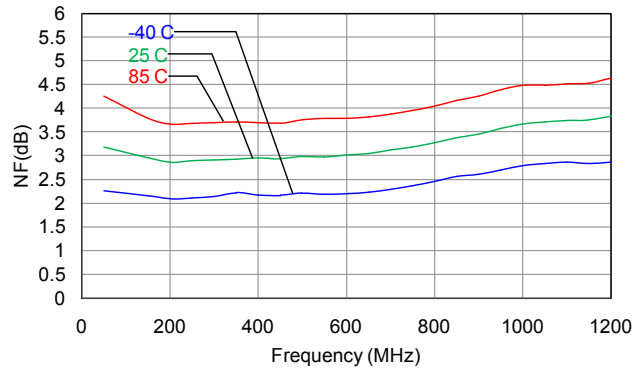
TAT7469 Output Return Loss



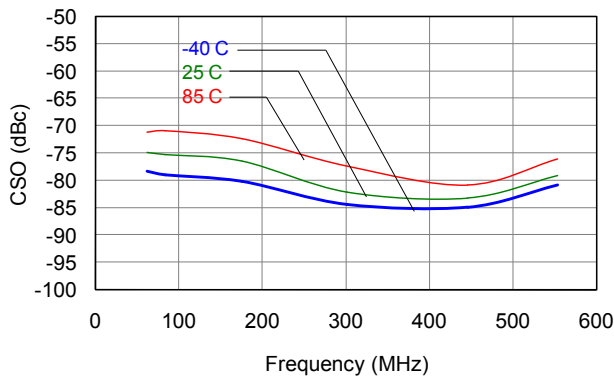
TAT7469 Gain



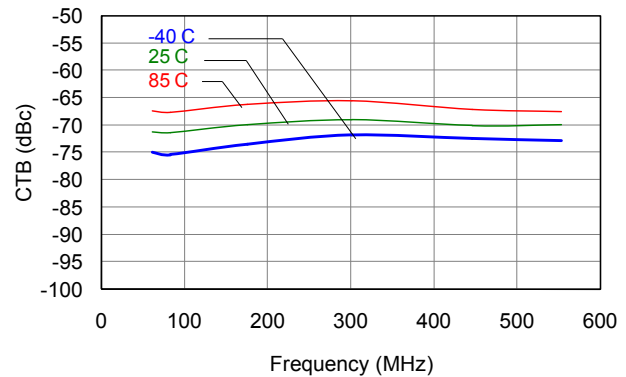
TAT7469 Noise Figure



TAT7469 CSO



TAT7469 CTB



Notes:

1. CSO and CTB: 39 dBmV/ch at output, 80 ch NTSC flat

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Mechanical Information

Package Information and Dimensions

This package is lead-free/RoHS-compliant. The plating material on the leads is 100% Matte Tin. It is compatible with both lead-free (maximum 260 °C reflow temperature) and lead (maximum 245 °C reflow temperature) soldering processes.

The TAT7469 will be marked with as follows:

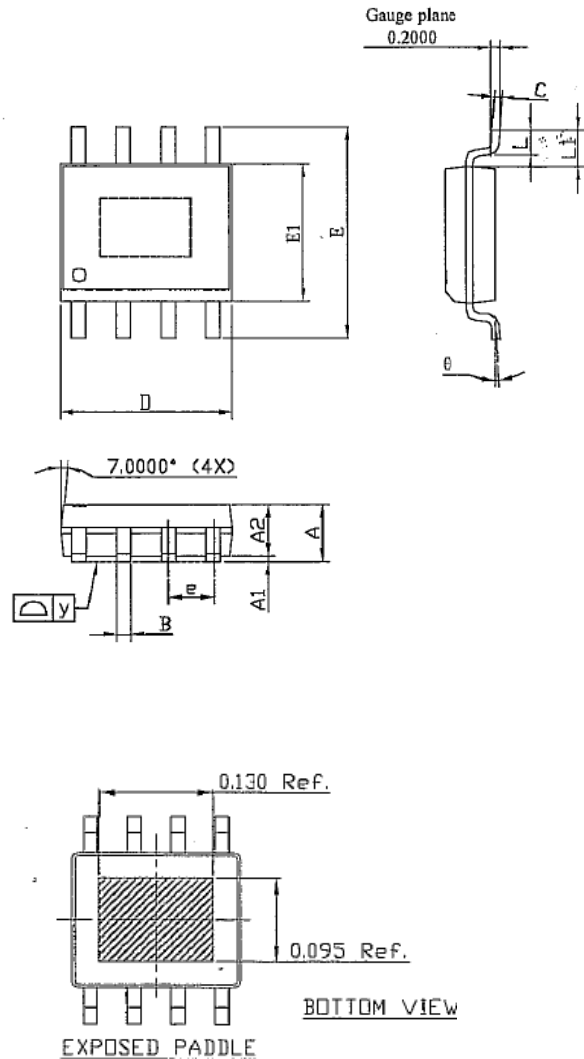
Pin 1 Location: Upper left hand corner

Line 1 Product Name “TAT7469” designator
Line 2 AaXXXX (Aa=Vendor Code, XXXX = lot number)
Line 3 YYWW (Year/week of assembly)



Package dimensions, Alternate A

SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	1.40	1.50	1.60	0.055	0.059	0.063
A1	0.00	---	0.10	0.000	---	0.004
A2	---	1.45	---	---	0.057	---
B	0.33	---	0.51	0.013	---	0.020
C	0.19	---	0.25	0.007	---	0.010
D	4.80	---	5.00	0.189	---	0.197
E1	3.80	3.90	4.00	0.150	0.153	0.157
e	---	1.27	---	---	0.050	---
E	5.80	6.00	6.20	0.228	0.236	0.244
L	0.40	---	1.27	0.016	---	0.050
y	---	---	0.10	---	---	0.004
θ	0°	---	8°	0°	---	8°
L1-L1'	---	---	0.12	---	---	0.005
L1	1.04REF			0.041REF		



Notes:

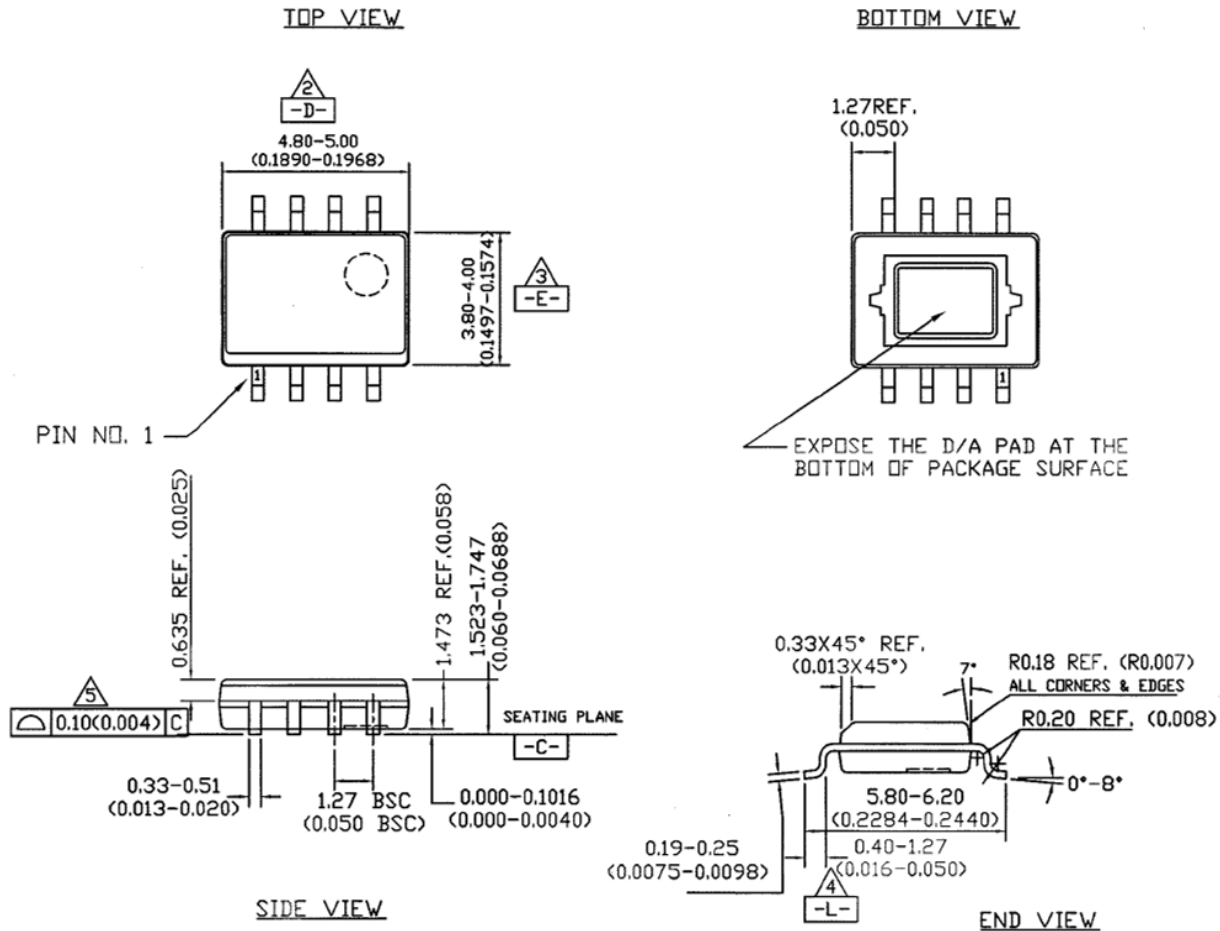
Dimensions D and E1 do not include mold flash, gate burrs, nor protrusions, not to exceed 0.25 mm per side.

Package dimensions are in the process of being updated. A new revision of this document with clarified package specifications will be released shortly. Thank you.

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Package Dimensions, Alt B



NOTES:

1. DIMENSIONING & TOLERANCING PER ANSI.Y14.5M-1982.
2. DIMENSION 'D' DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15MM(0.006") PER SIDE.
3. DIMENSION 'E' DOES NOT INCLUDE INTER-LEAD FLASH OR PROTRUSION, INTER-LEAD FLASH OR PROTRUSIONS. SHALL NOT EXCEED 0.25MM(0.010") PER SIDE.
4. 'L' IS A LENGTH OF TERMINAL FOR SOLDERING TO SUBSTATE.
5. FORMED LEAD SHALL BE PLANED WITH RESPECT TO ONE ANOTHER WITHIN 0.10MM(0.004") AT SEATING PLANE 'C'
4. BODY FINISH : 18-24 CHARMILLES.
5. CONTROLLING DIMENSION : MILLIMETER CONVERTED INCH DIMENSION ARE NOT NECESSARILY EXACT.
6. LEAD FINISH IS ELECTROPLATING WITH A THICKNESS OF 300 - 800 MICROINCH.
7. CHARACTER HEIGHT ON EJECTOR PIN IS 0.635MM(0.025"). 'TH' STAND FOR THAILAND.
8. RAISED CHARACTER NOT TO PROTRUDE BEYOND SURFACE OR PACKAGE BODY.

Product Compliance Information

ESD Information



Caution! ESD-Sensitive Device

ESD Rating: Class 1 B
Value: Passes \geq 600 V min.
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

ESD Rating: Class IV+
Value: Passes \geq 2000 V min.
Test: Charged Device Model (CDM)
Standard: JEDEC Standard JESD22-C101

MSL Rating

Level 3 at +260 °C convection reflow.
The part is rated Moisture Sensitivity Level 3 at 260 °C per
JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020, Lead free solder, 260 °C.

is part is compliant with EU 2002/95/EC RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment).

Contact Information

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