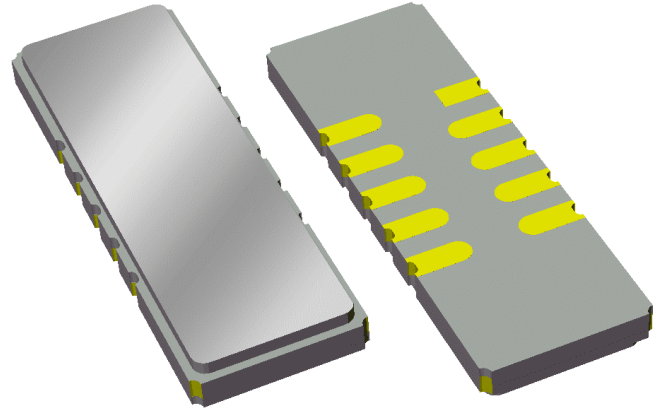


Preliminary Data Sheet

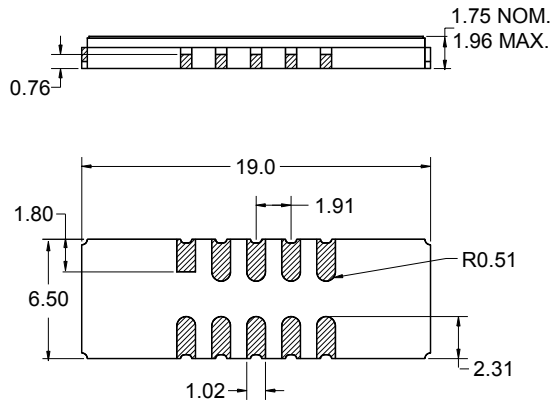
Features

- For broadband applications
- Typical 3 dB bandwidth of 2.2 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Small size
- Replaces Sawtek P/N 851546 (BW 3dB=2.0 MHz)



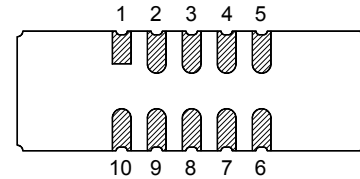
Package

Surface Mount 19.00 x 6.50 x 1.75 mm



Pin Configuration

Bottom View



Pin No.	Description
5	RF output
10	RF input
1,6	Ground
2,3,4	Case ground
7,8,9	Case ground

Dimensions shown are nominal in millimeters
 All tolerances are ± 0.15 mm except overall
 length and width $+0.15$ mm/ -0.10 mm

Body: Al_2O_3 ceramic
 Lid: Kovar, Ni plated
 Terminations: Au plating 0.5 - 1.0 μ m,
 over a 2 - 6 μ m Ni plating

Preliminary Data Sheet

Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ 0 to +70 °C

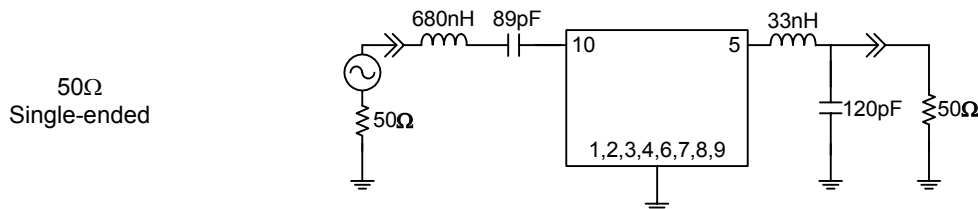
Parameter ⁽³⁾	Minimum	Typical	Maximum	Unit
Center Frequency	-	70	-	MHz
Minimum Insertion Loss	-	23	24.25	dB
Lower 1 dB Bandedge ⁽⁴⁾	-	69	69.13	MHz
Upper 1 dB Bandedge	70.87	71	-	MHz
Lower 3 dB Bandedge ⁽⁴⁾	-	68.9	68.94	MHz
Upper 3 dB Bandedge	71.06	71.1	-	MHz
Lower 40 dB Bandedge ⁽⁴⁾	68.21	68.3	-	MHz
Upper 40 dB Bandedge	-	71.7	71.79	MHz
Amplitude Variation 69.125 - 70.875 MHz	-	0.6	1	dB
Phase Linearity 69.125 - 70.875 MHz	-	1.7	3	deg
Group Delay Variation 69.125 - 70.875 MHz	-	70	110	nsec
Absolute Delay	-	2.3	-	μsec
Relative Attenuation ⁽⁴⁾				
10.00 - 67.75 MHz	50	60	-	dB
72.25 - 125.00 MHz	50	60	-	dB
125.00 - 145.00 MHz	45	50	-	dB
145.00 - 200.00 MHz	50	60	-	dB
Source Impedance: ⁽⁵⁾	-	50	-	Ω
Load Impedance: ⁽⁵⁾	-	50	-	Ω
Substrate Material	-	LiTaO ₃	-	-
Temperature Coefficient of Frequency	-	-23	-	ppm/°C

Notes:

1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. All attenuation measurements are measured relative to minimum insertion loss
5. This is the optimum impedance in order to achieve the performance shown

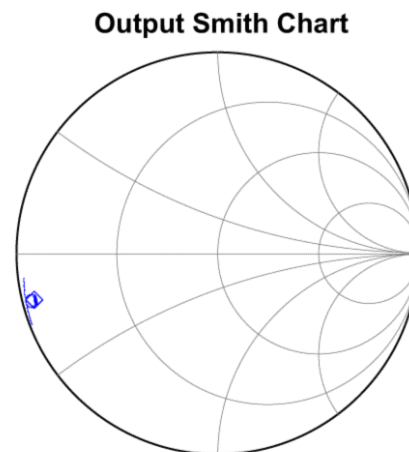
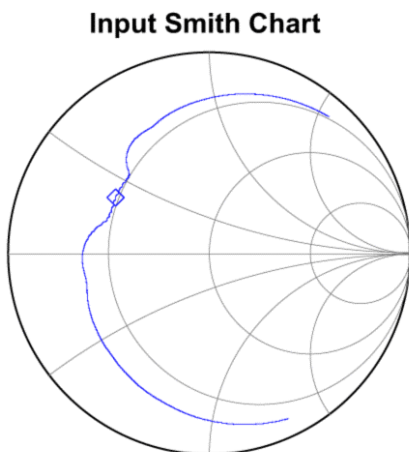
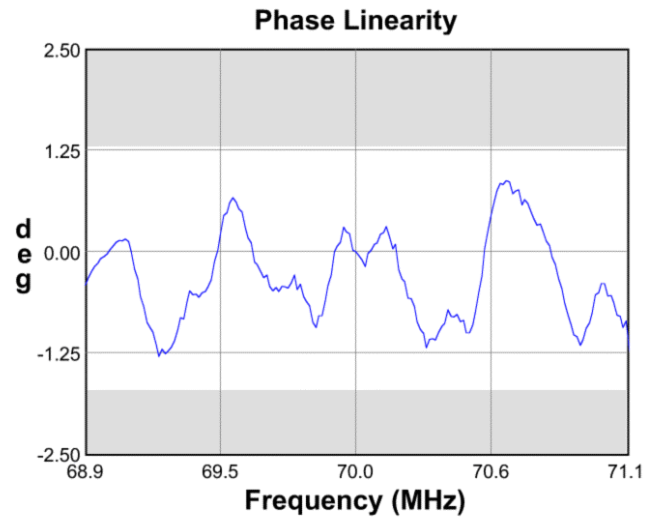
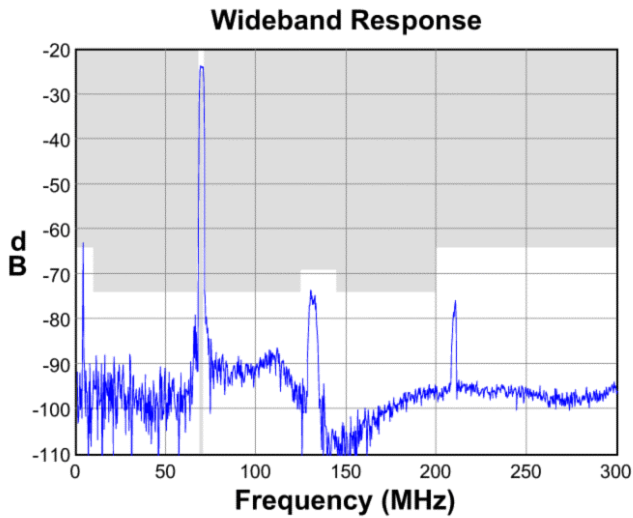
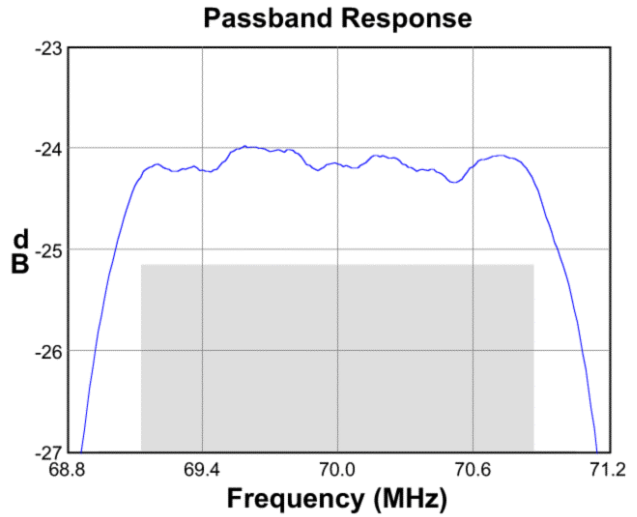
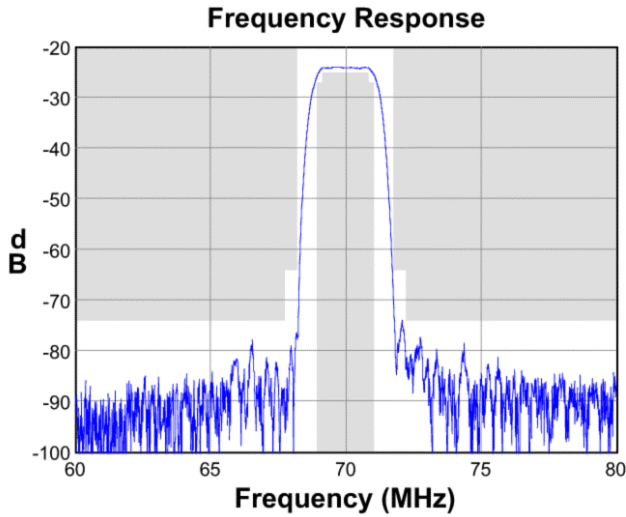
Test Circuit:

Actual matching values may vary due to PCB layout and parasitics



Preliminary Data Sheet

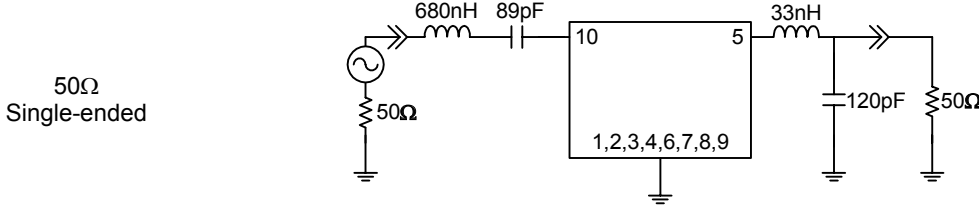
Typical Performance (at +25°C)



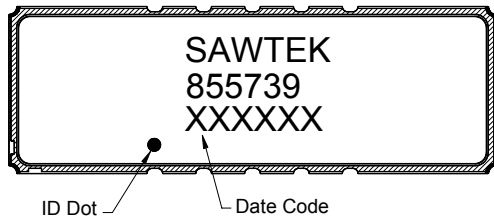
Preliminary Data Sheet

Matching Schematics

Actual matching values may vary due to PCB layout and parasitics

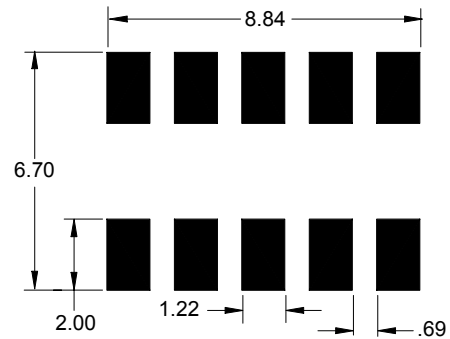


Marking



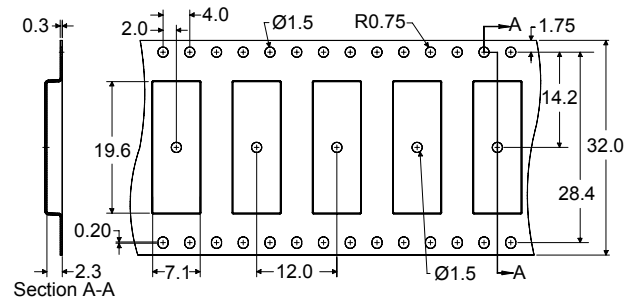
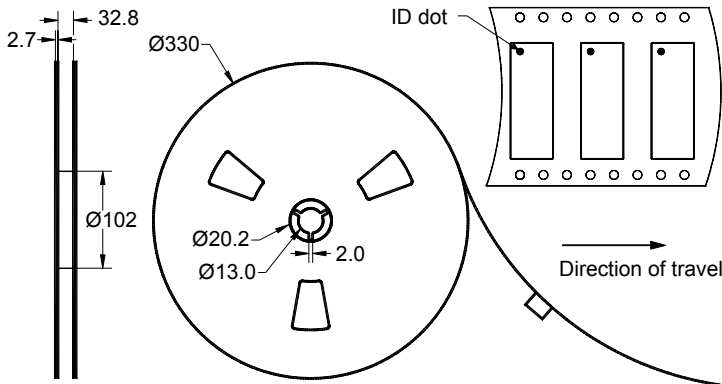
The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

PCB Footprint



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel




Dimensions shown are nominal in millimeters
Packaging quantity: 2000 units/reel

Preliminary Data Sheet

Maximum Ratings

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temperature Range	T	0	+25	+70	°C
Storage Temperature Range	T _{stg}	-40	-	+85	°C

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

Links to Additional Technical Information

[PCB Layout Tips](#)
[Qualification Flowchart](#)
[Soldering Profile](#)
[S-Parameters](#)
[Other Technical Information](#)

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