
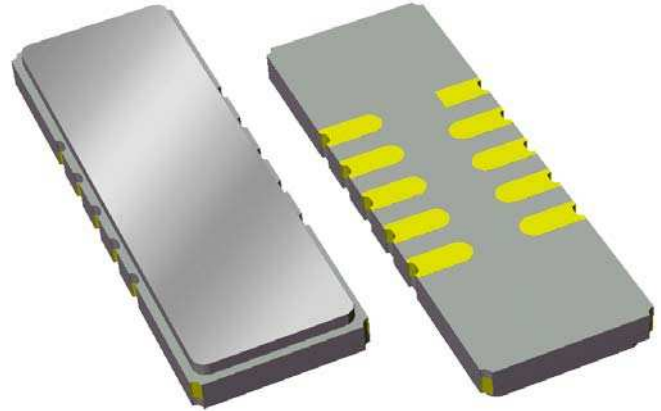


# Preliminary Data Sheet

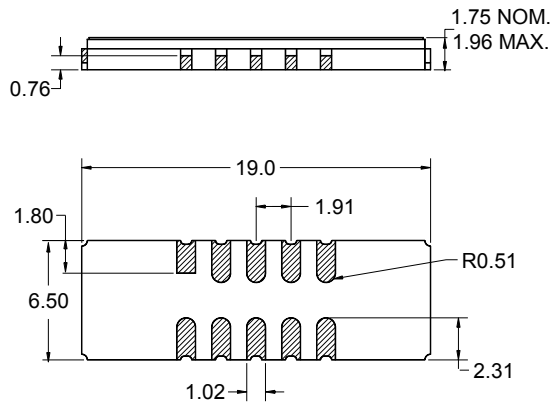
## Features

- For broadband applications
- Typical 3 dB bandwidth of 4.4 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851550 (BW 3dB=4.0 MHz)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



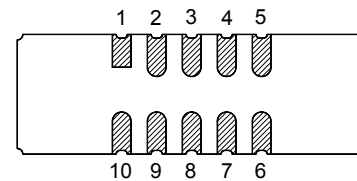
## Package

Surface Mount 19.00 x 6.50 x 1.75 mm



## Pin Configuration

Bottom View



Pin No.	Description
5	RF output
10	RF input
1,6	Ground
2,3,4	Case ground
7,8,9	Case ground

Dimensions shown are nominal in millimeters  
 All tolerances are  $\pm 0.15\text{mm}$  except overall  
 length and width  $+0.15\text{mm}/-0.10\text{mm}$

Body:  $\text{Al}_2\text{O}_3$  ceramic  
 Lid: Kovar, Ni plated  
 Terminations: Au plating 0.5 - 1.0 $\mu\text{m}$ ,  
 over a 2 - 6 $\mu\text{m}$  Ni plating

# Preliminary Data Sheet

## Electrical Specifications <sup>(1)</sup>

Operating Temperature Range: <sup>(2)</sup> 0 to +70 °C

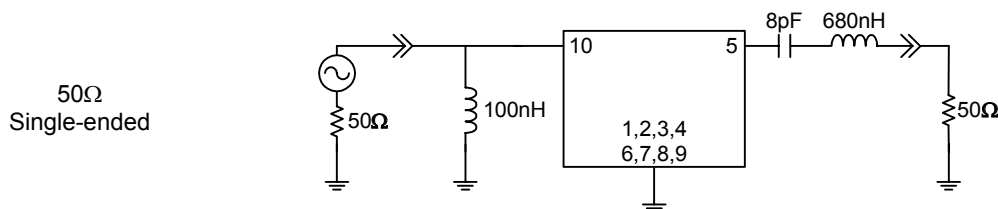
Parameter <sup>(3)</sup>	Minimum	Typical	Maximum	Unit
<b>Center Frequency</b>	-	70	-	MHz
<b>Minimum Insertion Loss</b>	-	23	24	dB
<b>Lower 1 dB Bandedge</b> <sup>(4)</sup>	-	68	68.1	MHz
<b>Upper 1 dB Bandedge</b>	71.9	72	-	MHz
<b>Lower 3 dB Bandedge</b> <sup>(4)</sup>	-	67.8	67.87	MHz
<b>Upper 3 dB Bandedge</b>	72.13	72.2	-	MHz
<b>Lower 40 dB Bandedge</b> <sup>(4)</sup>	67	67.2	-	MHz
<b>Upper 40 dB Bandedge</b>	-	72.8	73	MHz
<b>Amplitude Variation</b> 68.1 - 71.9 MHz	-	0.5	0.8	dB
<b>Phase Linearity</b> 68.1 - 71.9 MHz	-	3.3	4.75	deg
<b>Group Delay Variation</b> 68.1 - 71.9 MHz	-	70	100	nsec
<b>Absolute Delay</b>	-	2.4	-	μsec
<b>Relative Attenuation</b> <sup>(4)</sup>				
10 - 60 MHz	50	65	-	dB
60 - 67 MHz	45	50	-	dB
73 - 80 MHz	45	50	-	dB
80 - 125 MHz	50	50	-	dB
125 - 140 MHz	45	50	-	dB
140 - 200 MHz	50	65	-	dB
<b>Source Impedance:</b> <sup>(5)</sup>	-	50	-	Ω
<b>Load Impedance:</b> <sup>(5)</sup>	-	50	-	Ω
<b>Substrate Material</b>	-	LiTaO <sub>3</sub>	-	-
<b>Temperature Coefficient of Frequency</b>	-	-23	-	ppm/°C

### Notes:

- All specifications are based on the test circuit shown below
- In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
- Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
- All attenuation measurements are measured relative to minimum insertion loss
- This is the optimum impedance in order to achieve the performance shown

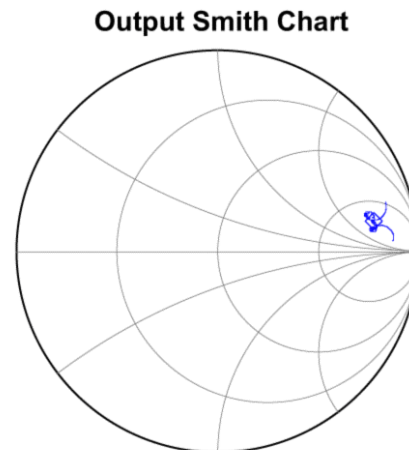
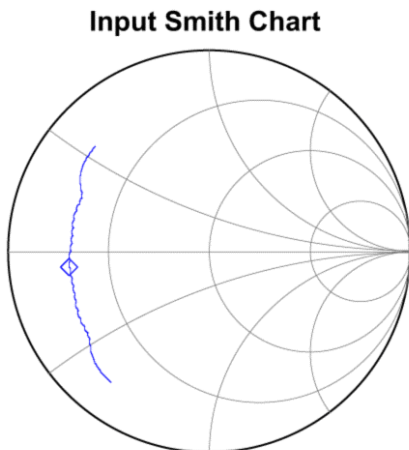
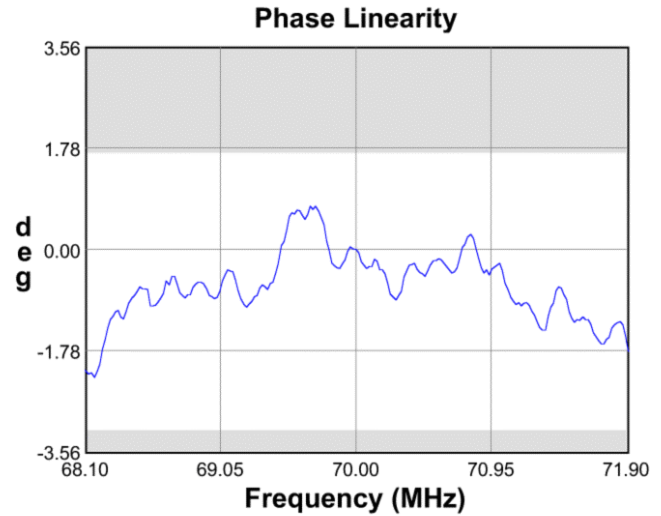
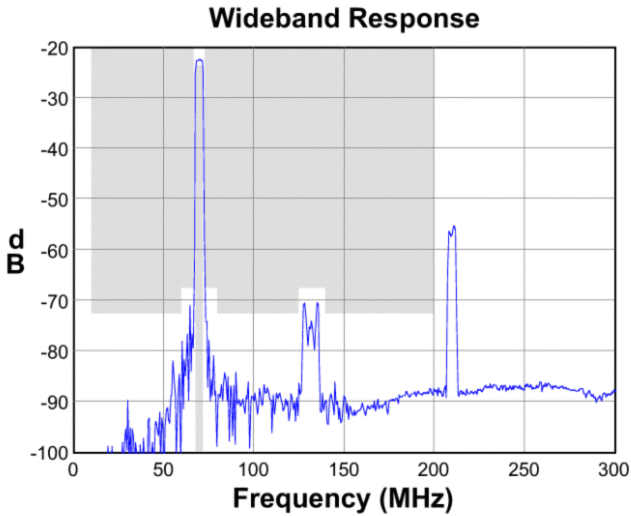
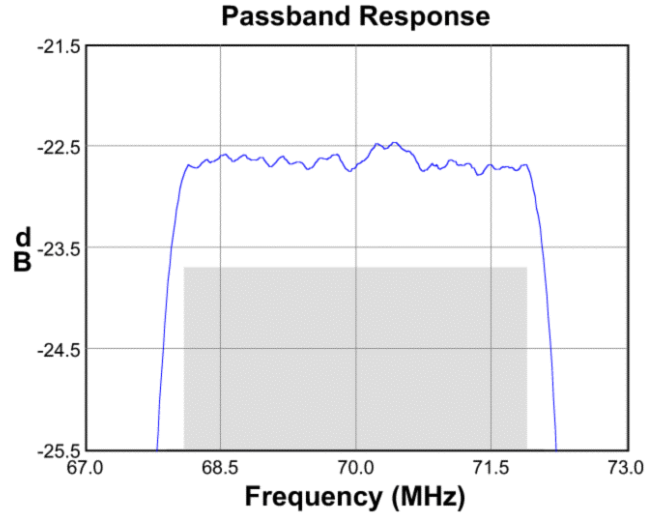
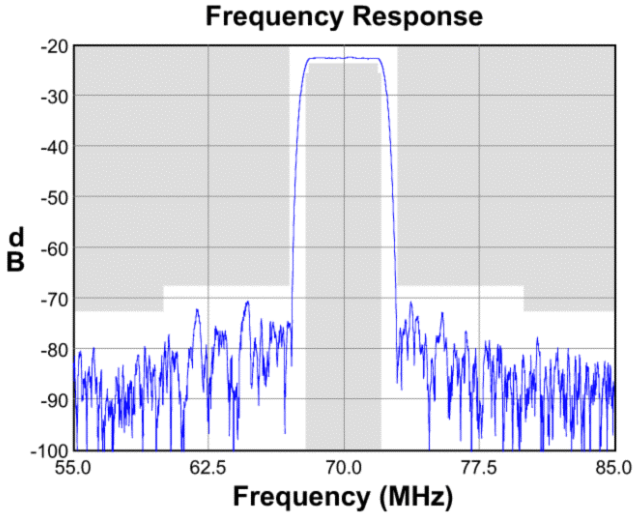
### Test Circuit:

Actual matching values may vary due to PCB layout and parasitics



**Preliminary Data Sheet**

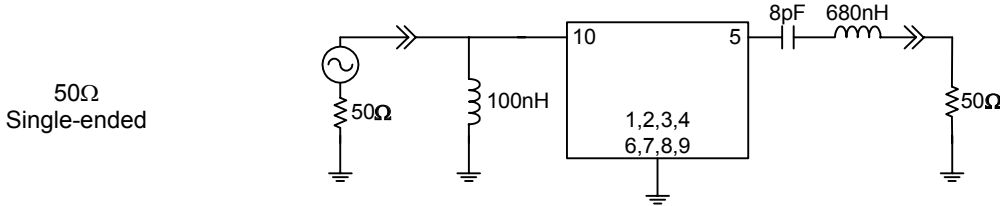
**Typical Performance (at +25°C)**



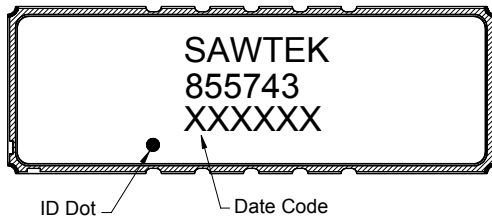
**Preliminary Data Sheet**

**Matching Schematics**

Actual matching values may vary due to PCB layout and parasitics

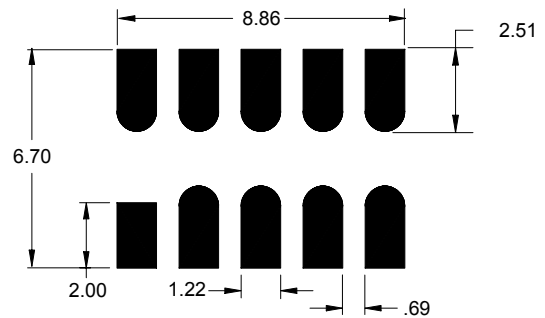


**Marking**



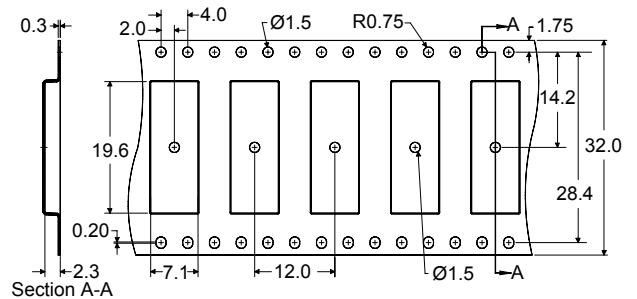
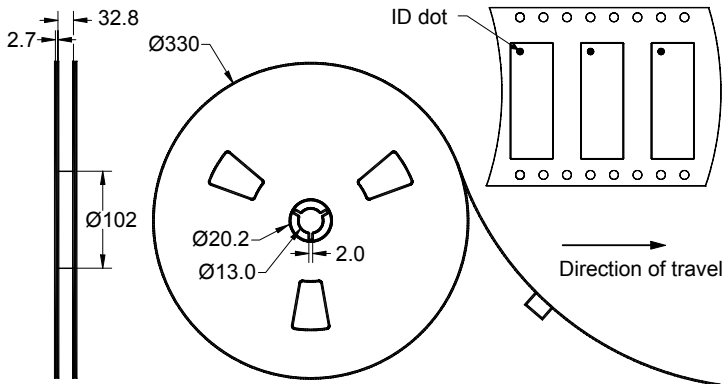
The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

**PCB Footprint**



This footprint represents a recommendation only  
Dimensions shown are nominal in millimeters

**Tape and Reel**



Dimensions shown are nominal in millimeters  
Packaging quantity: 2000 units/reel


# Preliminary Data Sheet

## Maximum Ratings


Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temperature Range	T	0	+25	+70	°C
Storage Temperature Range	T <sub>stg</sub>	-40	-	+85	°C

## Important Notes

### Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

### RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

### Solderability

- Compatible with JEDEC J-STD-020C **Pb**-free process, **260°C** peak reflow temperature ([see soldering profile](#))

## Links to Additional Technical Information

[PCB Layout Tips](#)
[Qualification Flowchart](#)
[Soldering Profile](#)
[S-Parameters](#)
[RoHS information](#)
[Other Technical Information](#)

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