
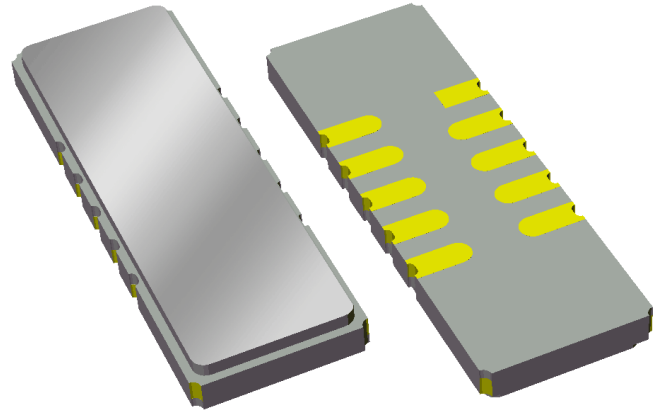


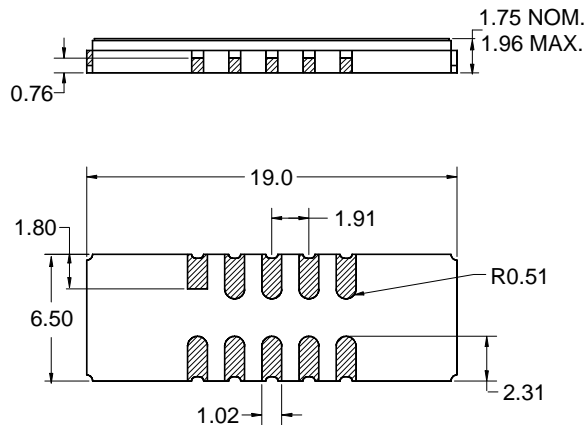
## Features

- For IF applications
- Typical 3dB bandwidth of 2 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851905 (BW 3dB = 2.0MHz)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



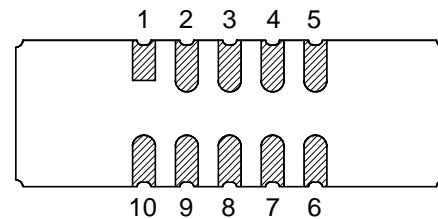
## Package

Surface Mount 19.00 x 6.50 x 1.75 mm  
SMP-75B



## Pin Configuration

Bottom View



### Single-ended Configuration

Pin No.	Description
10	RF input
5	RF output
1,6	Ground
2,3,4	Case Ground
7,8,9	Case Ground

Dimensions shown are nominal in millimeters  
All tolerances are  $\pm 0.15$ mm except overall  
length and width  $+0.15$ mm/ $-0.10$ mm

Body:  $Al_2O_3$  ceramic  
Lid: Kovar, Ni plated  
Terminations: Au plating 0.5 - 1.0 $\mu$ m,  
over a 2 - 6 $\mu$ m Ni plating

**Electrical Specifications <sup>(1)</sup>**

Operating Temperature Range: <sup>(2)</sup> 0 to +70 °C

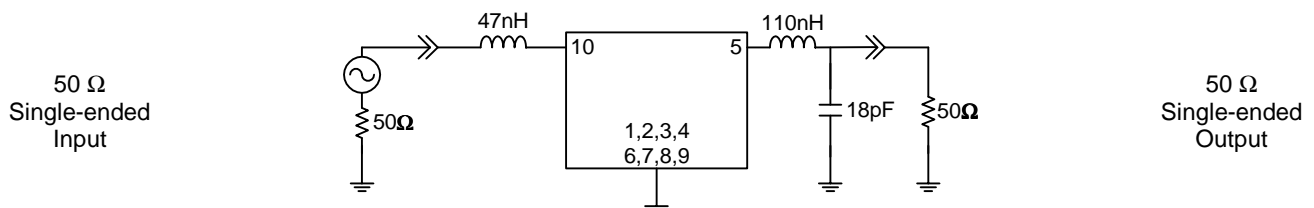
Parameter <sup>(3)</sup>	Minimum	Typical <sup>(4)</sup>	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	21.50	22.186	dB
Lower 1 dB Band Edge <sup>(5)</sup>	-	139.06	139.155	MHz
Upper 1 dB Band Edge <sup>(5)</sup>	140.845	140.94	-	MHz
Lower 3 dB Band Edge <sup>(5)</sup>	-	138.91	138.978	MHz
Upper 3 dB Band Edge <sup>(5)</sup>	141.022	141.09	-	MHz
Lower 40 dB Band Edge <sup>(5)</sup>	138.272	138.31	-	MHz
Upper 40 dB Band Edge <sup>(5)</sup>	-	141.67	141.726	MHz
Amplitude Variation 139.15 – 140.85 MHz	-	0.5	1.0	dB p-p
Phase Linearity 139.15 – 140.85 MHz	-	1.8	3.5	° p-p
Group Delay Variation 139.15 – 140.85 MHz	-	85	180	ns p-p
Relative Attenuation <sup>(5)</sup>				
15 – 136 MHz	60	64	-	dB
144 – 220 MHz	45	56	-	dB
220 – 230 MHz	38	46	-	dB
230 – 250 MHz	45	65	-	dB
250 – 260 MHz	26	31	-	dB
260 – 350 MHz	45	65	-	dB
Source Impedance (single-ended) <sup>(6)</sup>	-	50	-	Ω
Load Impedance (single-ended) <sup>(6)</sup>	-	50	-	Ω
Substrate Material	-	Quartz	-	-

**Notes:**

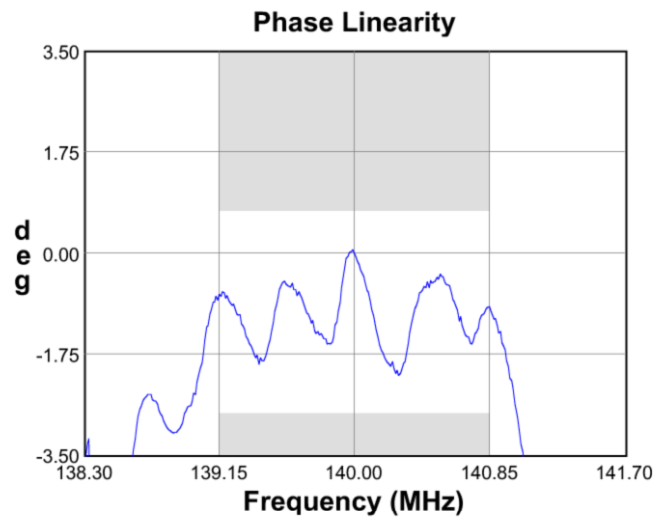
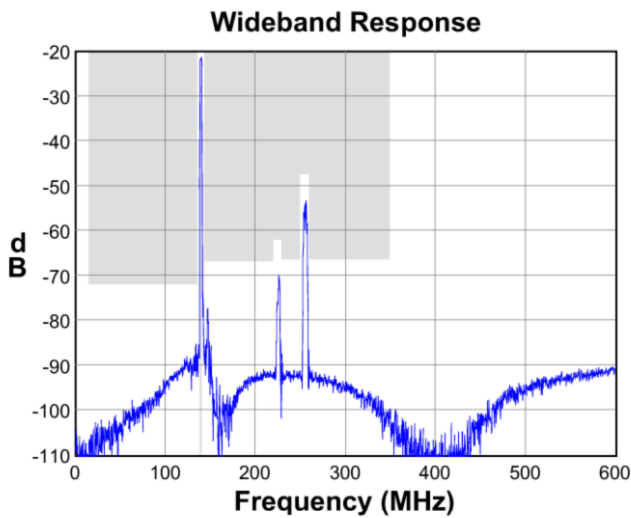
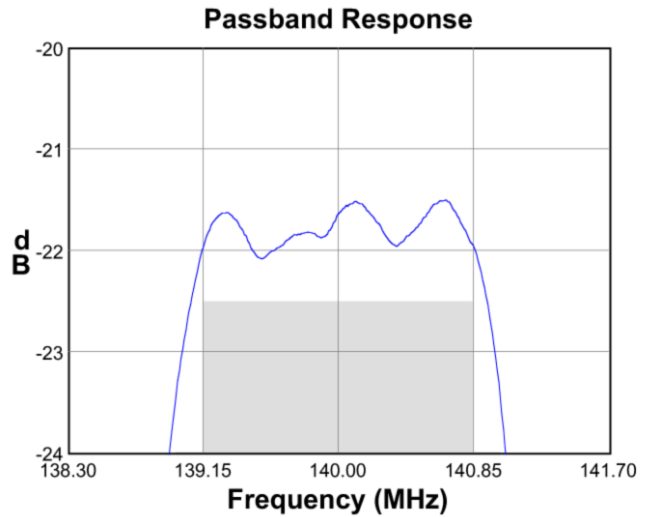
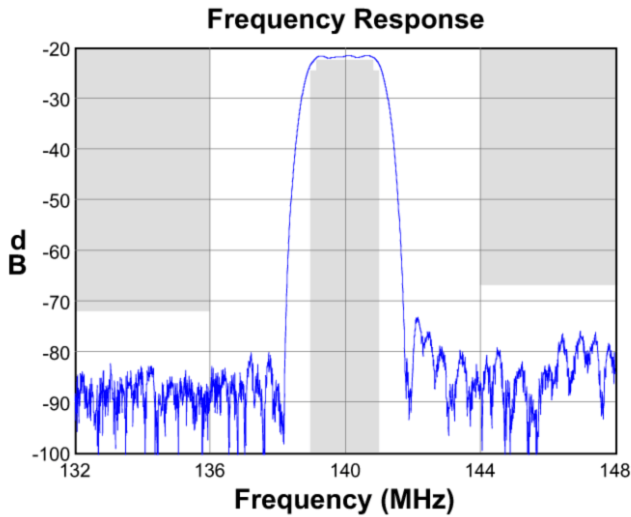
1. All specifications are based on the TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. Relative to minimum insertion loss
6. This is the optimum impedance in order to achieve the performance shown

**Test Circuit:**

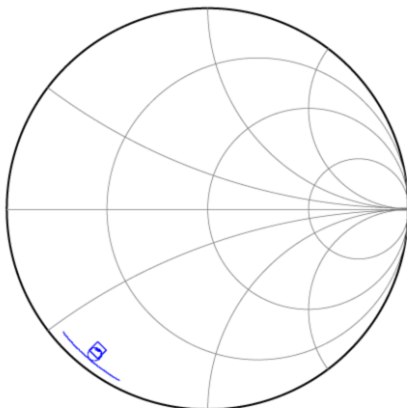
Actual matching values may vary due to PCB layout and parasitics



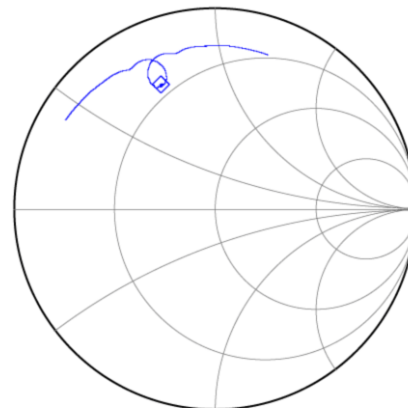
**Typical Performance (at room temperature)**



**Input Smith Chart**

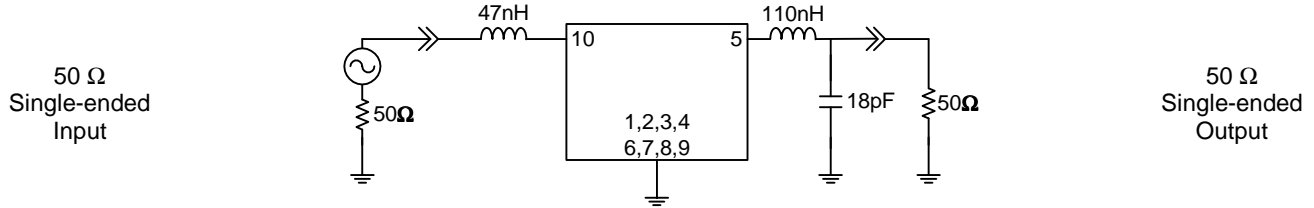


**Output Smith Chart**

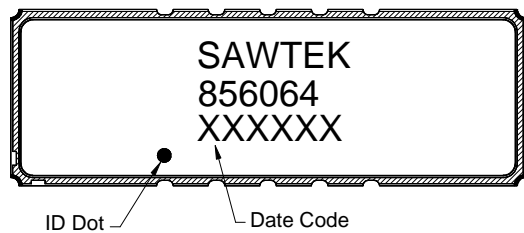


**Matching Schematics**

Actual matching values may vary due to PCB layout and parasitics

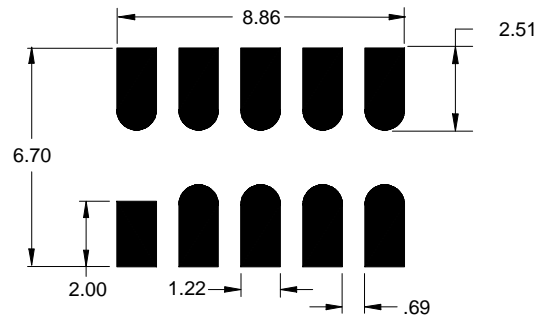


**Marking**



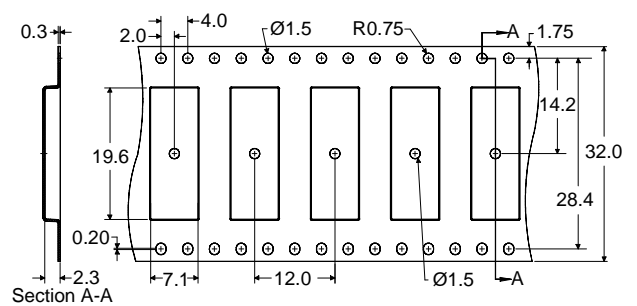
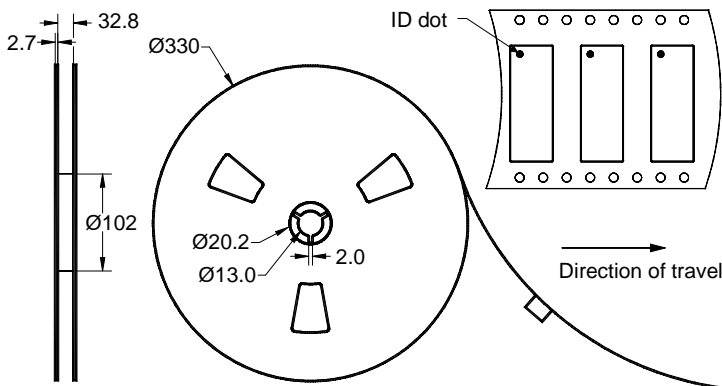
The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

**PCB Footprint**



This footprint represents a recommendation only  
Dimensions shown are nominal in millimeters

**Tape and Reel**




Dimensions shown are nominal in millimeters  
Packaging quantity: 2000 units/reel

### Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	0	+70	°C
Storage Temperature Range	T <sub>stg</sub>	-40	+85	°C

### Important Notes

#### Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

#### RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

#### Solderability

- Compatible with JESD22-B102, Pb-free process, 260C peak reflow temperature ([see soldering profile](#))

### Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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