
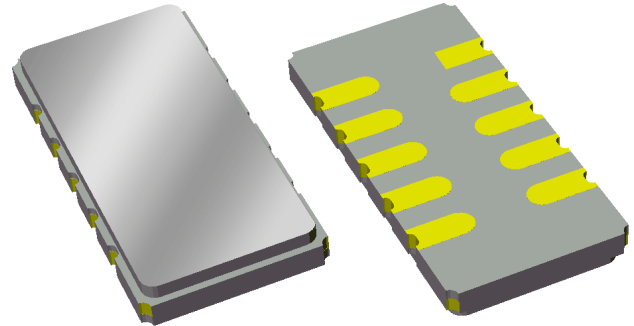


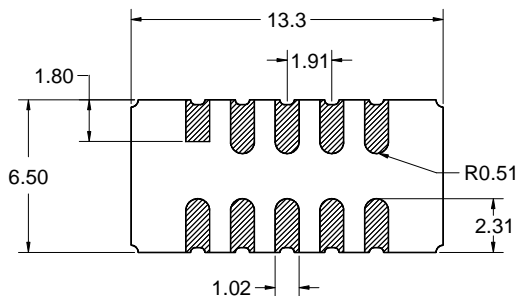
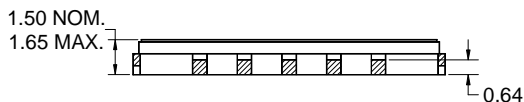
## Features

- For broadband applications
- Typical 3 dB bandwidth of 10 MHz
- High attenuation
- No impedance matching required for operation at 50  $\Omega$
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851921 (BW 3dB=10 MHz)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



## Package

Surface Mount 13.3 x 6.50 x 1.50 mm  
SMP-53C

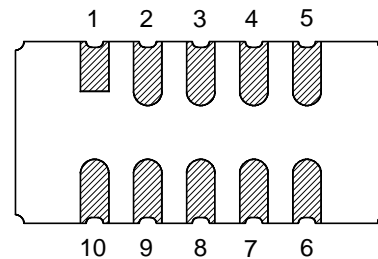


Dimensions shown are nominal in millimeters  
All tolerances are  $\pm 0.15$ mm except overall  
length and width  $\pm 0.10$ mm

Body:  $Al_2O_3$  ceramic  
Lid: Kovar, Ni plated  
Terminations: Au plating 0.5 - 1.0 $\mu$ m,  
over a 2 - 6 $\mu$ m Ni plating

## Pin Configuration

Bottom View



### Single-ended Configuration

Pin No.	Description
10	RF Input
5	RF Output
1,6	Ground
2,3,4	Case Ground
7,8,9	Case Ground

**Electrical Specifications <sup>(1)</sup>**

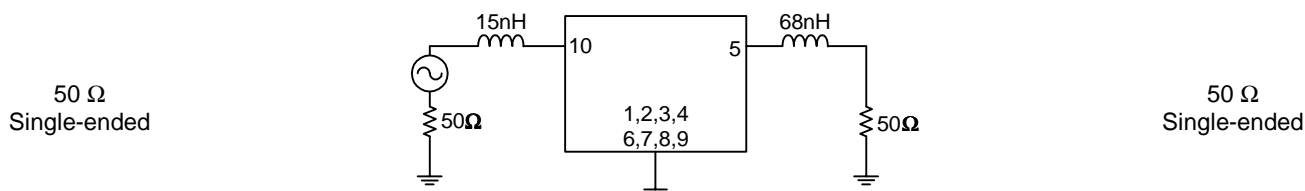
Operating Temperature Range: <sup>(2)</sup> -30 to +85 °C

Parameter <sup>(3)</sup>	Minimum	Typical <sup>(4)</sup>	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	20.87	21.7	dB
Lower 1 dB Bandedge <sup>(5)</sup>	-	135.38	135.524	MHz
Upper 1 dB Bandedge	144.508	144.79	-	MHz
Lower 3 dB Bandedge <sup>(5)</sup>	-	135.00	135	MHz
Upper 3 dB Bandedge	145	145.24	-	MHz
Lower 40 dB Bandedge <sup>(5)</sup>	133.379	133.85	-	MHz
Upper 40 dB Bandedge	-	146.72	146.551	MHz
Amplitude Variation 135.524 - 144.508 MHz	-	0.7	0.94	dB
Phase Linearity 135.524 - 144.508 MHz	-	5	6.31	deg
Group Delay Variation 135.524 - 144.508 MHz	-	45	57.3	nsec
Absolute Delay	-	1.52	-	µsec
Relative Attenuation <sup>(5)</sup>				
15 - 130 MHz	47.8	50	-	dB
130 - 133 MHz	52	57	-	dB
147 - 150 MHz	50.6	53	-	dB
150 - 350 MHz	51.3	53	-	dB
Source Impedance <sup>(6)</sup>	-	50	-	Ω
Load Impedance <sup>(6)</sup>	-	50	-	Ω
Substrate Material	-	LINbO <sub>3</sub>	-	-
Temperature Coefficient of Frequency	-	-94	-	ppm/°C

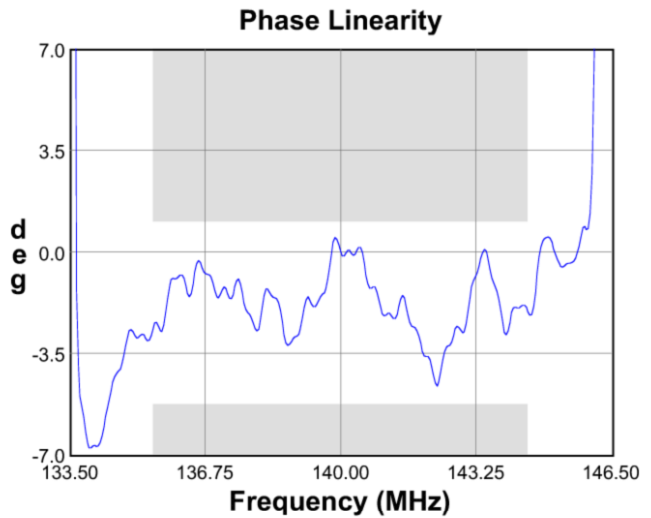
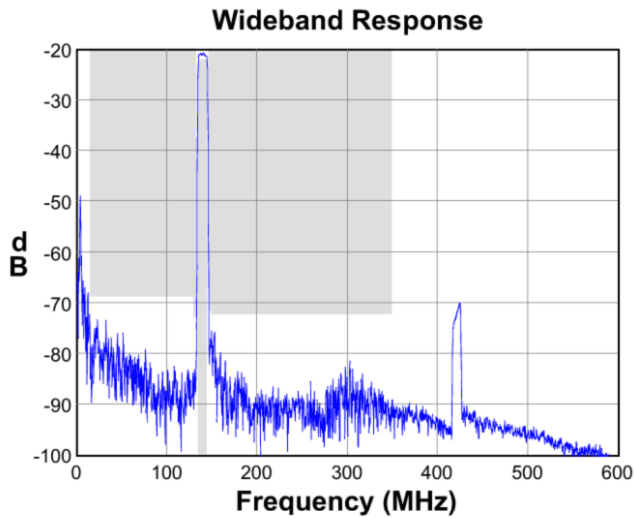
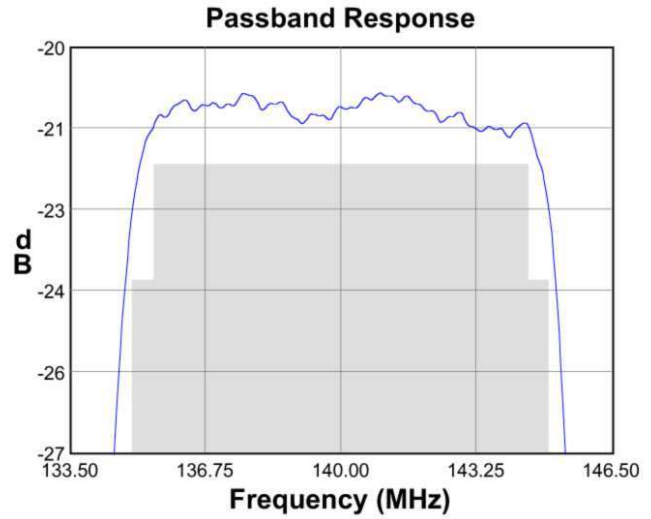
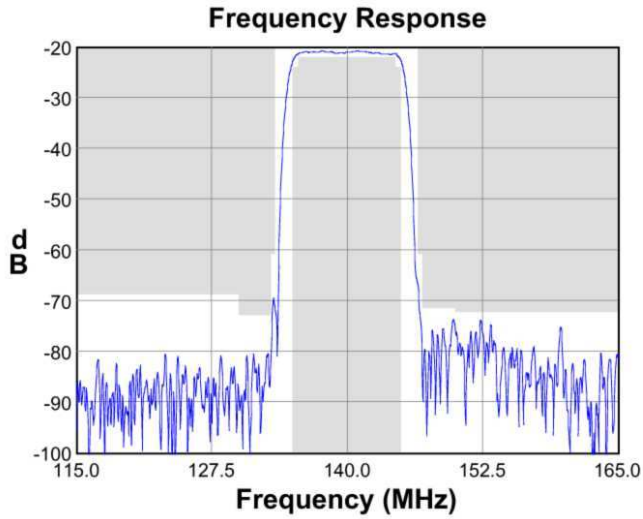
**Notes:**

1. All specifications are based on the TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. All attenuation measurements are measured relative to minimum insertion loss
6. This is the optimum impedance in order to achieve the performance shown

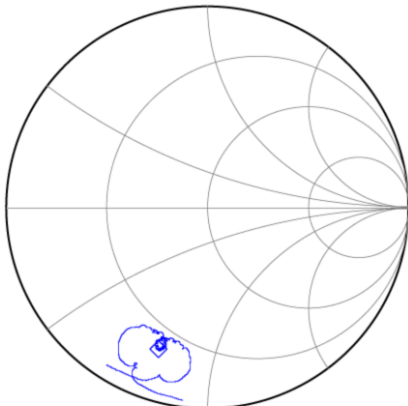
**Test Circuit:**



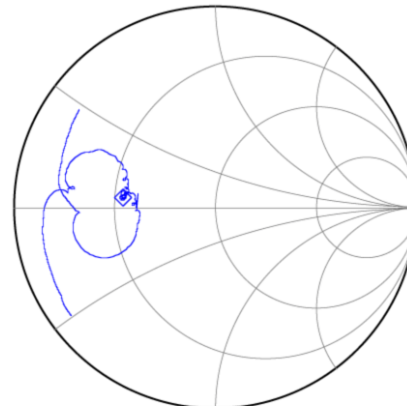
**Typical Performance (at room temperature)**



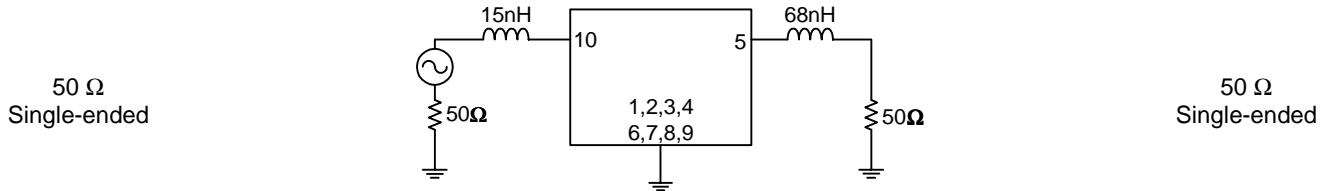
**Input Smith Chart**



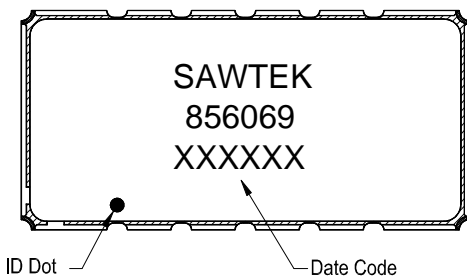
**Output Smith Chart**



**Matching Schematics**

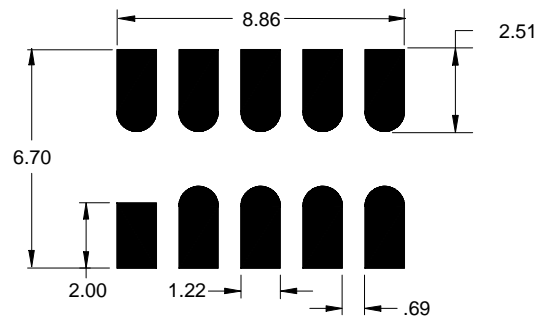


**Marking**



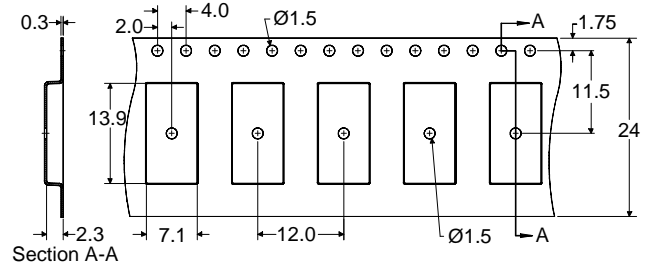
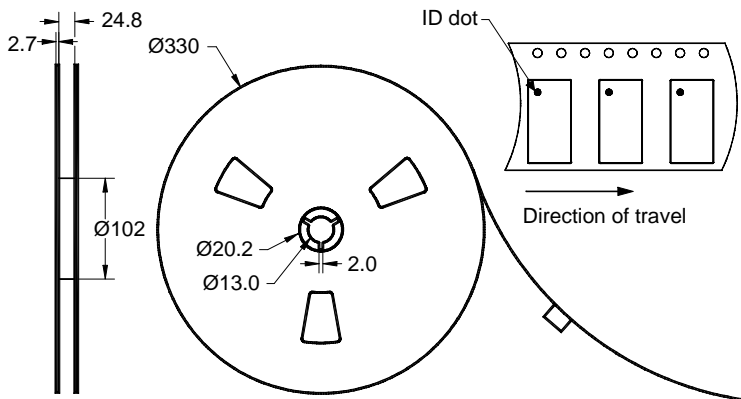
The date code consists of: JJJ = Julian day,  
Y = last digit of year, M = manufacturing site code

**PCB Footprint**



This footprint represents a recommendation only  
Dimensions shown are nominal in millimeters

**Tape and Reel**



Dimensions shown are nominal in millimeters  
Packaging quantity:2000 units/reel

### Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-30	+85	°C
Storage Temperature Range	T <sub>stg</sub>	-40	+85	°C

### Important Notes

#### Warnings

- Electrostatic Sensitive Device (ESD)
- Avoid ultrasonic exposure



#### RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS)



#### Solderability

- Compatible with JESD22-B102, Pb-free process, 260C peak reflow temperature ([see soldering profile](#))

### Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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