
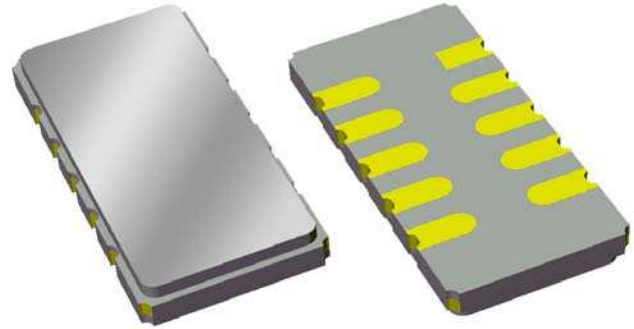


Preliminary Data Sheet

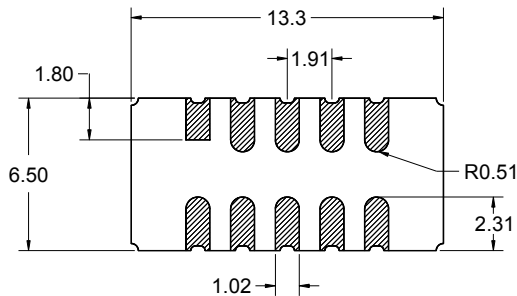
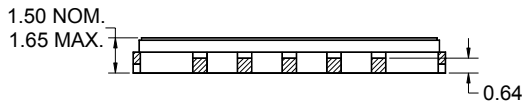
Features

- For broadband applications
- Typical 3 dB bandwidth of 14.1 MHz
- High attenuation
- No impedance matching required for operation at 50 Ω
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851925 (BW 3dB=14 MHz)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



Package

Surface Mount 13.30 x 6.50 x 1.50 mm

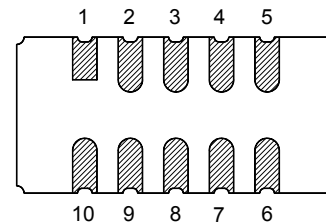


Dimensions shown are nominal in millimeters
 All tolerances are ±0.15mm except overall
 length and width ±0.10mm

Body: Al_2O_3 ceramic
 Lid: Kovar, Ni plated
 Terminations: Au plating 0.5 - 1.0μm,
 over a 2 - 6μm Ni plating

Pin Configuration

Bottom View



Pin No.	Description
5	Output
10	Input
1,6	Ground
2,3,4	Case ground
7,8,9	Case ground

Preliminary Data Sheet

Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ 0 to +70 °C

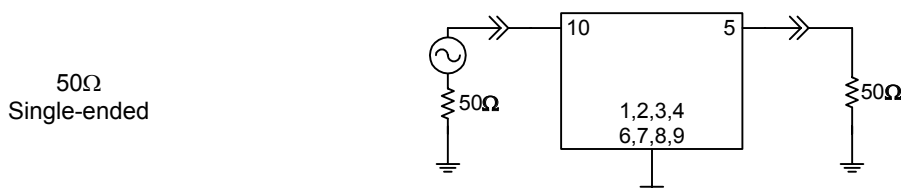
Parameter ⁽³⁾	Minimum	Typical	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	23.3	24.5	dB
Lower 1 dB Bandedge ⁽⁴⁾	-	133.26	134.11	MHz
Upper 1 dB Bandedge	145.89	146.67	-	MHz
Lower 3 dB Bandedge ⁽⁴⁾	-	132.93	133.77	MHz
Upper 3 dB Bandedge	146.23	147.00	-	MHz
Lower 40 dB Bandedge ⁽⁴⁾	130.87	131.58	-	MHz
Upper 40 dB Bandedge	-	148.33	149.13	MHz
Amplitude Variation 134.11 - 145.89 MHz	-	0.31	0.70	dB
Phase Linearity 134.11 - 145.89 MHz	-	2.06	6.00	deg
Group Delay Variation 134.11 - 145.89 MHz	-	27	55	nsec
Absolute Delay	-	1.50	-	μsec
Relative Attenuation ⁽⁴⁾				
15 - 50 MHz	42	49	-	dB
50 - 127 MHz	48	55	-	dB
156 - 240 MHz	48	53	-	dB
240 - 290 MHz	43	49	-	dB
290 - 310 MHz	42	48	-	dB
310 - 350 MHz	44	48	-	dB
Source Impedance ⁽⁵⁾	-	50	-	Ω
Load Impedance ⁽⁵⁾	-	50	-	Ω
Substrate Material	-	YZ LiNbO ₃	-	-
Temperature Coefficient of Frequency	-	-94	-	ppm/°C

Notes:

- All specifications are based on the test circuit shown below
- In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
- Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
- All attenuation measurements are measured relative to minimum insertion loss
- This is the optimum impedance in order to achieve the performance shown

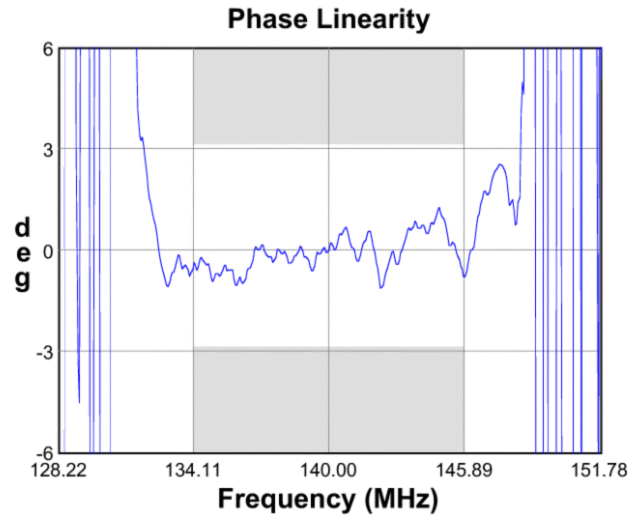
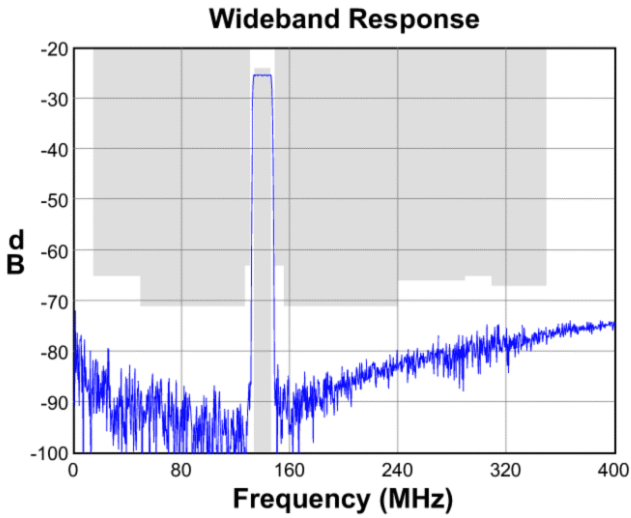
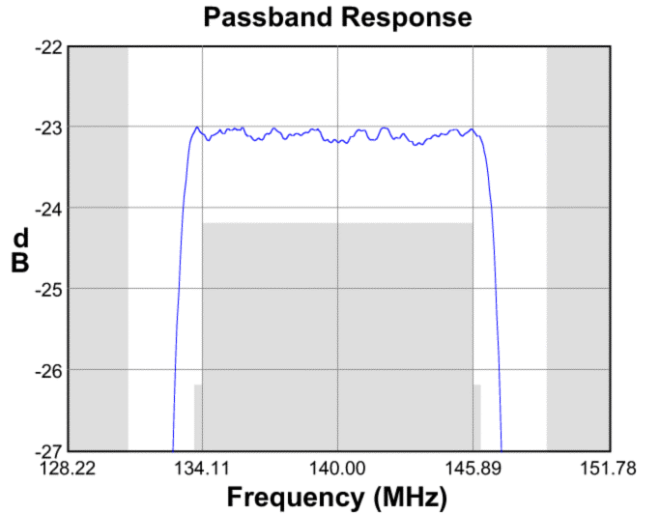
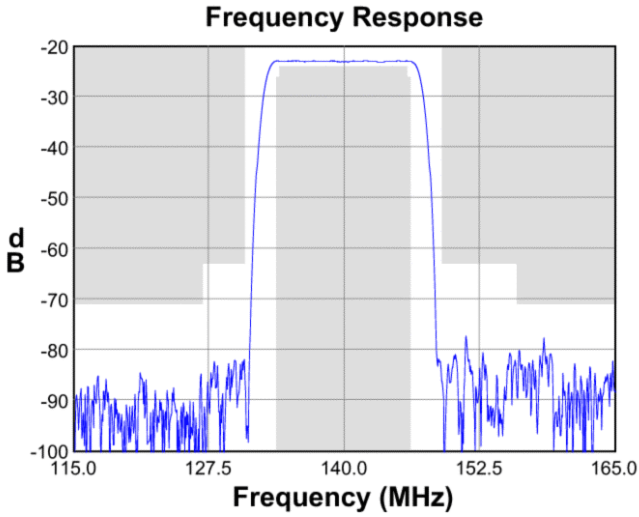
Test Circuit:

Actual matching values may vary due to PCB layout and parasitics

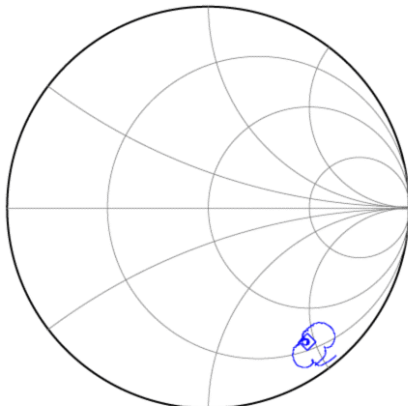


Preliminary Data Sheet

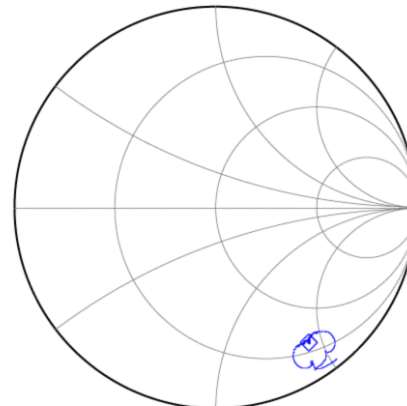
Typical Performance (at +25°C)



Input Smith Chart



Output Smith Chart

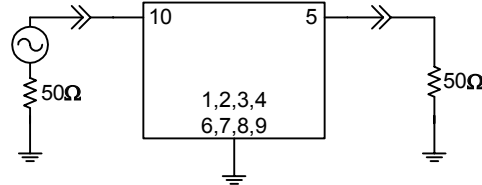


Preliminary Data Sheet

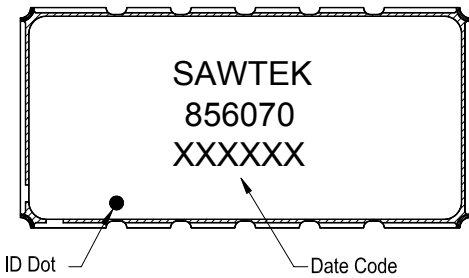
Matching Schematics

Actual matching values may vary due to PCB layout and parasitics

50Ω
Single-ended

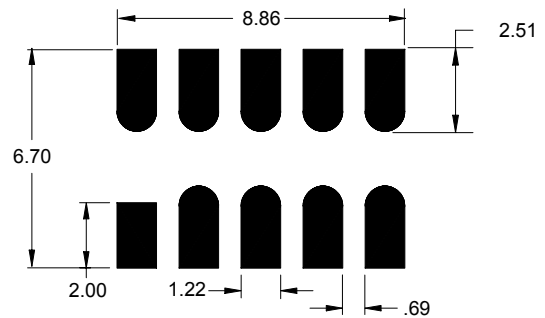


Marking



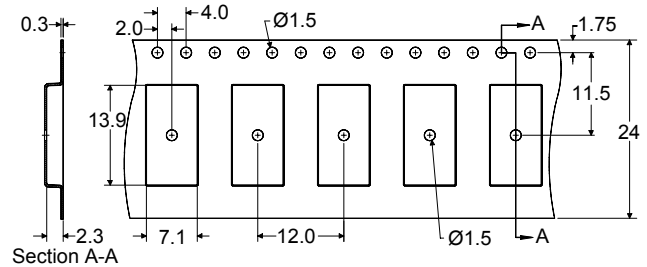
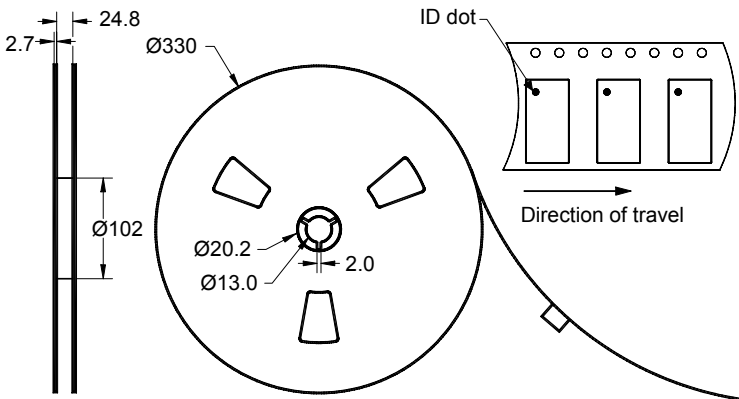
The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

PCB Footprint



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel



Dimensions shown are nominal in millimeters
Packaging quantity: 2000 units/reel


Preliminary Data Sheet

Maximum Ratings


Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temperature Range	T	0	+25	+70	°C
Storage Temperature Range	T _{stg}	-40	-	+85	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JEDEC J-STD-020C **Pb**-free process, **260°C** peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)
[Qualification Flowchart](#)
[Soldering Profile](#)
[S-Parameters](#)
[RoHS Information](#)
[Other Technical Information](#)

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[representatives or distributors](#)