
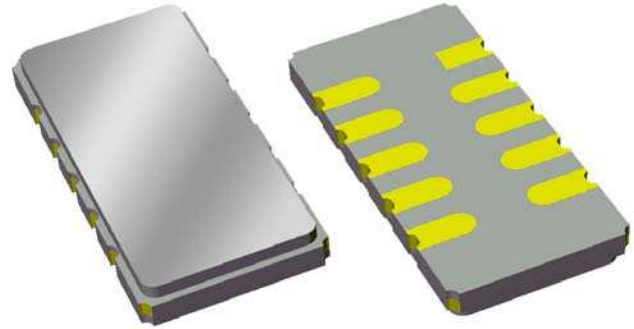


# Data Sheet

## Features

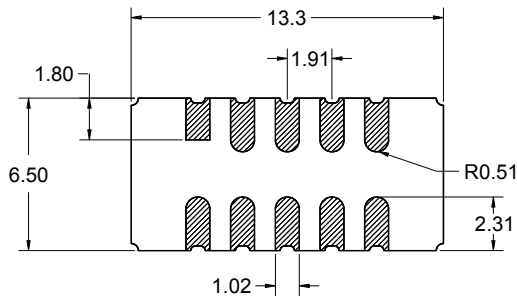
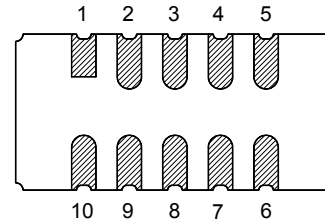
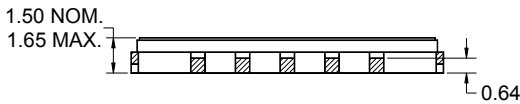
- For broadband applications
- Typical 3 dB bandwidth of 16.2 MHz
- High attenuation
- Single-ended operation
- Ceramic Surface Mount Package (SMP)
- Replaces Sawtek P/N 851927 (BW 3dB=16 MHz)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



## Package Pin Configuration

Surface Mount 13.30 x 6.50 x 1.50 mm

Bottom View



Pin No.	Description
5	Output
10	Input
1,6	Ground
2,3,4	Case ground
7,8,9	Case ground

Dimensions shown are nominal in millimeters  
 All tolerances are  $\pm 0.15$ mm except overall  
 length and width  $\pm 0.10$ mm

Body:  $Al_2O_3$  ceramic  
 Lid: Kovar, Ni plated  
 Terminations: Au plating 0.5 - 1.0 $\mu$ m,  
 over a 2 - 6 $\mu$ m Ni plating

# Data Sheet

## Electrical Specifications <sup>(1)</sup>

Operating Temperature Range: <sup>(2)</sup> 0 to +70 °C

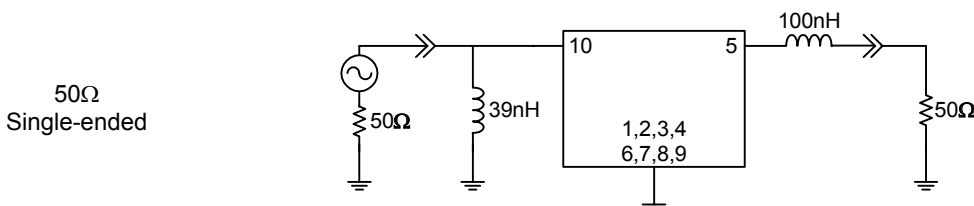
Parameter <sup>(3)</sup>	Minimum	Typical	Maximum	Unit
Center Frequency	-	140	-	MHz
Minimum Insertion Loss	-	21.7	22.5	dB
Lower 1 dB Bandedge <sup>(4)</sup>	-	132.32	133.01	MHz
Upper 1 dB Bandedge	146.99	147.77	-	MHz
Lower 3 dB Bandedge <sup>(4)</sup>	-	131.93	132.6	MHz
Upper 3 dB Bandedge	147.4	148.14	-	MHz
Lower 40 dB Bandedge <sup>(4)</sup>	129.656	130.33	-	MHz
Upper 40 dB Bandedge	-	149.67	150.344	MHz
Amplitude Variation 133.01 - 146.99 MHz	-	0.44	0.87	dB
Phase Linearity 133.01 - 146.99 MHz	-	2.99	5.67	deg
Group Delay Variation 133.01 - 146.99 MHz	-	30	52	nsec
Absolute Delay	-	1.09	-	µsec
Relative Attenuation <sup>(4)</sup>				
15 - 100 MHz	53	58	-	dB
100 - 125 MHz	49.5	53	-	dB
155 - 175 MHz	46	50	-	dB
175 - 270 MHz	47.5	55	-	dB
270 - 280 MHz	38	46	-	dB
280 - 350 MHz	49	57	-	dB
Source Impedance <sup>(5)</sup>	-	50	-	Ω
Load Impedance <sup>(5)</sup>	-	50	-	Ω
Substrate Material	-	YZ LiNbO <sub>3</sub>	-	-
Temperature Coefficient of Frequency	-	-94	-	ppm/°C

### Notes:

- All specifications are based on the test circuit shown below
- In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
- Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
- All attenuation measurements are measured relative to minimum insertion loss
- This is the optimum impedance in order to achieve the performance shown

### Test Circuit:

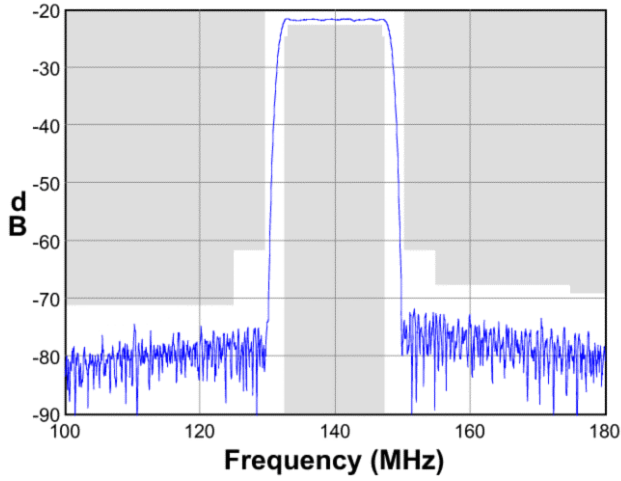
Actual matching values may vary due to PCB layout and parasitics



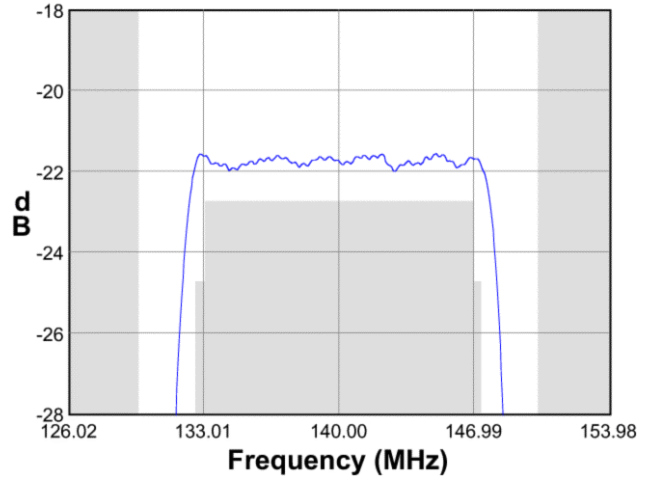
**Data Sheet**

**Typical Performance (at +25°C)**

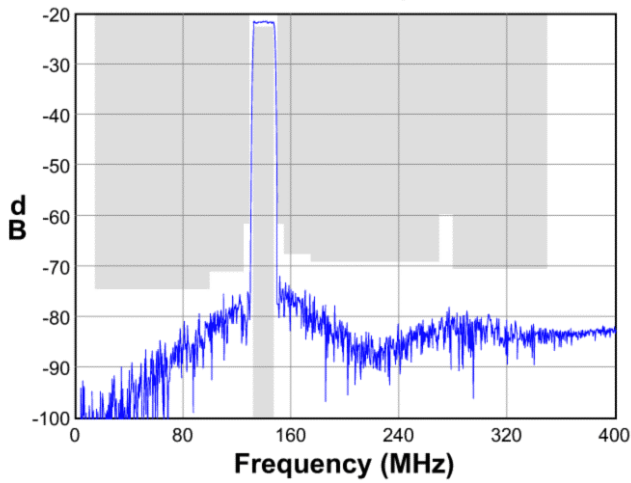
**Frequency Response**



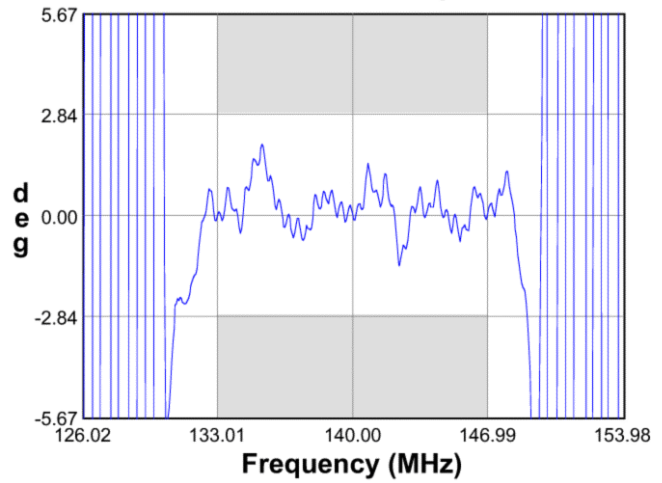
**Passband Response**



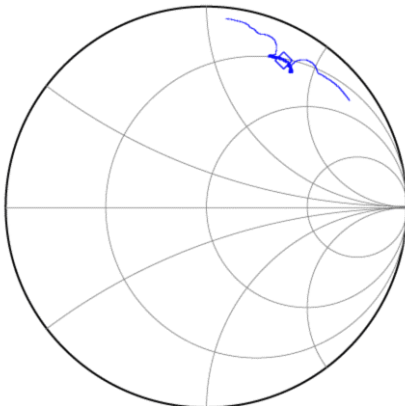
**Wideband Response**



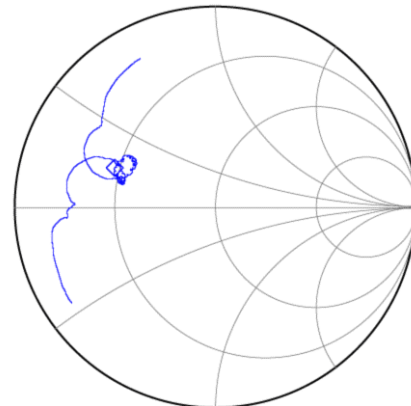
**Phase Linearity**



**Input Smith Chart**



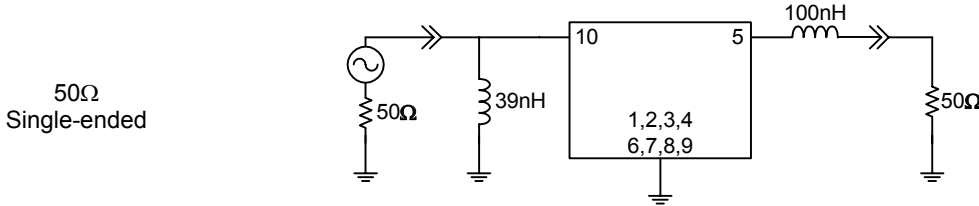
**Output Smith Chart**



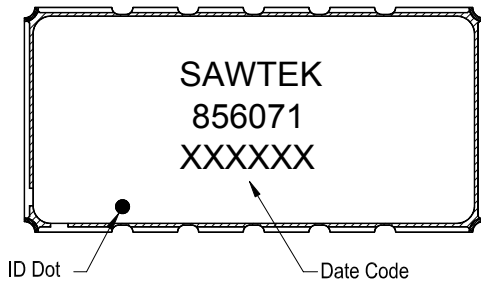
**Data Sheet**

**Matching Schematics**

Actual matching values may vary due to PCB layout and parasitics

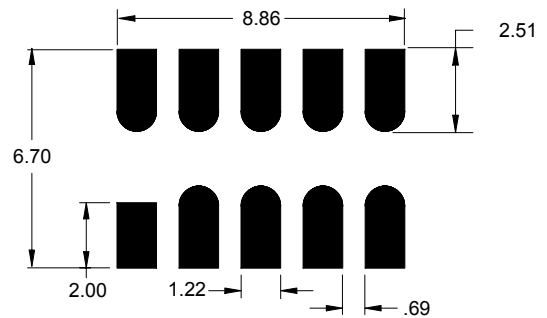


**Marking**



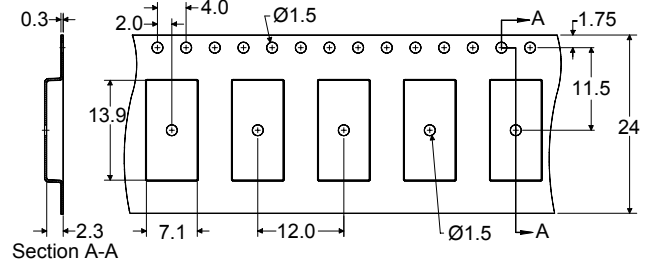
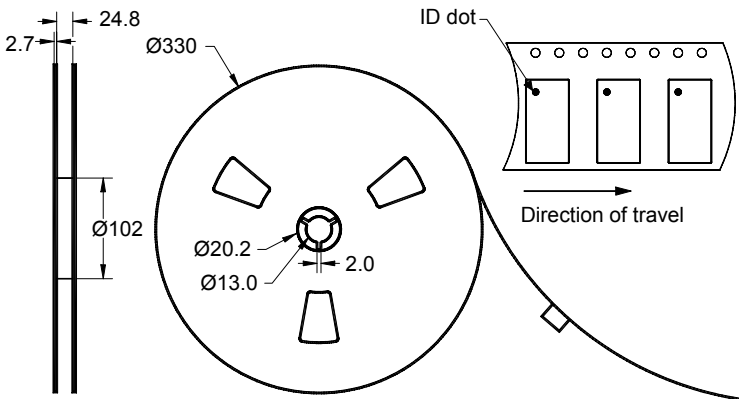
The date code consists of: day of the current year (Julian, 3 digits), last digit of the year (1 digit) and hour (2 digits)

**PCB Footprint**



This footprint represents a recommendation only  
Dimensions shown are nominal in millimeters

**Tape and Reel**



Dimensions shown are nominal in millimeters  
Packaging quantity: 2000 units/reel


# Data Sheet

## Maximum Ratings


Parameter	Symbol	Minimum	Typical	Maximum	Unit
Operating Temperature Range	T	0	+25	+70	°C
Storage Temperature Range	T <sub>stg</sub>	-40	-	+85	°C

## Important Notes

### Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

### RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

### Solderability

- Compatible with JEDEC J-STD-020C **Pb-free** process, **260°C** peak reflow temperature ([see soldering profile](#))

## Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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