
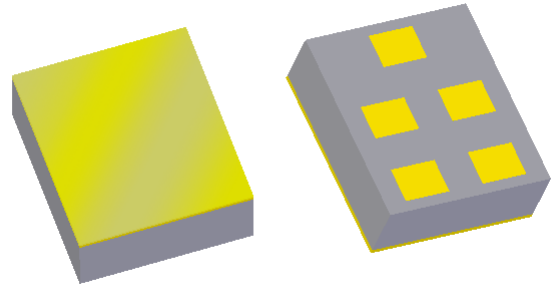


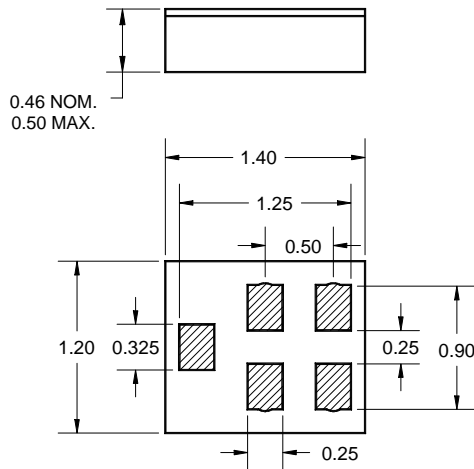
Features

- For GPS applications
- Usable bandwidth of 2 MHz
- Compatible with leading chipset suppliers
- Low loss
- Single-ended operation
- Ceramic Chip Scale Package (CSP)
- Hermetic
- Suitable for Automotive applications - Compliant to the AEC-Q200 reliability standard
- Manufacturing facilities are certified with ISO/TS 16949:2002
- **RoHS** compliant (2002/95/EC), **Pb-free** 



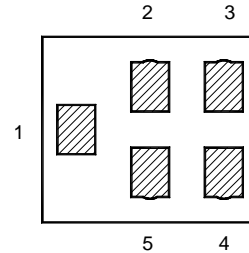
Package

Surface Mount 1.40 x 1.20 x 0.46 mm
CSP-5BT



Pin Configuration

Bottom View



Pin No.	Description
1	Input
4	Output
3	Ground
2,5	Case ground

Dimensions shown are nominal in millimeters
All tolerances are ± 0.10 mm

Body: Al_2O_3 ceramic
Lid: Kovar or Alloy 42, Au over Ni plated
Terminations: Au plating 0.5 - 1.0 μ m,
over a 2 - 6 μ m Ni plating

Data Sheet

Electrical Specifications ⁽¹⁾

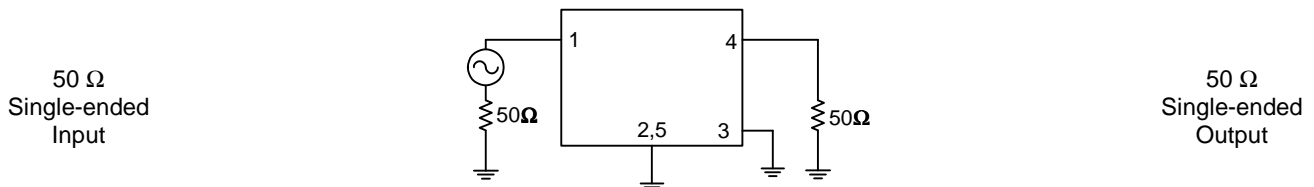
Operating Temperature Range: ⁽²⁾ -30 to +85 °C

Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	1575.42	-	MHz
Insertion Loss				
1574.42 - 1576.42 MHz	-	0.75	1.2	dB
1574.42 - 1576.42 MHz (-40 to +85 °C)	-	0.75	1.4	dB
Absolute Attenuation ⁽⁵⁾				
0.1 - 824 MHz	32	36	-	dB
824 - 849 MHz	33.5	36	-	dB
849 - 960 MHz	32	36	-	dB
1495 - 1515 MHz	25	31	-	dB
1635 - 1655 MHz	35	40	-	dB
1710 - 1750 MHz	35	39	-	dB
1750 - 1780 MHz	35	39	-	dB
1780 - 1785 MHz	35	39	-	dB
1850 - 1910 MHz	35	39	-	dB
1920 - 1980 MHz	35	39	-	dB
2402 - 2480 MHz	25	35	-	dB
3000 - 4000 MHz	10	15	-	dB
4000 - 6000 MHz	10	15	-	dB
Input/Output Return Loss				
1574.42 - 1576.42 MHz	-	1.4	2.0	-
Source Impedance ⁽⁶⁾	-	50	-	Ω
Load Impedance ⁽⁶⁾	-	50	-	Ω

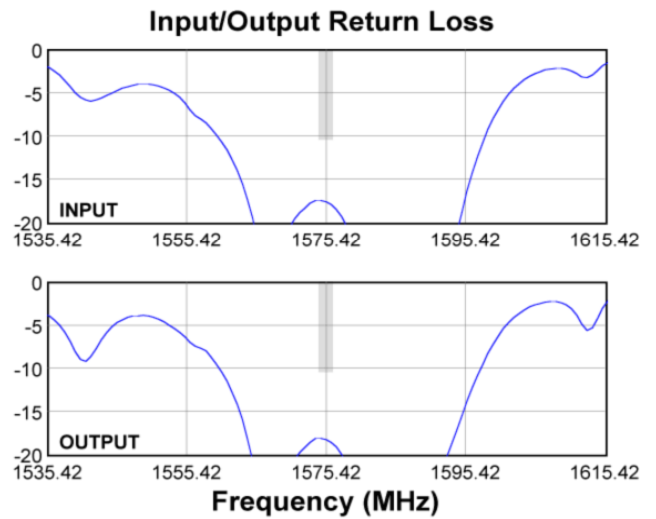
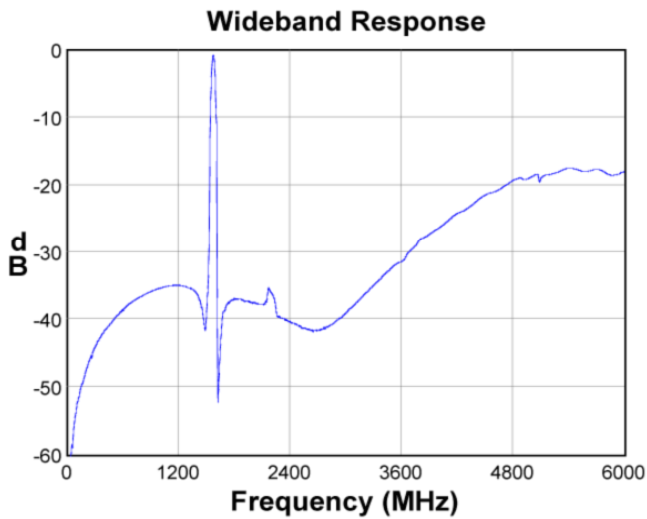
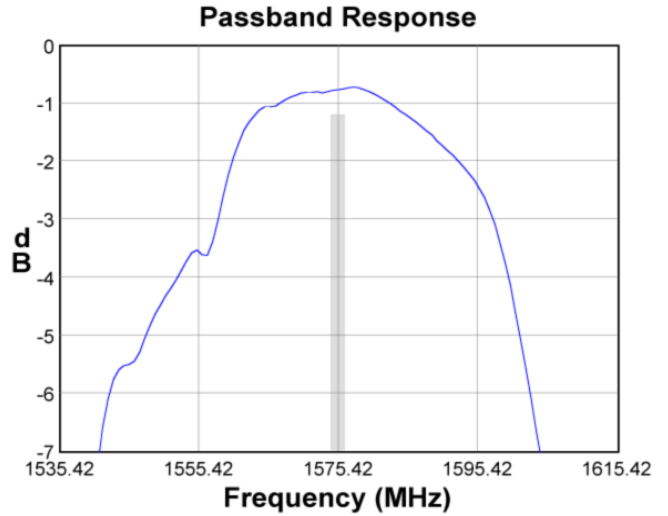
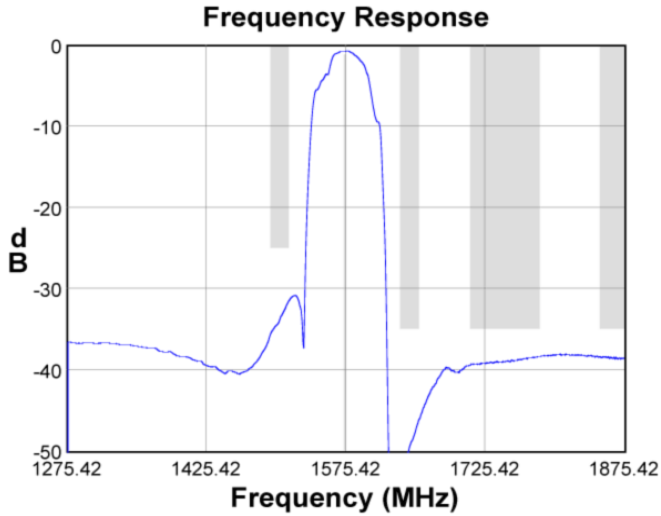
Notes:

1. All specifications are based on the TriQuint test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements at room temperature
5. Relative to zero dB
6. This is the optimum impedance in order to achieve the performance shown

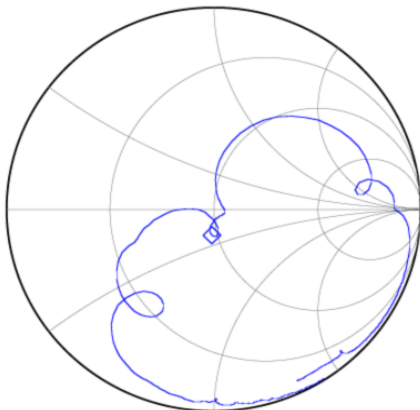
Test Circuit:



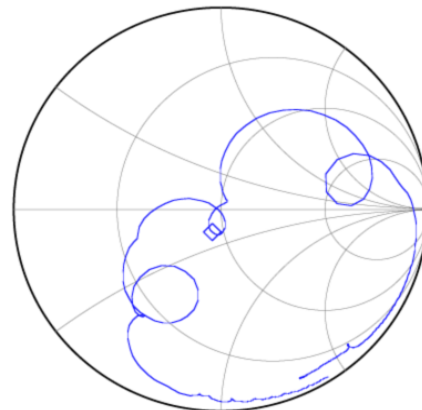
Typical Performance (at room temperature)



Input Smith Chart

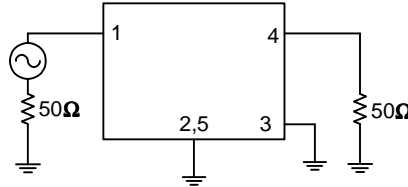


Output Smith Chart



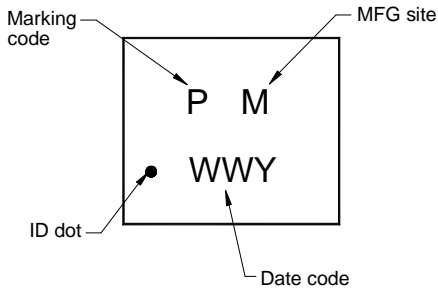
Matching Schematics

50 Ω
Single-ended
Input



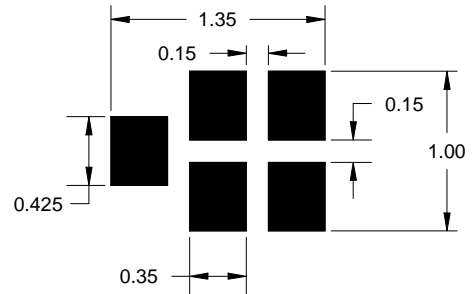
50 Ω
Single-ended
Output

Marking



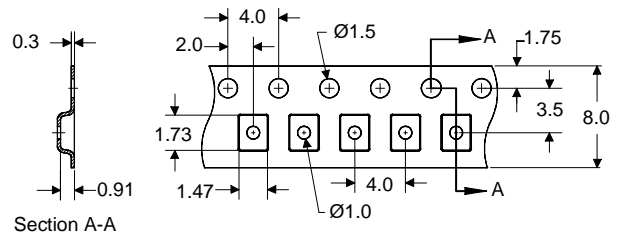
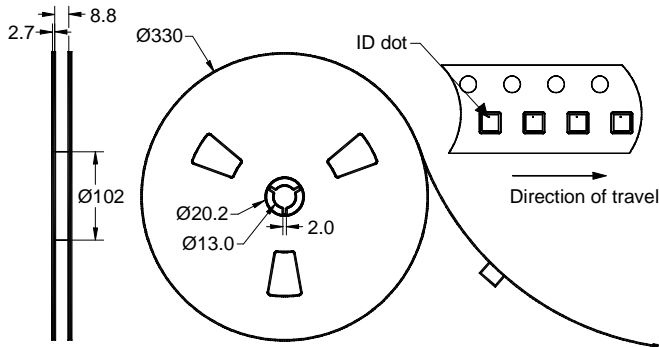
The date code consists of: WW = 2 digit week,
Y = last digit of year, M = manufacturing site code

PCB Footprint



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel



Dimensions shown are nominal in millimeters
Packaging quantity: 10000 units/reel


Data Sheet

Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-30	+85	°C
Storage Temperature Range	T _{stg}	-40	+85	°C
Power Handling (10,000 hours at +55 °C)	P _{in}			
824 - 849 MHz		-	+20	dBm
1850 - 1910 MHz		-	+20	dBm

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JESD22-B102 **Pb**-free process, **260°C** peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS information](#)

[Other Technical Information](#)

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[Representatives or distributors](#)

