
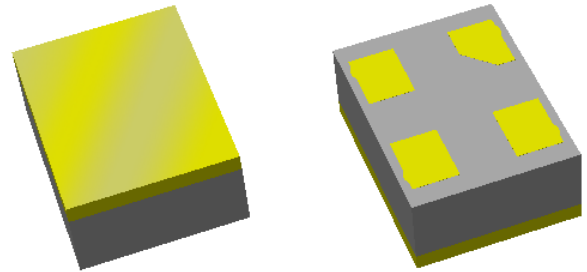


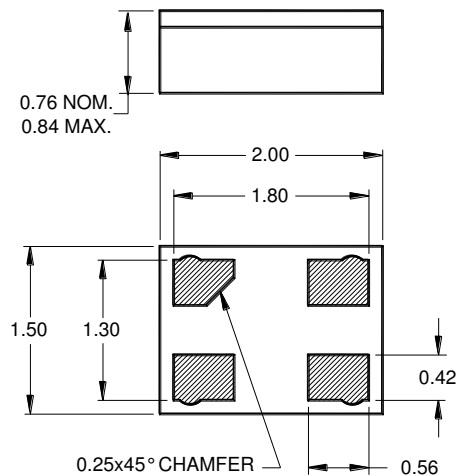
Features

- For Base Station applications
- Usable bandwidth 13 MHz
- Low loss
- Single-ended operation
- Ceramic Chip Scale Package (CSP)
- Hermetic
- RoHS compliant (2002/95/EC), Pb-free 



Package

Surface Mount 2.00 x 1.50 x 0.76 mm
CSP-8A

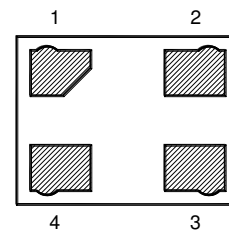


Dimensions shown are nominal in millimeters
All tolerances are ± 0.10 mm

Body: Al_2O_3 ceramic
Lid: Kovar or Alloy 42, Au over Ni plated
Terminations: Au plating 0.5 - 1.0 μ m,
over a 2 - 6 μ m Ni plating

Pin Configuration

Bottom View



Pin No.	Description
1	Input
3	Output
2,4	Case ground

Electrical Specifications ⁽¹⁾

Operating Temperature Range: ⁽²⁾ -40 to +85 °C

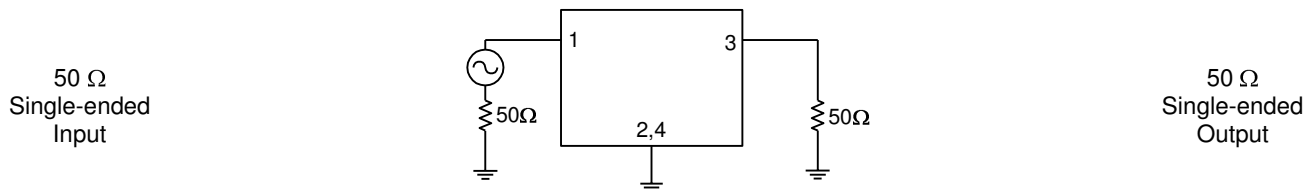
Parameter ⁽³⁾	Minimum	Typical ⁽⁴⁾	Maximum	Unit
Center Frequency	-	921.5	-	MHz
Maximum Insertion Loss 915 – 928 MHz	-	1.9	3.0	dB
Absolute Attenuation ⁽⁵⁾				
10 – 857.5 MHz	40	50.7	-	dB
857.5 – 895 MHz	35	41.1	-	dB
970 – 1005 MHz	35	46.7	-	dB
1005 – 1110 MHz	40	53.6	-	dB
1110 – 3000 MHz	30	35.2	-	dB
Amplitude Variation 915 – 928 MHz	-	0.3	1.0	dB p-p
Group Delay Variation 915 – 928 MHz	-	28.0	50	ns p-p
Input/Output Return Loss 915 – 928 MHz	10	13.1	-	dB
Source Impedance (single-ended) ⁽⁶⁾	-	50	-	Ω
Load Impedance (single-ended) ⁽⁶⁾	-	50	-	Ω

Notes:

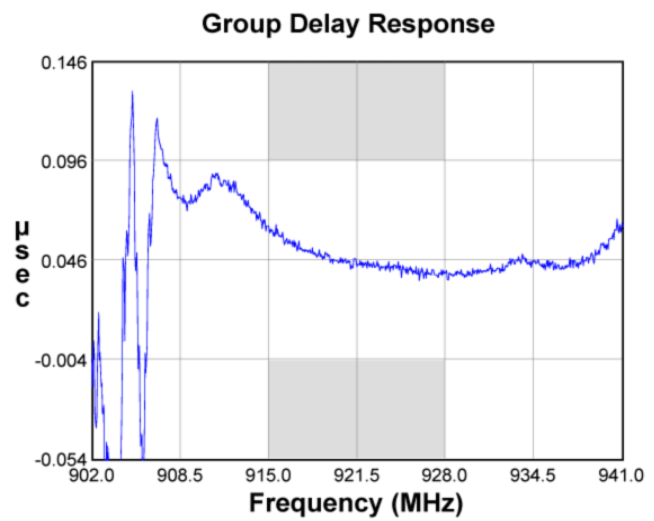
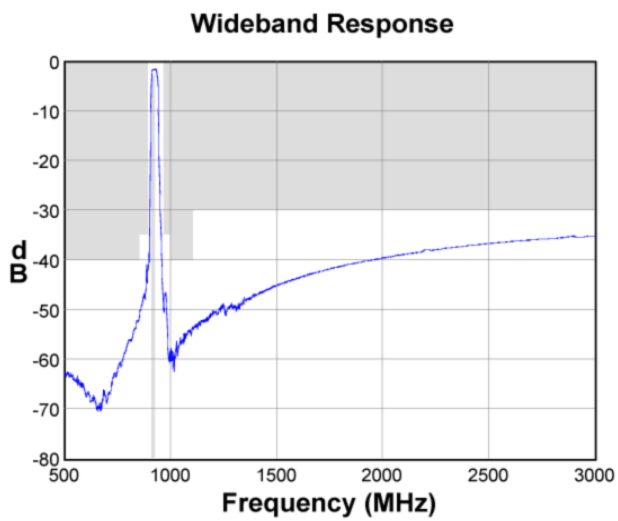
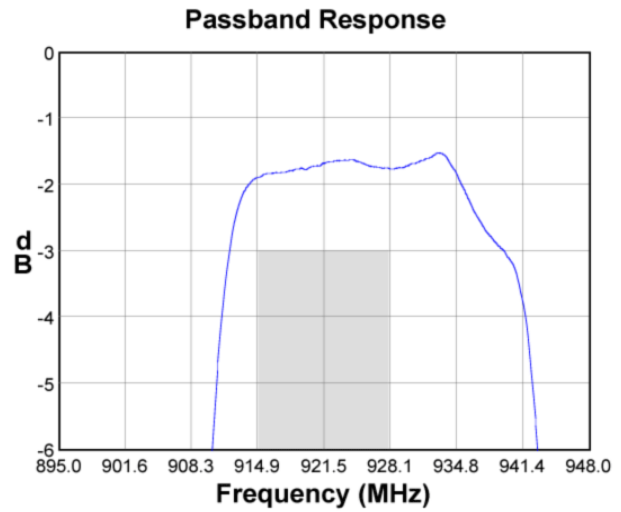
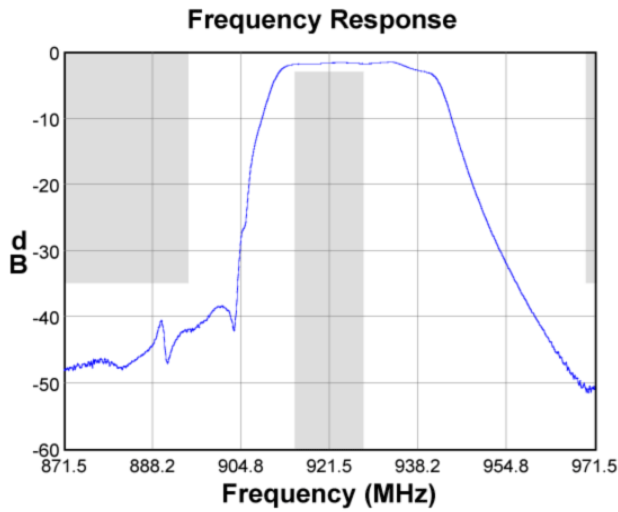
1. All specifications are based on the test circuit shown below
2. In production, devices will be tested at room temperature to a guardbanded specification to ensure electrical compliance over temperature
3. Electrical margin has been built into the design to account for the variations due to temperature drift and manufacturing tolerances
4. Typical values are based on average measurements on pcb at room temperature, unless otherwise noted
5. Relative to zero dB
6. This is the optimum impedance in order to achieve the performance shown

Test Circuit:

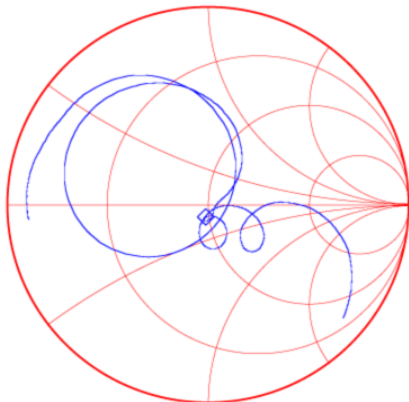
Actual matching values may vary due to PCB layout and parasitics



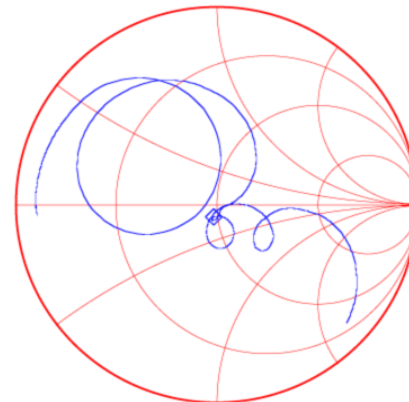
Typical Performance (at room temperature)



Input Smith Chart



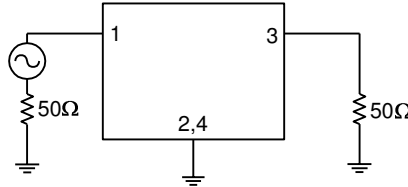
Output Smith Chart



Matching Schematics

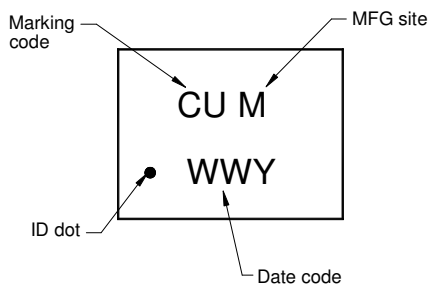
Actual matching values may vary due to PCB layout and parasitics

50 Ω
Single-ended
Input



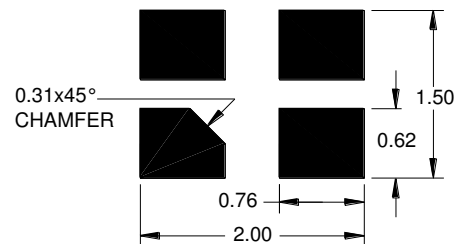
50 Ω
Single-ended
Output

Marking



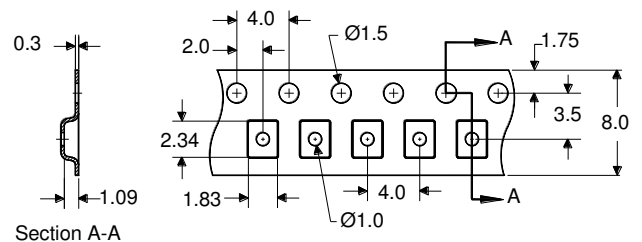
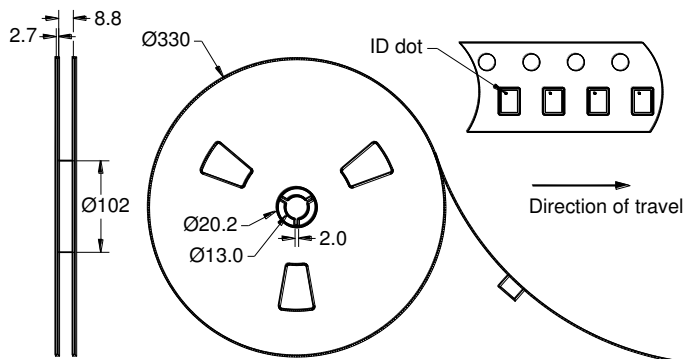
The date code consists of: WW = 2 digit week,
Y = last digit of year, M = manufacturing site code

PCB Footprint



This footprint represents a recommendation only
Dimensions shown are nominal in millimeters

Tape and Reel




Dimensions shown are nominal in millimeters
Packaging quantity: 10000 units/reel

Maximum Ratings


Parameter	Symbol	Minimum	Maximum	Unit
Operating Temperature Range	T	-40	+85	°C
Storage Temperature Range	T _{stg}	-40	+85	°C

Important Notes

Warnings

- Electrostatic Sensitive Device (ESD) 
- Avoid ultrasonic exposure

RoHS Compliance

- This product complies with EU directive 2002/95/EC (RoHS) 

Solderability

- Compatible with JEDEC J-STD-020C **Pb**-free process, **260 °C** peak reflow temperature ([see soldering profile](#))

Links to Additional Technical Information

[PCB Layout Tips](#)

[Qualification Flowchart](#)

[Soldering Profile](#)

[S-Parameters](#)

[RoHS Information](#)

[Other Technical Information](#)

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